# μPD431001
# 1,048,576 x 1-Bit
# Static CMOS RAM

## Description

The μPD431001 is a 1,048,576-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD431001 a high-speed device that requires no clock or refreshing. The μPD431001 is available in 28-pin plastic SOJ packaging.

## Features

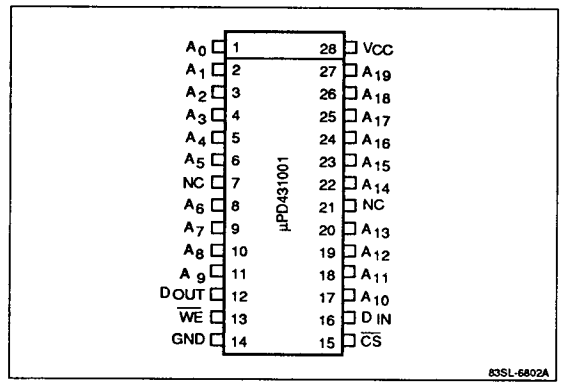
- 1,048,576-word x 1-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - — 140 mA max (active)
  - — 2 mA max (standby)
- Standard 400-mil, 28-pin plastic SOJ packaging

## Ordering Information

| Part Number | | Access Time (max) | Package |
|---|---|---|---|
| μPD431001 | LE-20 | 20 ns | 28-pin plastic SOJ |
| | LE-25 | 25 ns | |
| | LE-35 | 35 ns | |

## Pin Configuration

***28-Pin Plastic SOJ***




## Pin Identification

| Symbol | Function |
|---|---|
| $A_0$ - $A_{19}$ | Address inputs |
| $D_{IN}$ | Data input |
| $D_{OUT}$ | Data output |
| $\overline{CS}$ | Chip select |
| $\overline{WE}$ | Write enable |
| GND | Ground |
| $V_{CC}$ | +5-volt power supply |
| NC | No connection |

## Absolute Maximum Ratings

| | |
|---|---|
| Power supply voltage, $V_{CC}$ | −0.5 to +7.0 V |
| Input voltage, $V_{IN}$ (Note 1) | −0.5 to $V_{CC}$ + 0.3 V |
| Output voltage, $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.3 V |
| Operating temperature, $T_{OPR}$ | 0 to +70°C |
| Storage temperature, $T_{STG}$ | −55 to +125°C |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Notes:**

(1) $V_{IN}$ = −3.0 V minimum for 10 ns maximum pulse.

## Truth Table

| $\overline{CS}$ | $\overline{WE}$ | Function | $D_{OUT}$ | $I_{CC}$ |
|---|---|---|---|---|
| H | X | Not selected | High-Z | Standby |
| L | H | Read | Output data | Active |
| L | L | Write | High-Z | Active |

**Note:**

(1) X = don't care

## Capacitance

$T_A$ = +25°C; f = 1 MHz (Note 1); $V_{IN}$ and $V_{OUT}$ = 0 V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_I$ | | | 6 | pF |
| Output capacitance | $C_O$ | | | 10 | pF |

**Notes:**

(1) This parameter is sampled and not 100% tested.

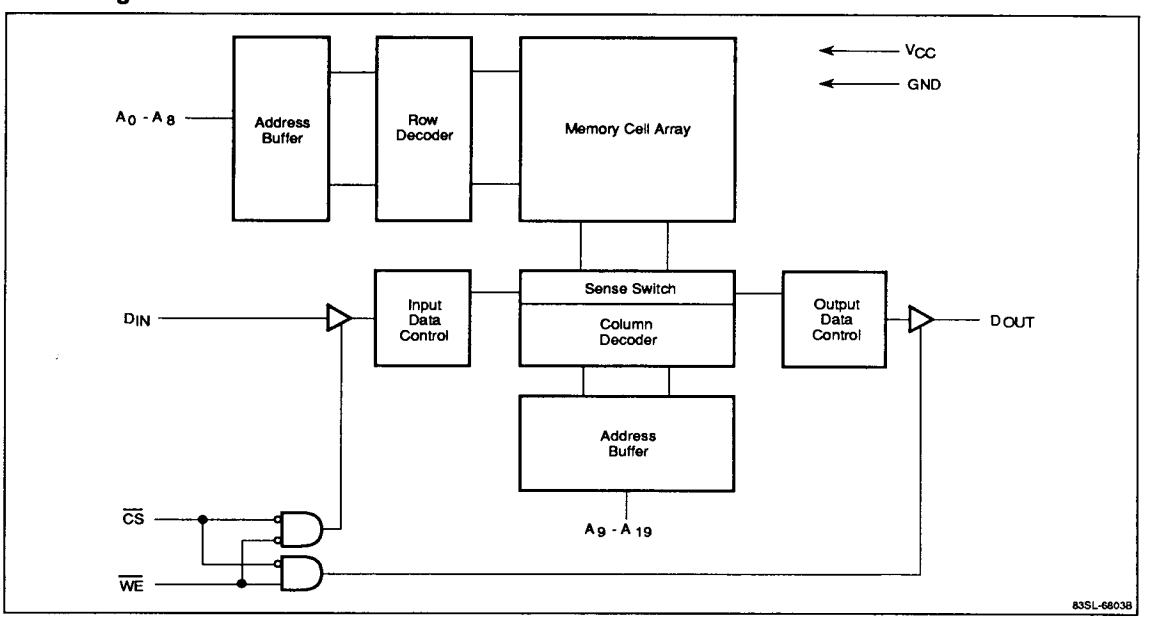
## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input voltage, low | $V_{IL}$ | −0.5 | | 0.8 | V |
| Input voltage, high | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V |
| Ambient temperature | $T_A$ | 0 | | 70 | °C |

**Note:**

(1) $V_{IL}$ = −3.0 V minimum for 10 ns maximum pulse.

## Block Diagram



## DC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | −2 | | 2 | μA | $V_{IN}$ = 0 V to $V_{CC}$ |
| Output leakage current | $I_{LO}$ | −2 | | 2 | μA | $V_{OUT}$ = 0 V to $V_{CC}$; $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ |
| Standby supply current | $I_{SB}$ | | | 30 | mA | $\overline{CS}$ = $V_{IH}$; $V_{IN}$ = $V_{IH}$ or $V_{IL}$ |
| | $I_{SB1}$ | | | 2 | mA | $\overline{CS}$ ≥ $V_{CC}$ − 0.2 V; $V_{IN}$ ≤ 0.2 V or ≥ $V_{CC}$ − 0.2 V |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8.0 mA |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −4.0 mA |

## AC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| | | μPD431001-20 | | μPD431001-25 | | μPD431001-35 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| ***Read Operation*** | | | | | | | | | |
| Operating supply current | $I_{CC}$ | | 140 | | 120 | | 100 | mA | $\overline{CS}$ = $V_{IL}$; $t_{RC}$ = $t_{RC}$ (min); $I_{OUT}$ = 0 mA |
| Read cycle time | $t_{RC}$ | 20 | | 25 | | 35 | | ns | (Note 2) |
| Read access time | $t_{AA}$ | | 20 | | 25 | | 35 | ns | |
| Chip select access time | $t_{ACS}$ | | 20 | | 25 | | 35 | ns | |
| Output hold from address change | $t_{OH}$ | 5 | | 5 | | 5 | | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 5 | | 5 | | 5 | | ns | (Note 3) |
| Chip deselect to output in high-Z | $t_{CHZ}$ | 0 | 8 | 0 | 10 | 0 | 15 | ns | (Note 4) |
| ***Write Operation*** | | | | | | | | | |
| Write cycle time | $t_{WC}$ | 20 | | 25 | | 35 | | ns | (Note 2) |
| Chip select to end of write | $t_{CW}$ | 15 | | 20 | | 30 | | ns | |
| Address valid to end of write | $t_{AW}$ | 15 | | 20 | | 30 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | 0 | | 0 | | ns | |
| Write pulse width | $t_{WP}$ | 15 | | 15 | | 25 | | ns | |
| Write recovery time | $t_{WR}$ | 3 | | 3 | | 3 | | ns | |
| Data valid to end of write | $t_{DW}$ | 12 | | 15 | | 20 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | 0 | | 0 | | ns | |
| Write enable to output in high-Z | $t_{WHZ}$ | | 8 | 0 | 10 | 0 | 10 | ns | (Note 4) |
| Output active from end of write | $t_{OW}$ | 0 | | 0 | | 0 | | ns | (Note 3) |

**Notes:**

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 2.

(4) The transition is measured at $V_{OL}$ + 200 mV and $V_{OH}$ − 200 mV with the load shown in figure 2.

***Figure 1. Output Load***

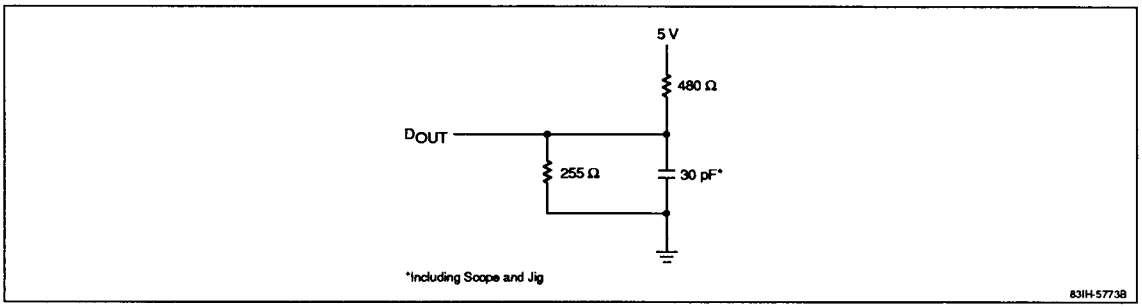
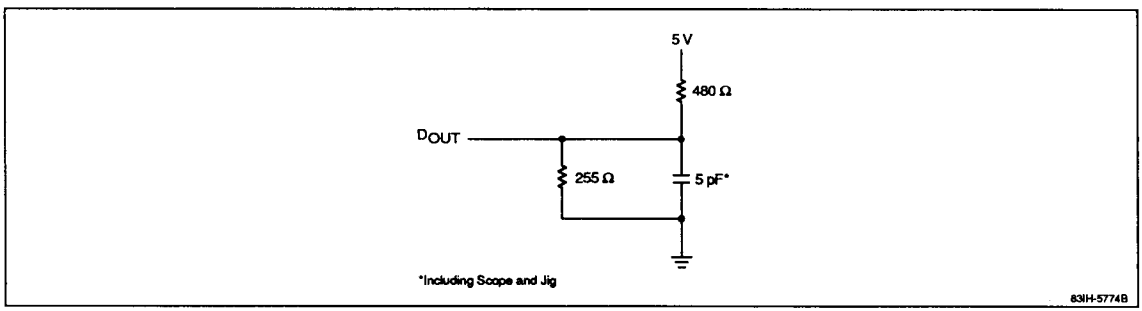
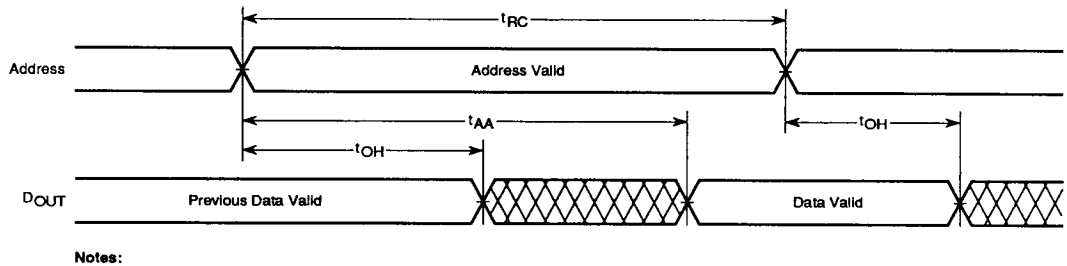



***Figure 2. Output Load for $t_{CHZ}$, $t_{CLZ}$, $t_{OW}$, and $t_{WHZ}$***



## Timing Waveforms

### *Address Access Cycle*




**Notes:**
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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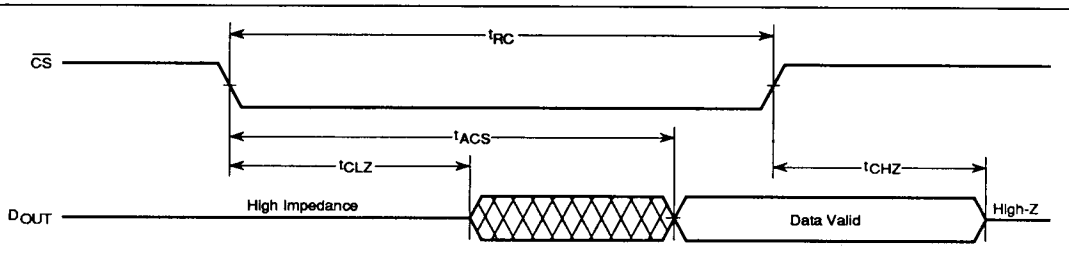
### *Chip Select Access Cycle*




**Notes:**
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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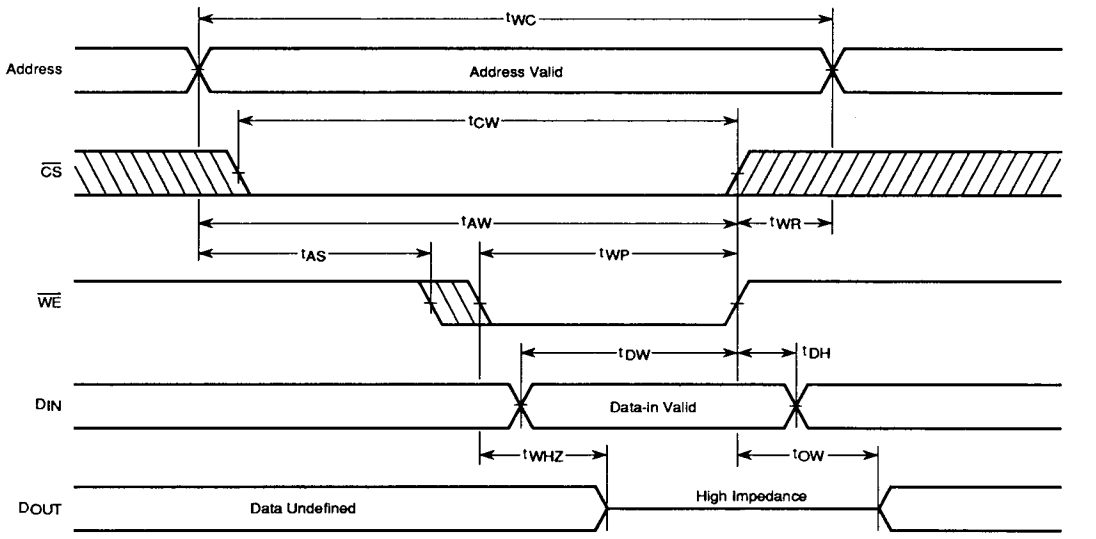
## Timing Waveforms (cont)

### $\overline{WE}$-Controlled Write Cycle




**Notes:**

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] $t_{WR}$ is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of $t_{WC}$.

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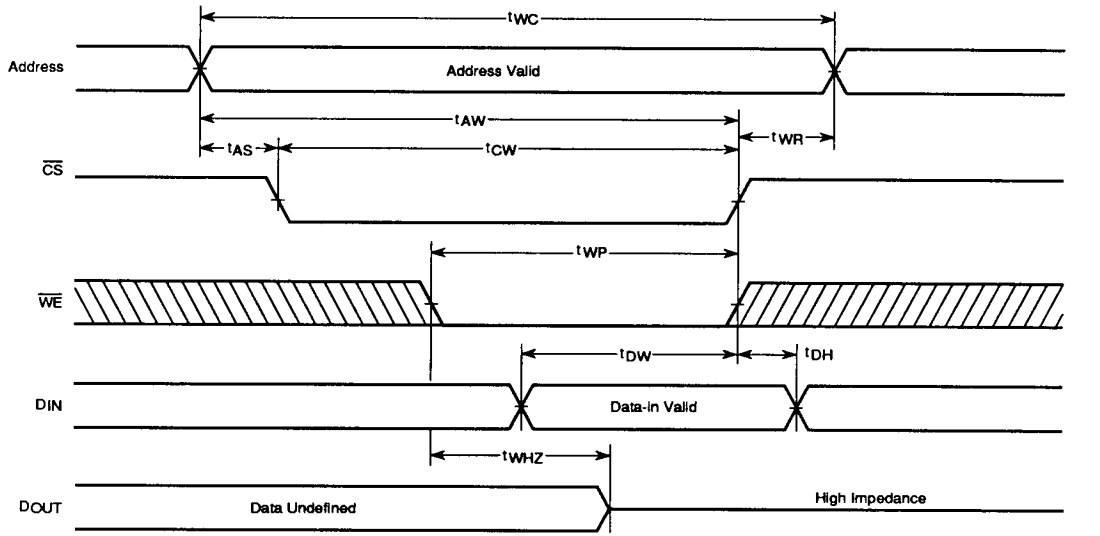
## Timing Waveforms (cont)

### $\overline{CS}$-Controlled Write Cycle




**Notes:**

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] $t_{WR}$ is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of $t_{WC}$.

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