NEC

MOS INTEGRATED CIRCUIT

μPD42S16400L, 4216400L, 42S17400L, 4217400L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μPD42S16400L, 4216400L, 42S17400L, 4217400L are 4,194,304 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycles and the μPD42S16400L, 42S17400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 26-pin plastic TSOP(II) and 26-pin plastic SOJ.

Features

- 4,194,304 words by 4 bits organization
- Fast page mode
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIM.)
μPD42S16400L-A60, 4216400L-A60	288 mW	60 ns	110 ns	40 ns
μPD42S17400L-A60, 4217400L-A60	360 mW			
μPD42S16400L-A70, 4216400L-A70	252 mW	70 ns	130 ns	45 ns
μPD42S17400L-A70, 4217400L-A70	324 mW			
μPD42S16400L-A80, 4216400L-A80	216 mW	80 ns	150 ns	50 ns
μPD42S17400L-A80, 4217400L-A80	288 mW			

- The μPD42S16400L, μPD42S17400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

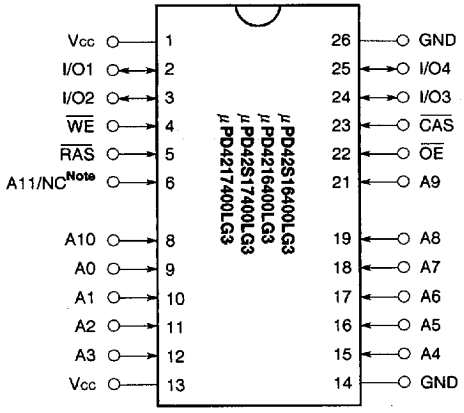
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16400L	4,096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh. $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD42S17400L	2,048 cycles/128 ms		
μPD4216400L	4,096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μPD4217400L	2,048 cycles/32 ms		

Ordering Information

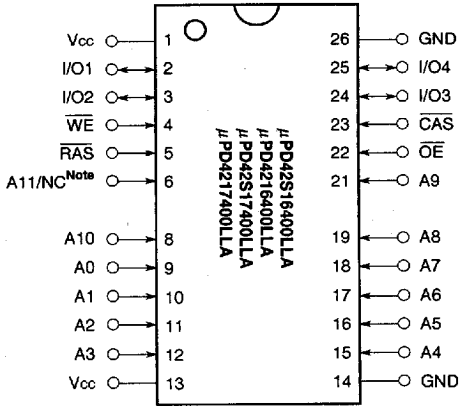
Part number	Access time (MAX.)	Package	Refresh
μPD42S16400LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17400LG3-A60			
μPD42S16400LG3-A70	70 ns		
μPD42S17400LG3-A70			
μPD42S16400LG3-A80	80 ns		
μPD42S17400LG3-A80			
μPD42S16400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD42S17400LLA-A60			
μPD42S16400LLA-A70	70 ns		
μPD42S17400LLA-A70			
μPD42S16400LLA-A80	80 ns		
μPD42S17400LLA-A80			
μPD4216400LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217400LG3-A60			
μPD4216400LG3-A70	70 ns		
μPD4217400LG3-A70			
μPD4216400LG3-A80	80 ns		
μPD4217400LG3-A80			
μPD4216400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4217400LLA-A60			
μPD4216400LLA-A70	70 ns		
μPD4217400LLA-A70			
μPD4216400LLA-A80	80 ns		
μPD4217400LLA-A80			

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)



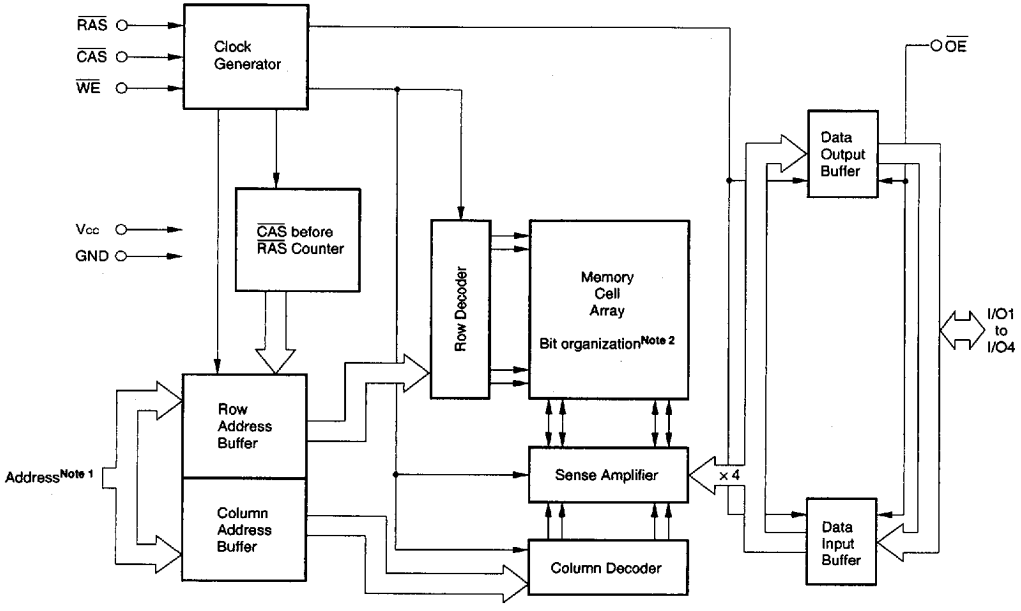
26-pin Plastic SOJ (300 mil)



Note A11 ··· μPD42S16400L, 4216400L
NC ··· μPD42S17400L, 4217400L

A0 to A11	:	Address Inputs
I/O1 to I/O4	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16400L, 4216400L	A0 - A11	A0 - A9
μPD42S17400L, 4217400L	A0 - A10	A0 - A10

2. μPD42S16400L, 4216400L ··· 4,096 × 1,024 × 4 μPD42S17400L, 4217400L ··· 2,048 × 2,048 × 4

Input/Output Pin Functions

The μPD42S16400L, 4216400L, 42S17400L, 4217400L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD42S16400L, 4216400L	A0 - A11	12 bits	10 bits
μPD42S17400L, 4217400L	A0 - A10	11 bits	11 bits

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)
[μPD42S16400L, 4216400L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		80	mA	1, 2, 3
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		70		
			I_O = 0 mA	t_{RAC} = 80 ns		60		
Standby current	μPD42S16400L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4216400L		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 60 ns		80	mA	1, 2, 3, 4
			t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		70		
				t_{RAC} = 80 ns		60		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ cycling	t_{RAC} = 60 ns		70	mA	1, 2, 5
			t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		80	mA	1, 2
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		70		
			I_O = 0 mA	t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16400L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (MAX.), 0 V ≤ V_{IL} ≤ 0.2 V Standby : $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		220	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16400L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH(MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD42S17400L, 4217400L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		100	mA	1, 2, 3
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		90		
			I_O = 0 mA	t_{RAC} = 80 ns		80		
Standby current	μPD42S17400L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4217400L		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 60 ns		100	mA	1, 2, 3, 4
			t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		90		
				t_{RAC} = 80 ns		80		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ cycling	t_{RAC} = 60 ns		70	mA	1, 2, 5
			t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		100	mA	1, 2
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		90		
			I_O = 0 mA	t_{RAC} = 80 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17400L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (MAX.), 0 V ≤ V_{IL} ≤ 0.2 V Standby : $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		200	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17400L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH(MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ V_{IL} (MAX.) and $\overline{CAS}$ ≥ V_{IH} (MIN.).

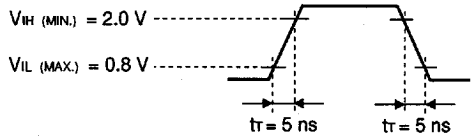
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

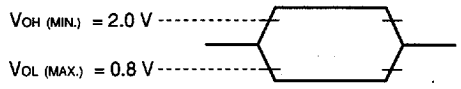
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

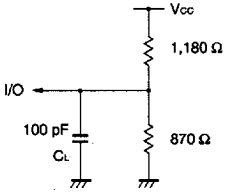
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	52	25	60	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	17	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	12	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	15	–	15	–	20	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	3	50	ns	
Refresh time	μPD42S16400L, 42S17400L	tREF	–	128	–	128	–	128	ms	4
	μPD4216400L		–	64	–	64	–	64	ms	
	μPD4217400L		–	32	–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	160	–	180	–	205	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	–	95	–	110	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	–	43	–	50	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	55	–	60	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	70	–	ns	1

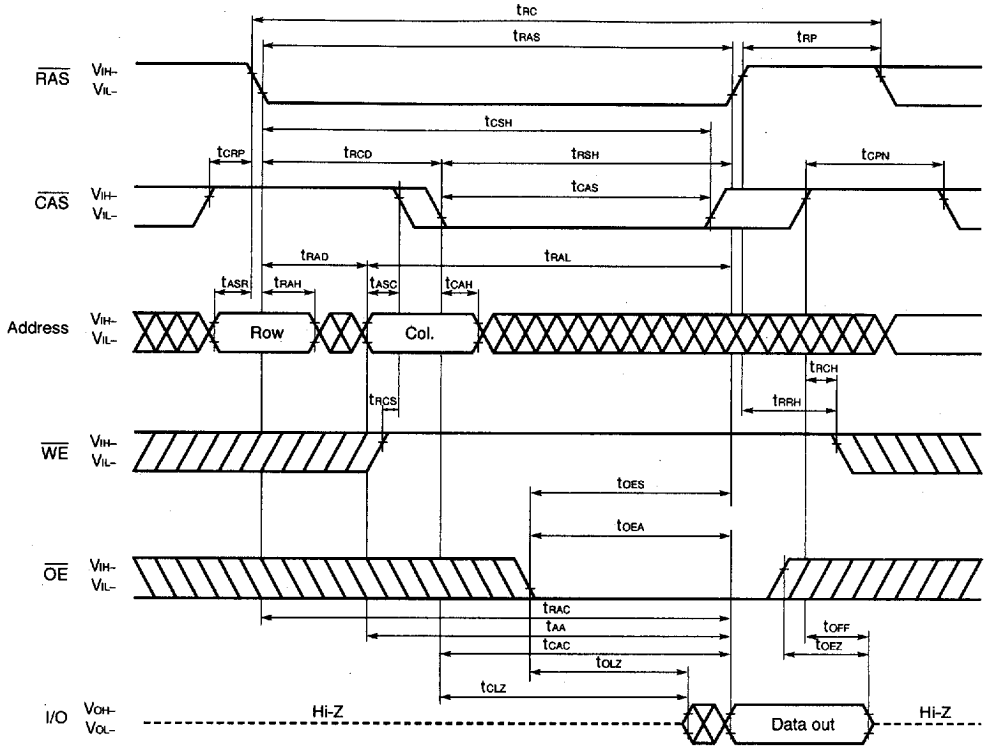
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

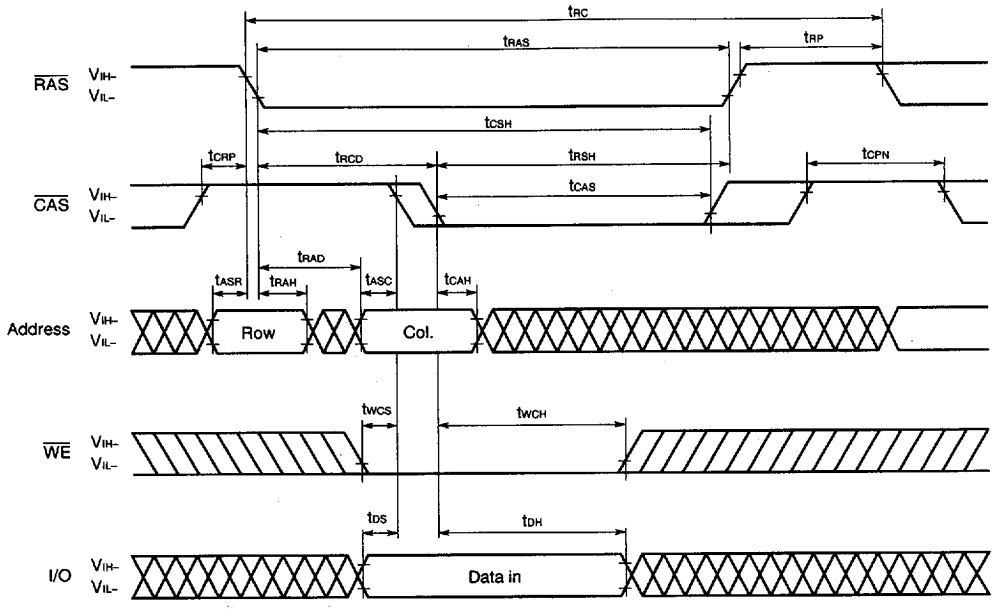
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	150	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

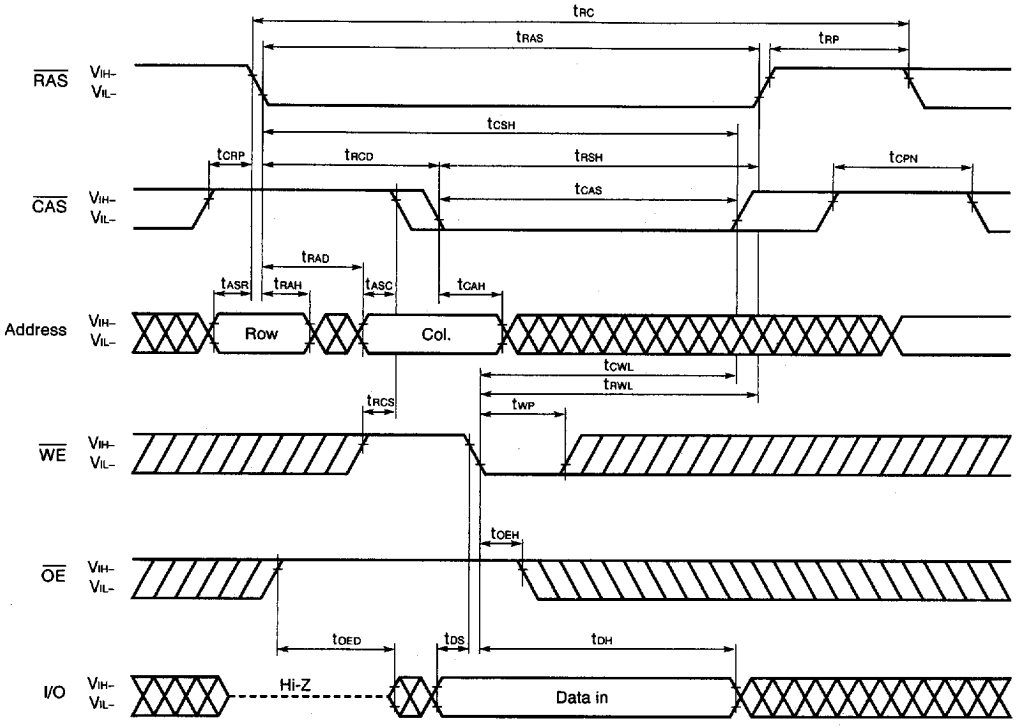


Early Write Cycle

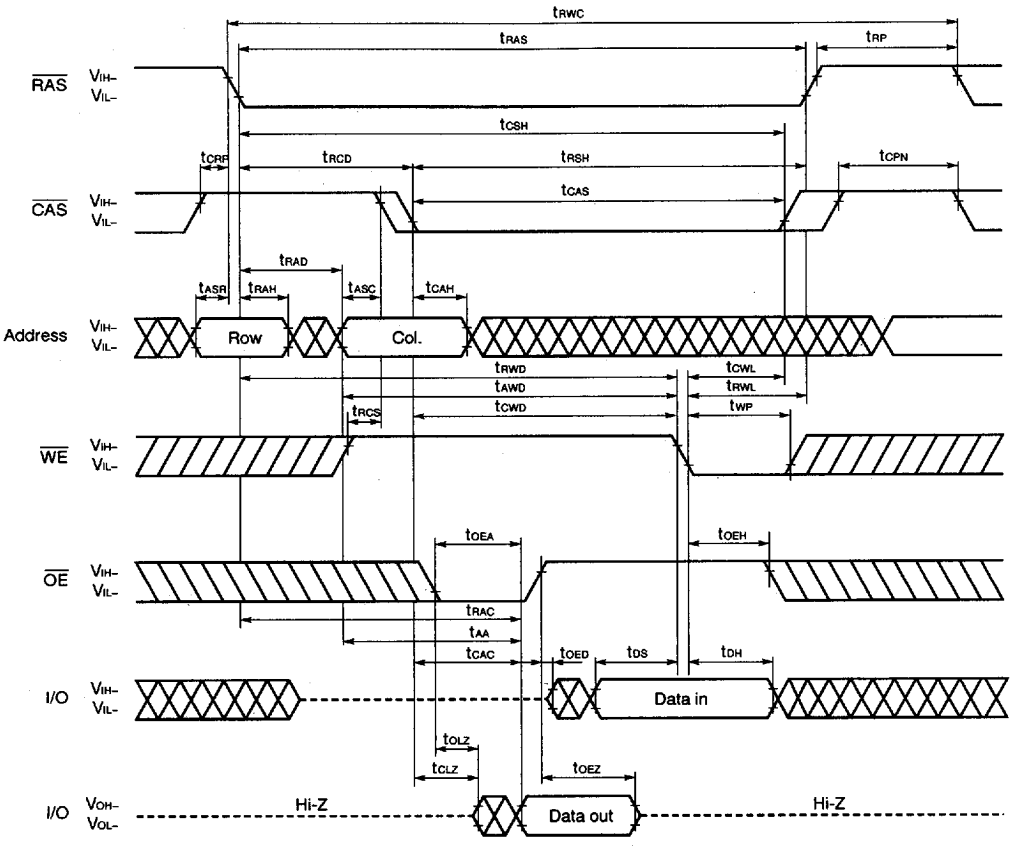


Remark $\overline{OE}$: Don't care

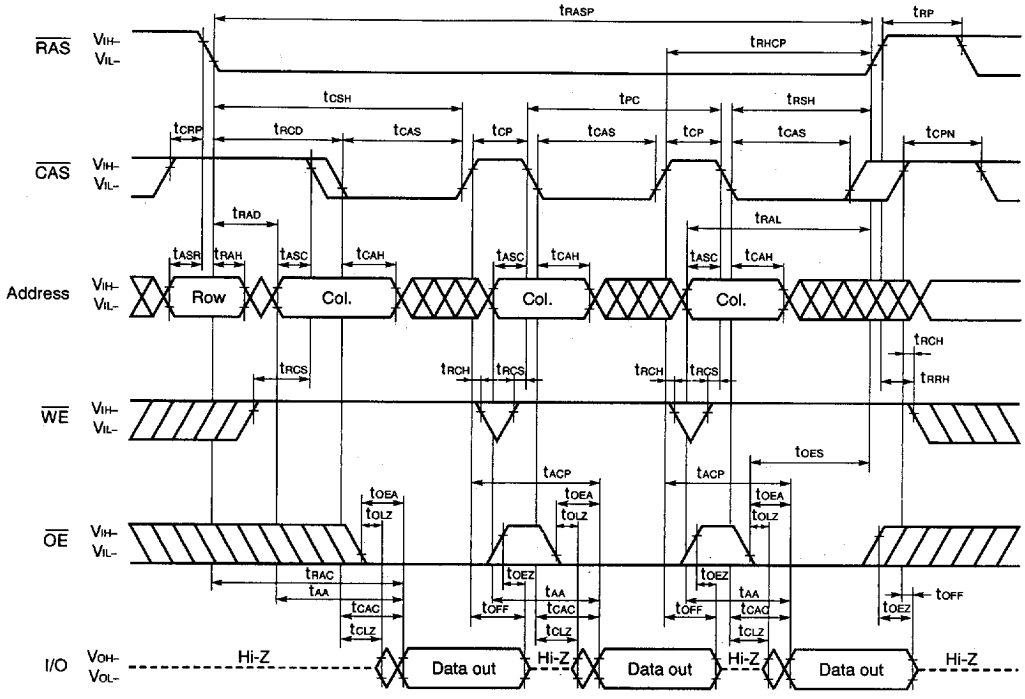
Late Write Cycle



Read Modify Write Cycle

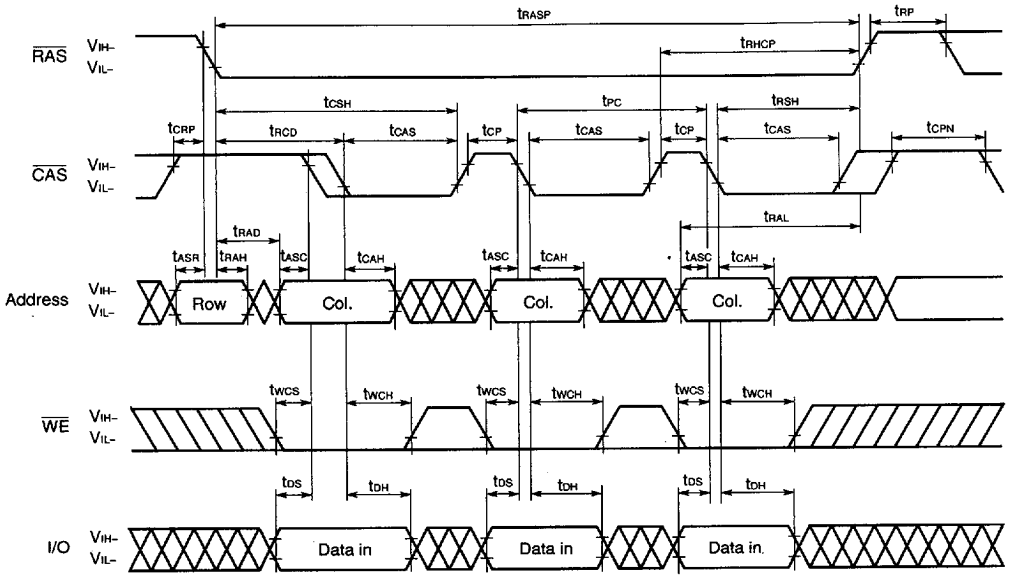


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

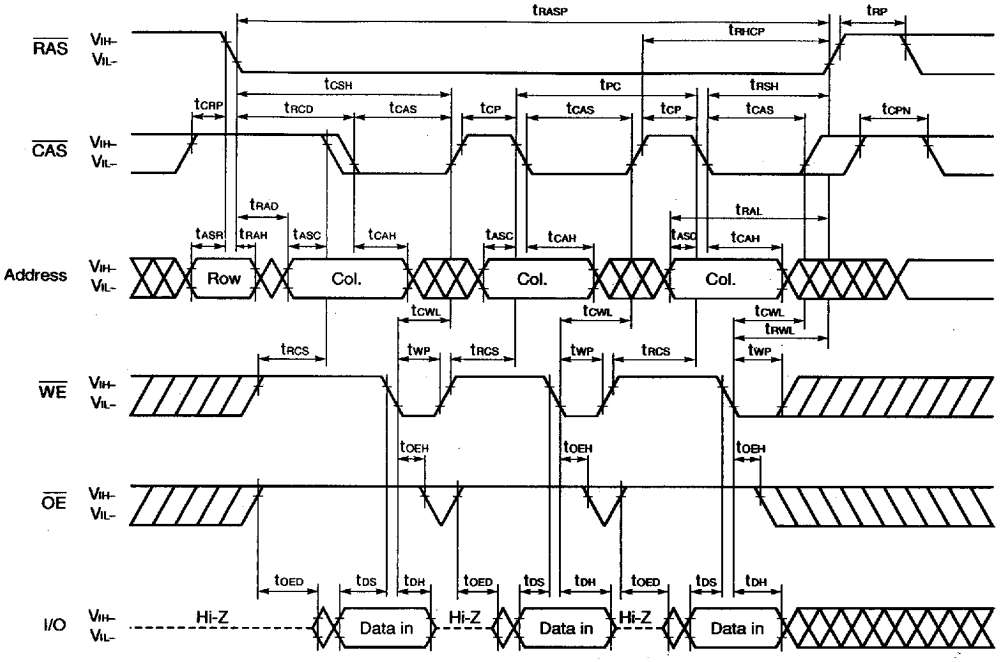
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

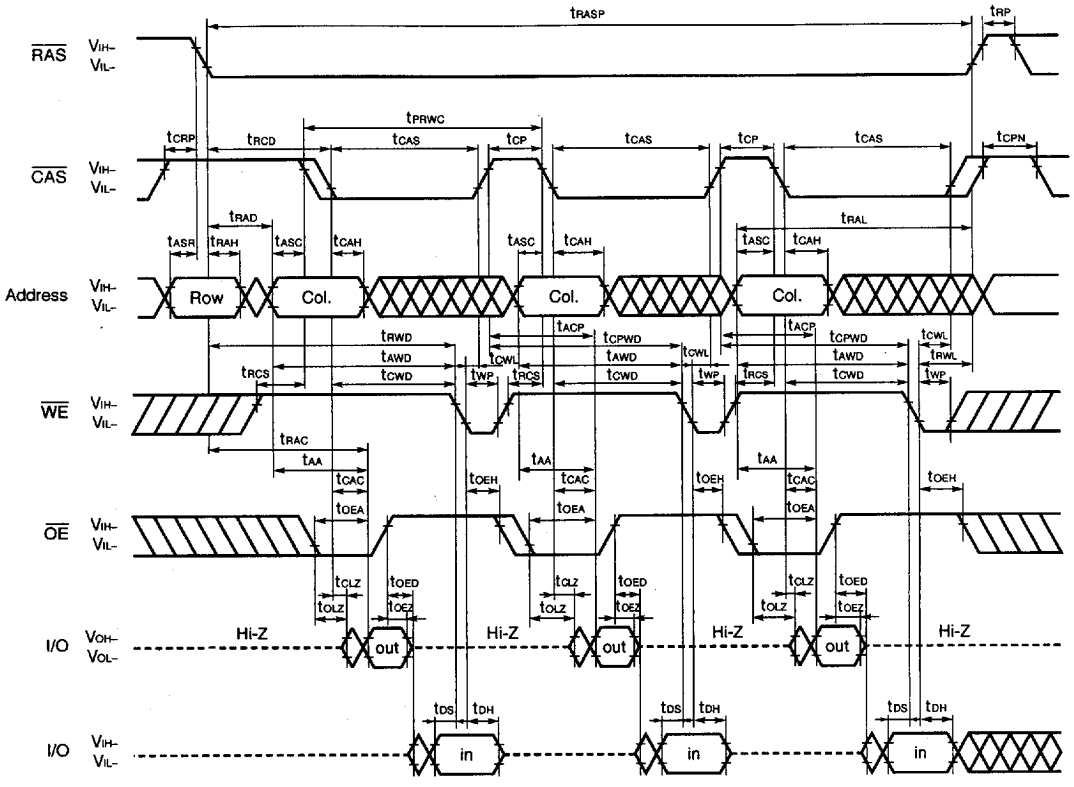
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



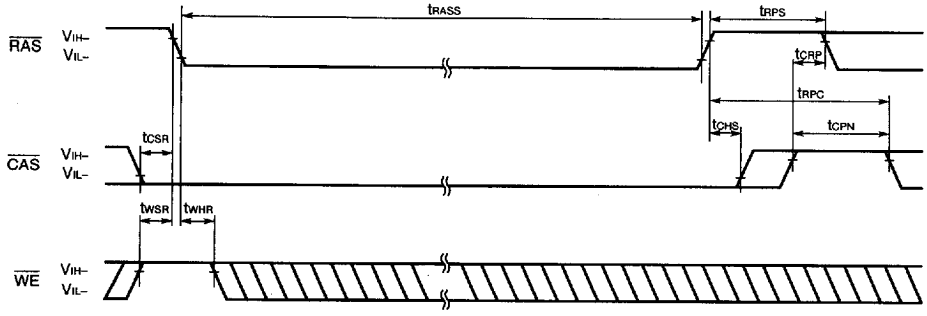
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16400L, 42S17400L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S16400L : 4,096 times within a 64 ms interval
μPD42S17400L : 2,048 times within a 32 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

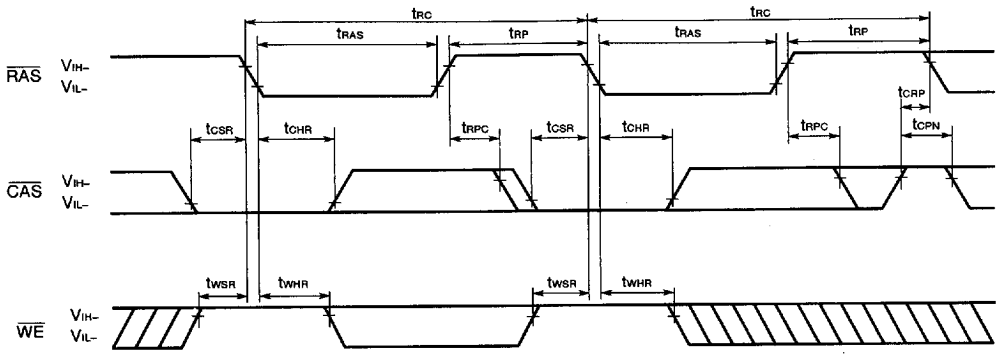
μPD42S16400L : 4,096 times within a 64 ms interval
μPD42S17400L : 2,048 times within a 32 ms interval

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100$ μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S16400L : 4,096 times within a 128 ms interval
μPD42S17400L : 2,048 times within a 128 ms interval

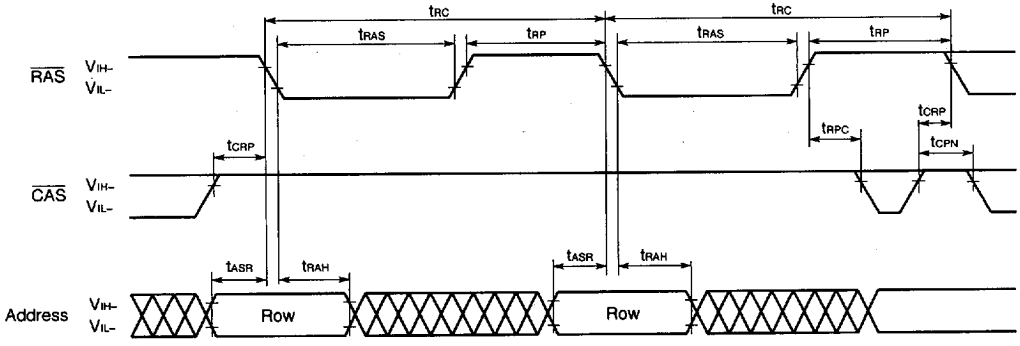
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



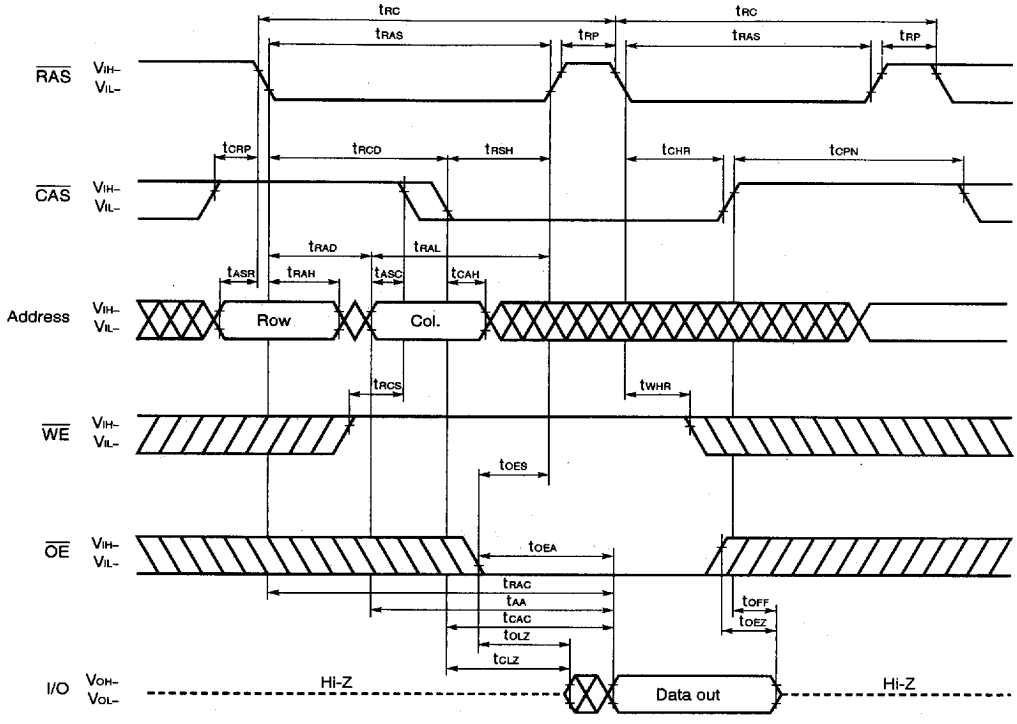
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

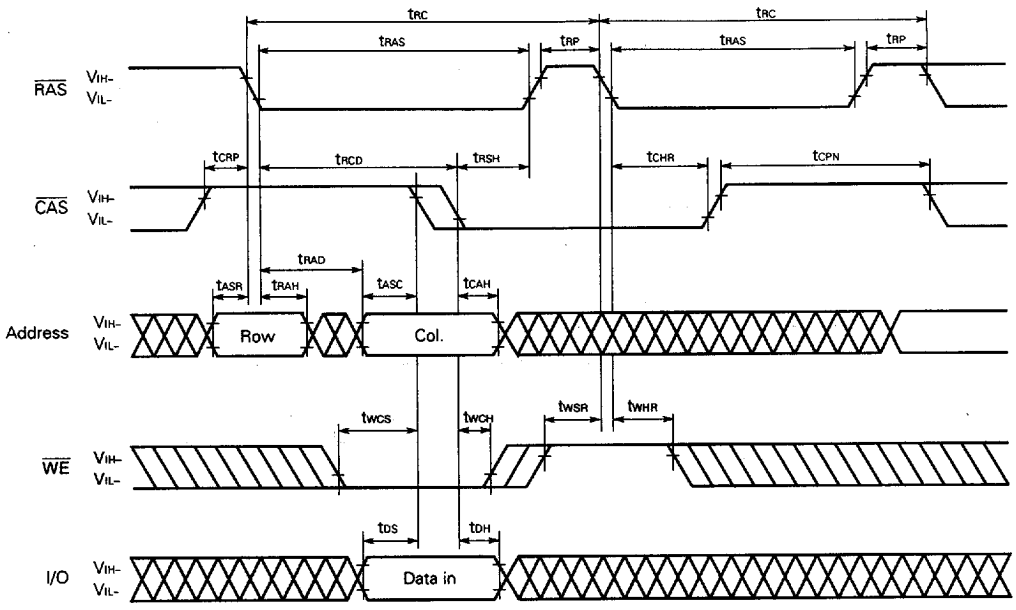


Remark $\overline{WE}$, $\overline{OE}$: Don't care、I/O: Hi-Z

Hidden Refresh Cycle (Read)

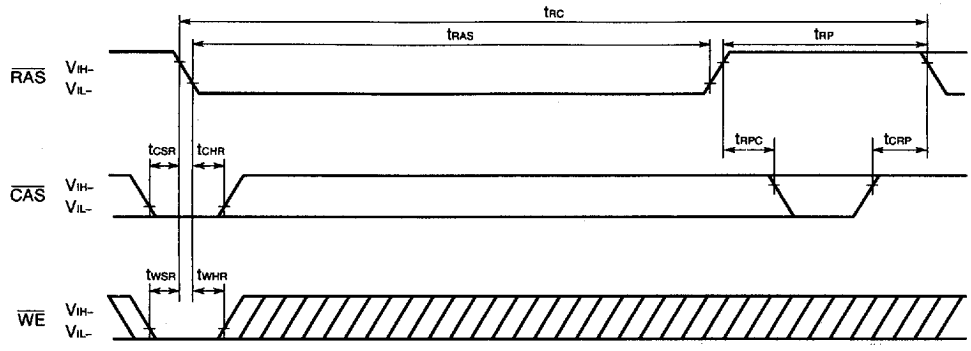


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

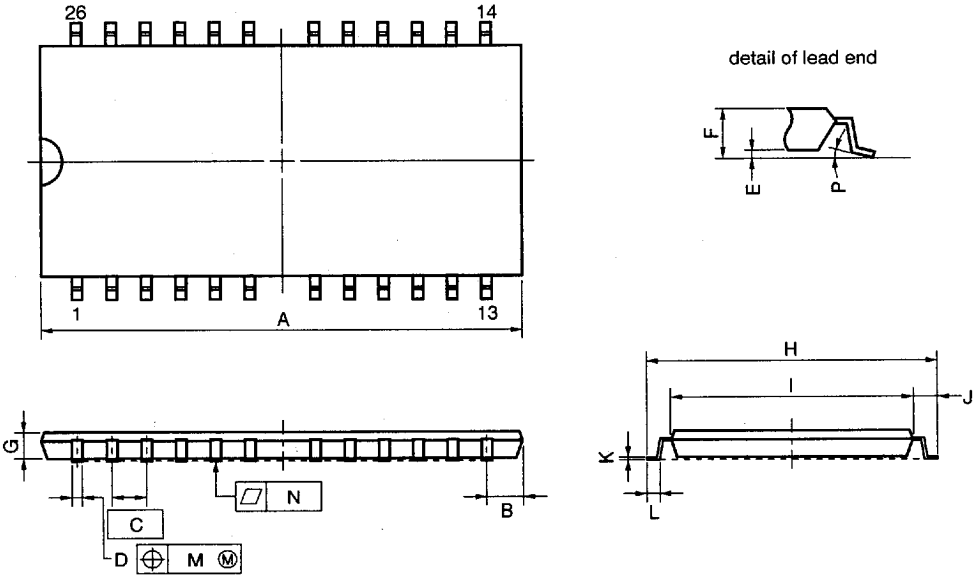
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



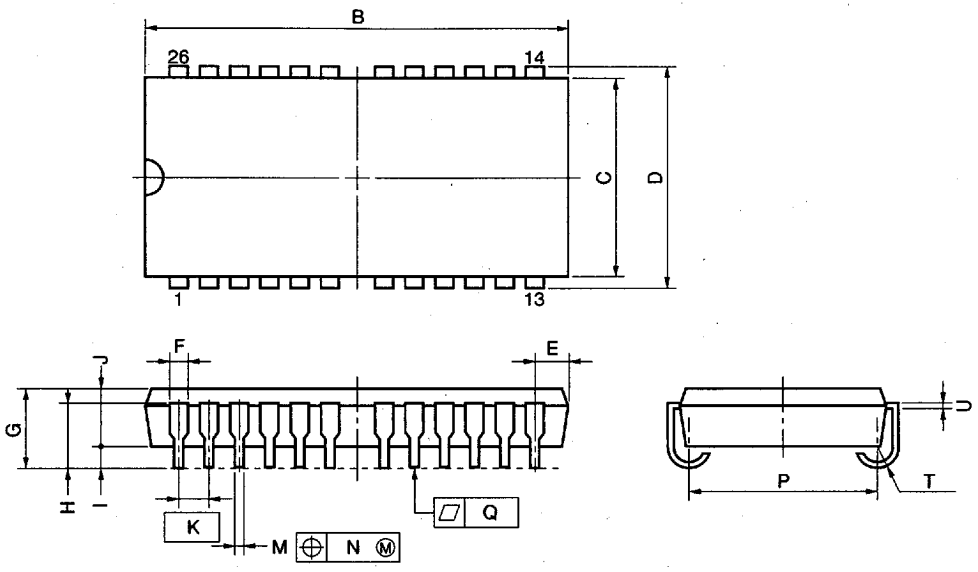
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03 ± 0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16400L, 4216400L, 42S17400L, 4217400L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400LG3, 4216400LG3, 42S17400LG3, 4217400LG3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limi: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16400LLA, 4216400LLA, 42S17400LLA, 4217400LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".