μPB100A484
4,096 x 4-Bit
100K ECL RAM

Description

The μPB100A484 is a very high-speed 100K interface ECL RAM organized as 4K words by 4 bits and designed with open emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack packages.

Features

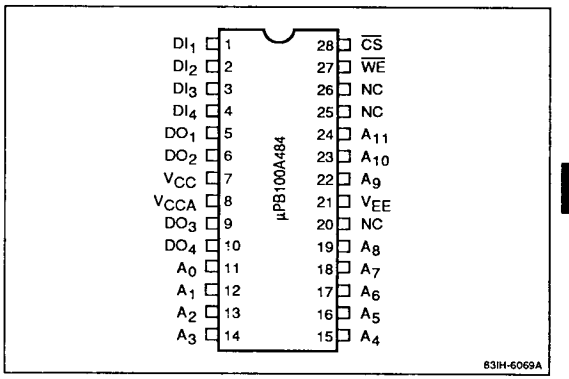
- 4096 word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times and low power consumption
- 28-pin cerdip and flatpack packaging
- Center power pins

Ordering Information

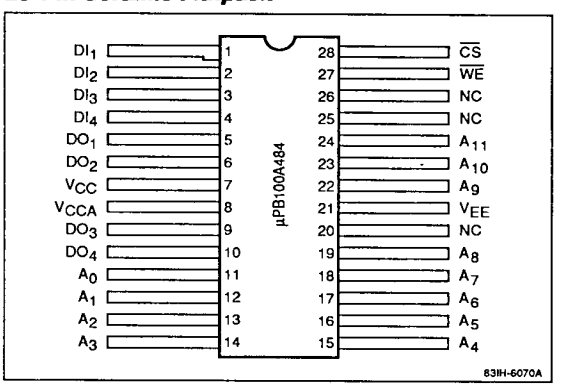
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100A484B-5	5 ns	TBD	28-pin ceramic flatpack
B-7	7 ns	TBD	
μPB100A484D-5	5 ns	TBD	28-pin cerdip
D-7	7 ns	TBD	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−4.5-volt power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

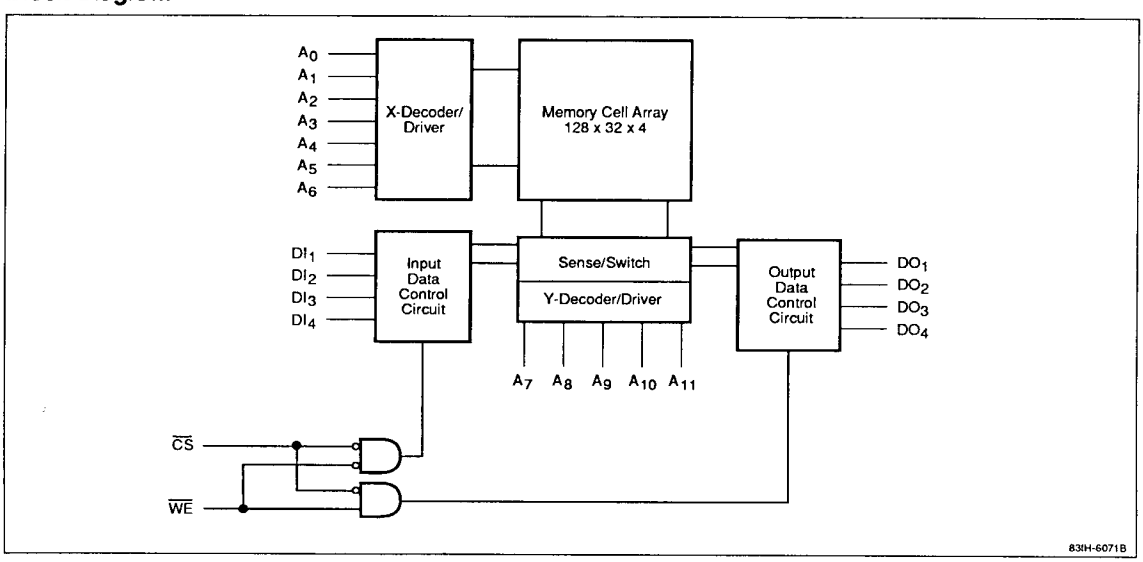
Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	TBD			mA	μPB100A484-5: all inputs and outputs open
		TBD			mA	μPB100A484-7: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100A484-5			μPB100A484-7				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

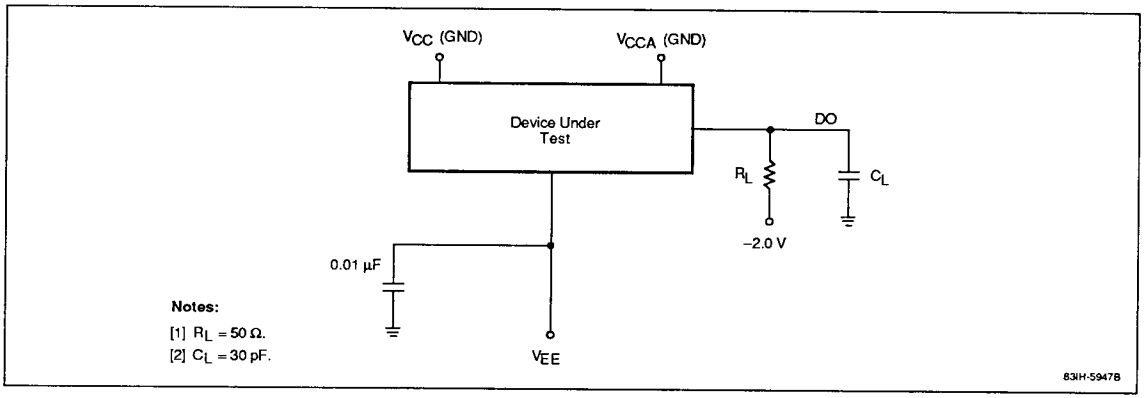
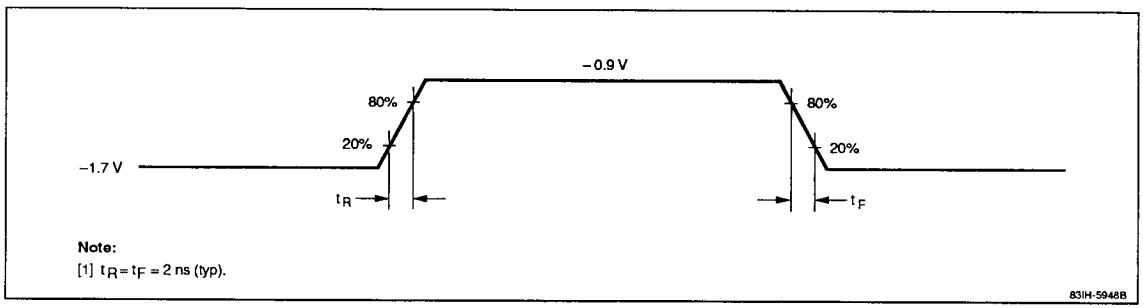
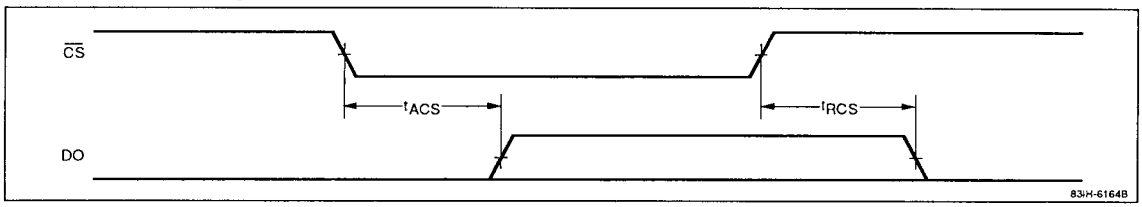


Figure 2. Input Pulse

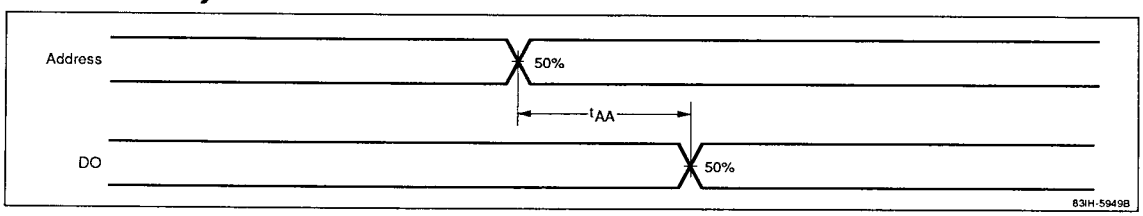


Timing Waveforms

Chip Select Access Cycle



Address Access Cycle



Write Cycle