CYF0018V, CYF0036V CYF0072V

18/36/72 Mbit Programmable FIFOs

Features

- Memory organization
  - Industry's largest first in first out (FIFO) memory densities: 18 Mbit, 36 Mbit, and 72 Mbit
  - Selectable memory organization: ×9, ×12, ×16, ×18, ×20, ×24, ×32, ×36
- Up to 133-MHz clock operation
- Unidirectional operation
- Independent read and write ports
  - Supports simultaneous read and write operations
  - Reads and writes operate on independent clocks up to a maximum ratio of two enabling data buffering across clock domains
  - Supports multiple I/O voltage standard: low voltage complementary metal oxide semiconductor (LVCMOS) 3.3 V and 1.8 V voltage standards.
- Input and output enable control for write mask and read skip operations
- Mark and retransmit: resets read pointer to user marked position
- Empty, full, half-full, and programmable almost-empty and almost-full status flags with preselected offsets
- Flow-through mailbox register to send data from input to output port, bypassing the FIFO sequence
- Configure programmable flags and registers through serial or parallel modes
- Separate serial clock (SCLK) input for serial programming
- Master reset to clear entire FIFO
- Partial reset to clear data but retain programmable settings
- Joint test action group (JTAG) port provided for boundary scan function
- Industrial temperature range: –40 °C to +85 °C

Functional Description

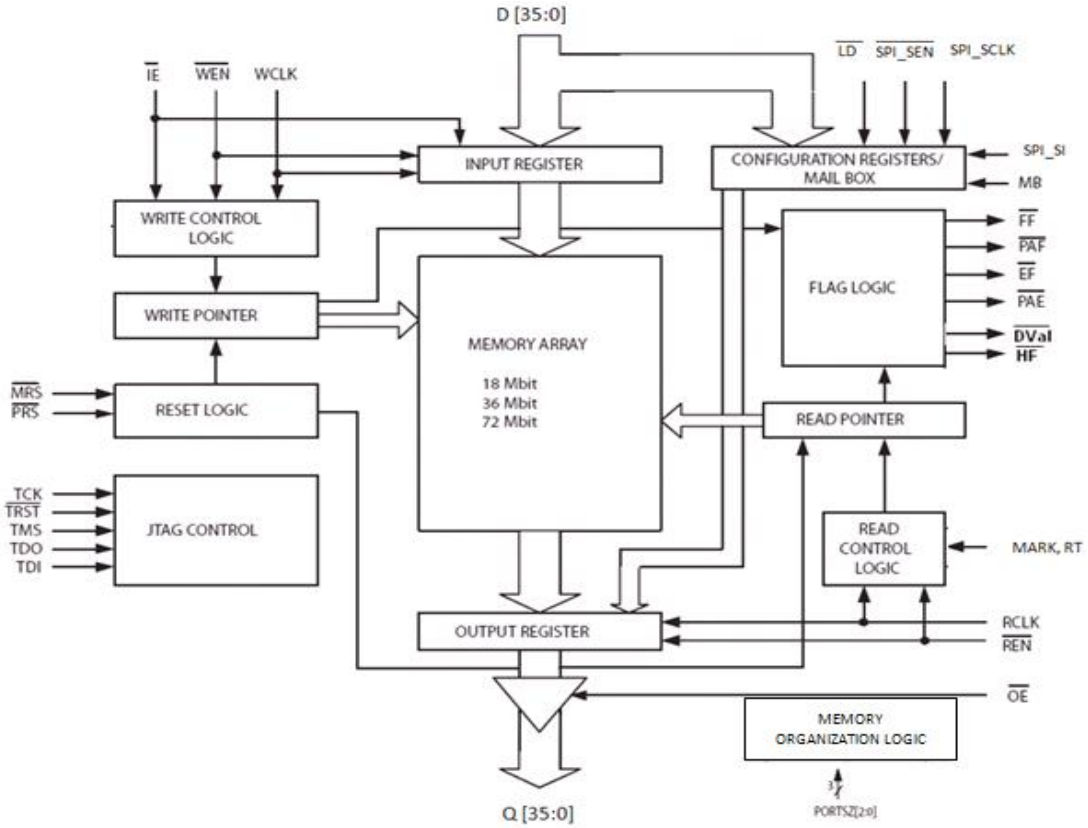
The Cypress programmable FIFO family offers the industry's highest-density programmable FIFO memory device. It has independent read and write ports, which can be clocked up to 133 MHz. User can configure input and output bus sizes. The maximum bus size of 36 bits enables a maximum data throughput of 4.8 Gbps. The read and write ports can support multiple I/O voltage standards. The user-programmable registers enable user to configure the device operation as desired. The device also offers a simple and easy-to-use interface to reduce implementation and debugging efforts, improve time-to-market, and reduce engineering costs. This makes it an ideal memory choice for a wide range of applications including multiprocessor interfaces, video and image processing, networking and telecommunications, high-speed data acquisition, or any system that needs buffering at very high speeds across different domains.

As implied by the name, the functionality of the FIFO is such that the data is read out of the read port in the same sequence in which it was written into the write port. The data is sequentially written into the FIFO from the write port. If the writes and inputs are enabled, the data on the write port gets written into the device at the rising edge of the write clock. Enabling the reads and outputs fetches data on the read port at every rising edge of the read clock. Both reads and writes can occur simultaneously at different speeds provided the ratio between read and write clock is in the range of 0.5 to 2. Appropriate flags are set whenever the FIFO is empty, full, half-full, almost-full, or almost-empty.

The device also supports mark and retransmit of data, and a flow-through mailbox register.

All product features and specs are common to all densities (CYF0072V, CYF0036V, and CYF0018V) unless otherwise specified. All descriptions are given assuming the device is CYF0072V operated in ×36 mode. They hold good for other densities (CYF0036V, and CYF0018V) and all port sizes ×9, ×12, ×16, ×18, ×20, ×24 and ×32 unless otherwise specified. the only difference will be in the input and output bus width. Table 1 shows the part of bus with valid data from D[35:0] and Q[35:0] in ×9, ×12, ×16, ×18, ×20, ×24, ×32 and ×36 modes.

Logic Block Diagram



Contents

Pin Diagram for CYF 0 XXX V

Figure 1. 209-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{FF}$	D0	D1	DNU	PORTSZ0	PORTSZ1	DNU	DNU	RT	Q0	Q1
B	$\overline{EF}$	D2	D3	DNU	DNU	PORTSZ2	DNU	DNU	$\overline{REN}$	Q2	Q3
C	D4	D5	$\overline{WEN}$	DNU	VCC1	DNU	VCC1	DNU	RCLK	Q4	Q5
D	D6	D7	V_{SS}	VCC1	DNU	$\overline{LD}$	DNU	VCC1	Vss	Q6	Q7
E	D8	D9	VCC2	VCC2	VCCIO	VCCIO	VCCIO	VCC2	VCC2	Q8	Q9
F	D10	D11	V_{SS}	V_{SS}	V_{SS}	DNU	V_{SS}	V_{SS}	V_{SS}	Q10	Q11
G	D12	D13	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q12	Q13
H	D14	D15	V_{SS}	V_{SS}	V_{SS}	VCC1	V_{SS}	V_{SS}	V_{SS}	Q14	Q15
J	D16	D17	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q16	Q17
K	DNU	DNU	WCLK	DNU	V_{SS}	$\overline{IE}$	V_{SS}	DNU	VCCIO	VCCIO	VCCIO
L	D18	D19	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q18	Q19
M	D20	D21	V_{SS}	V_{SS}	V_{SS}	VCC1	V_{SS}	V_{SS}	V_{SS}	Q20	Q21
N	D22	D23	VCC2	VCC2	VCCIO	VCC1	VCCIO	VCC2	VCC2	Q22	Q23
P	D24	D25	V_{SS}	V_{SS}	V_{SS}	$\overline{SPI\_SEN}$	V_{SS}	V_{SS}	V_{SS}	Q24	Q25
R	D26	D27	VCC2	VCC2	VCCIO	VCCIO	VCCIO	VCC2	VCC2	Q26	Q27
T	D28	D29	V_{SS}	VCC1	VCC1	SPI_SI	VCC1	VCC1	V_{SS}	Q28	Q29
U	$\overline{DVal}$	DNU	D30	D31	$\overline{PRS}$	DNU	SPI_SCLK	Vref	$\overline{OE}$	Q30	Q31
V	$\overline{PAF}$	$\overline{PAE}$	D32	D33	DNU	$\overline{MRS}$	MB	DNU	MARK	Q32	Q33
W	TDO	$\overline{HF}$	D34	D35	TDI	$\overline{TRST}$	TMS	TCK	Vref	Q34	Q35

Pin Definitions

Pin Name	I/O	Pin Description
D[35:0]	Input	Data inputs: Data inputs for a 36-bit bus
Q[35:0]	Output	Data outputs: Data outputs for a 36-bit bus
$\overline{WEN}$	Input	Write enable: $\overline{WEN}$ enables WCLK to write data into the FIFO memory and configuration registers.
$\overline{REN}$	Input	Read enable: $\overline{REN}$ enables RCLK to read data from the FIFO memory and configuration registers.
$\overline{IE}$	Input	Input enable: $\overline{IE}$ is the data input enable signal that controls the enabling and disabling of the 36-bit data input pins. If it is enabled, data on the D[35:0] pins is written into the FIFO. The internal write address pointer is always incremented at rising edge of WCLK if $\overline{WEN}$ is enabled, regardless of the $\overline{IE}$ level. This is used for 'write masking' or incrementing the write pointer without writing into a location.
$\overline{OE}$	Input	Output enable: When $\overline{OE}$ is LOW, FIFO data outputs are enabled; when $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high impedance) state.
WCLK	Input	Write clock: When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO if $\overline{LD}$ is high and into the configuration registers if $\overline{LD}$ is low.
RCLK	Input	Read clock: When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory if $\overline{LD}$ is high and from the configuration registers if $\overline{LD}$ is low.
$\overline{EF}$	Output	Empty flag: When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Output	Full flag: When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Output	Programmable almost-empty: When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. It is synchronized to RCLK.
$\overline{PAF}$	Output	Programmable almost-full: When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost-full offset value programmed into the FIFO. It is synchronized to WCLK.
$\overline{LD}$	Input	Load: When $\overline{LD}$ is LOW, D[7:0] (Q[7:0]) are written (read) into (from) the configuration registers. When $\overline{LD}$ is HIGH, D[35:0] (Q[35:0]) are written (read) into (from) the FIFO
RT	Input	Retransmit: A HIGH pulse on RT resets the internal read pointer to a physical location of the FIFO which is marked by the user (using MARK pin). With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer.
$\overline{MRS}$	Input	Master reset: $\overline{MRS}$ initializes the internal read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the configuration registers are all set to default values and flags are reset.
$\overline{PRS}$	Input	Partial reset: $\overline{PRS}$ initializes the internal read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the configuration register settings are all retained and flags are reset.
SPI_SCLK	Input	Serial clock: A rising edge on SPI_SCLK clocks the serial data present on the SPI_SI input into the offset registers if SPI_$\overline{SEN}$ is enabled.
SPI_SI	Input	Serial input: Serial input data in SPI mode.
$\overline{SPI\_SEN}$	Input	Serial enable: Enables serial loading of programmable flag offsets and configuration registers.
MARK	Input	Mark for retransmit: When this pin is asserted the current location of the read pointer is marked. Any subsequent retransmit operation resets the read pointer to this position.
MB	Input	Mailbox: When asserted the reads and writes happen to flow-through mailbox register.
TCK	Input	Test clock (TCK) Pin for JTAG
$\overline{TRST}$	Input	Reset pin for JTAG
TMS	Input	Test mode select (TMS) pin for JTAG
TDI	Input	Test data in (TDI) pin for JTAG
TDO	Output	Test data out (TDO) for JTAG
$\overline{HF}$	Output	Half-full flag: When $\overline{HF}$ is LOW, half of the FIFO is full. $\overline{HF}$ is synchronized to WCLK.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
$\overline{\text{DVal}}$	Output	Data valid: Active low data valid signal to indicate valid data on Q[35:0]
PORTSZ [2:0]	Input	Port word size select: Port word width select pins (common for read and write ports)
VCC1	Power Supply	Core voltage supply 1: 1.8V supply voltage
VCC2	Power Supply	Core voltage supply 2: 1.5V supply voltage
VCCIO	Power Supply	Supply for I/Os
Vref	Input Reference	Reference voltage: Reference voltage (regardless of I/O standard used)
V_{SS}	Ground	Ground
DNU	–	Do not use: These pins need to be left floating

Architecture

The CYF0072V, CYF0036V, and CYF0018V are of memory arrays of 72 Mbit, 36 Mbit, and 18 Mbit respectively. The memory organization is user configurable and word sizes can be selected as x9, x12, x16, x18, x20, x24, x32, or x36. The logic blocks to implement FIFO functionality and the associated features are built around these memory arrays.

The input and output data buses have a maximium width of 36 bits. The input data bus goes to an input register and the data flow from the input register to the memory is controlled by the write logic block. The inputs to the write logic block are WCLK, WEN and IE. When the writes are enabled through WEN and if the inputs are enabled by IE, then the data on the input bus is written into the memory array at the rising edge of WCLK. This also increments the write pointer. Enabling writes but disabling the data input pins through IE only increments the write pointer without doing any writes or altering the contents of the location.

Similarly, the output register is connected to the data output bus. Transfer of contents from the memory to the output register is controlled by the read control logic. The inputs to the read control logic include RCLK, REN, OE, RT and MARK. When reads are enabled by REN and outputs are enabled through OE, the data from the memory pointed by the read pointer is transferred to the output data bus at the rising edge of RCLK along with active low DVal. If the outputs are disabled but the reads enabled, the outputs are in high impedance state, but internally the read pointer is incremented.

During write operation, the number of writes performed is always a even number (i.e., minimum write burst length is two and number of writes always a multiple of two). Whereas during read operation, the number of reads performed can be even or odd (i.e., minimum read burst length is one).

The MARK signal is used to ‘mark’ the location from which data is retransmitted when requested.

Reset Logic

The FIFO can be reset in two ways: Master Reset ($\overline{MRS}$) and Partial Reset ($\overline{PRS}$). The $\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. It also resets the configuration registers to their default values. The word size is configured through pins; values of the three PORTSZ pins are latched during $\overline{MRS}$. A Master Reset is required after power-up before accessing the FIFO. The $\overline{PRS}$ resets only the read and write pointer to the first location and does not affect the programmed configuration registers.

Flag Operation

This device provides five flag pins to indicate the condition of the FIFO contents.

Full Flag

The Full Flag ($\overline{FF}$) goes LOW when the device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK. The worst case assertion latency for Full Flag is four. As the user cannot know that the FIFO is full for four clock cycles, it is possible that user continues writing data during this time. In this case, the four data word written will be stored to prevent data loss and these words have to be read back in order for full flag to get de-asserted.The minimum number of reads required to de-assert full-flag is two and the maximum number of reads required to de-assert full flag is six.

Half-Full Flag

The Half-Full ($\overline{HF}$) flag goes LOW when half of the memory array is written. The assertion of HF is synchronized to WCLK. The assertion and de-assertion of Half-Full flag with associated latencies is explained in Table 12

Empty Flag

The Empty Flag ($\overline{EF}$) goes LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, that is, it is exclusively updated by each rising edge of RCLK. The assertion and de-assertion of empty flag with associated latencies is explained in Table 12

Programmable Almost-Empty and Almost-Full Flags

The CYF0072V includes programmable Almost-Empty and Almost-Full flags. Each flag is programmed (see Programming Flag Offsets and Configuration Registers on page 8) a specific distance from the corresponding boundary flags (Empty or Full). (offset can range from 16 to 1024) When the FIFO contains the number of words (or fewer) for which the flags are programmed, the $\overline{PAF}$ or $\overline{PAE}$ is asserted, signifying that the FIFO is either almost-full or almost-empty. The $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock. The assertion and de-assertion of empty flag with associated latencies is explained in Table 12

Retransmit from Mark Operation

The retransmit feature is useful for transferring packets of data repeatedly. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit feature is used when the number of writes after MARK is equal to or less than the depth of the FIFO and at least one word has been read since the last reset cycle. A HIGH pulse on RT resets the internal read pointer to a physical location of the FIFO that is marked by the user (using the MARK pin). With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to FIFO after activation of RT are also transmitted. The full depth of the FIFO can be repeatedly retransmitted.

To mark a location, the Mark pin is asserted when reading that particular location.

Flow-through Mailbox Register

This feature transfers data from input to output directly by bypassing the FIFO sequence. When MB signal is asserted the data present in D[35:0] will be available at Q[35:0] after two WCLK cycles. Normal read and write operations are not allowed during flow-through mailbox operation. Before starting Flow-through mailbox operation FIFO read should be completed to make data valid $\overline{DVal}$ high in order to avoid data loss from FIFO. The width of flow-through mailbox register always corresponds to port size.

Selecting Word Sizes

The word sizes are configured based on the logic levels on the PORTSZ pins during the master reset (MRS) cycle only (latched on low to high edge). The port size cannot be changed during normal mode of operation and these pins are ignored. Table 1. explains the pins of D[35:0] and Q[35:0] that will have valid data in modes where the word size is less than ×36. If word size is less than ×36, the unused output pins are tri-stated by the device and unused input pins will be ignored by the internal logic. The pins with valid data input D[N:0] and output Q[N:0] is given in Table 1.

Data Valid Signal (DVal)

Data valid (DVal) is an active low signal, synchronized to RCLK and is provided for easy capture of output data to the user. When a read operation is performed, the DVal signal goes low along with output data. This helps user to capture the data without keeping track of REN to data output latency. This signal also helps when write and read operations are performed continuously at different frequencies by indicating when valid data is available at the output port Q[35:0].

Power Up

The device becomes functional after VCC1, VCC2, VCCIO, and Vref attain minimum stable voltage required as given in Recommended DC Operating Conditions on page 13. The device can be accessed t_{PU} time after these supplies attain the minimum required level (see Switching Characteristics on page 15). There is no particular power sequencing required for the device.

Table 1. Word Size Selection

PORTSZ[2:0]	Word Size	Active Input Data Pins D[X:0]	Active Output Data Pins Q[X:0]
000	×9	D[8:0]	Q[8:0]
001	×12	D[11:0]	Q[11:0]
010	×16	D[15:0]	Q[15:0]
011	×18	D[17:0]	Q[17:0]
100	×20	D[19:0]	Q[19:0]
101	×24	D[23:0]	Q[23:0]
110	×32	D[31:0]	Q[31:0]
111	×36	D[35:0]	Q[35:0]

Write Mask and Read Skip Operation

As mentioned in Architecture on page 7, enabling writes but disabling the inputs (IE HIGH) increments the write pointer without doing any write operations or altering the contents of the location.

This feature is called Write Mask and allows user to move the write pointer without actually writing to the locations. This “write masking” ability is useful in some video applications such as Picture In Picture (PIP).

Similarly, during a read operation, if the outputs are disabled by having the OE high, the read data does not appear on the output bus; however, the read pointer is incremented.

Programming Flag Offsets and Configuration Registers

The CYF0072V has ten 8-bit user configurable registers. These registers contain the almost-full offset (M) and almost-empty (N) values which decide when the PAF and PAE flags are asserted.

These registers can be programmed into the FIFO in one of two ways: using either the serial or parallel loading method. The loading method is selected using the SPI_SEN (Serial Enable) pin. A low on the SPI_SEN selects the serial method for writing into the registers. For serial programming, there is a separate SCLK and a Serial Input (SI). In parallel mode, a low on the load (LD) pin causes the write and read operation to these registers. The write and read operation happens from the first location (0x1) to the last location (0xA) in a sequence. If LD is high, the writes occur to the FIFO.

In addition to loading register values into the FIFO, it is also possible to read the current register values. Register values can be read through the parallel output port regardless of the programming mode selected (serial or parallel). Register values cannot be read serially. The registers may be programmed (and reprogrammed) any time after master reset, regardless of whether serial or parallel programming is selected.

See Table 3 on page 9 and Table 4 on page 10 for access to configuration registers in serial and parallel modes.

In parallel mode, the read and write operations loop back when the maximum address location of the configuration registers is reached. Simultaneous read and write operations should be avoided on the configuration registers. Any change in configuration registers will take effect after eight write clock cycles(WCLK) cycles.

Table 2. Configuration Registers

ADDR	Configuration Register	Default	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
0x1	Reserved	0x00	X	X	X	X	X	X	X	X
0x2	Reserved	0x00	X	X	X	X	X	X	X	X
0x3	Reserved	0x00	X	X	X	X	X	X	X	X
0x4	Almost-Empty Flag generation address - (LSB) (N)	0x7F	D7	D6	D5	D4	D3	D2	D1	D0
0x5	Almost-Empty Flag generation address - (MSB) (N)	0x00	X	X	X	X	X	X	D9	D8
0x6	Reserved	0x00	X	X	X	X	X	X	X	X
0x7	Almost-Full Flag generation address - (LSB) (M)	0x7F	D7	D6	D5	D4	D3	D2	D1	D0
0x8	Almost-Full Flag generation address - (MSB) (M)	0x00	X	X	X	X	X	X	D9	D8
0x9	Reserved	0x00	X	X	X	X	X	X	X	X
0xA	Fast CLK Bit Register	1XXXXXXXb	Fast CLK bit	X	X	X	X	X	X	X

Table 3. Writing and Reading Configuration Registers in Parallel Mode

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SPI_SCLK	Operation
1	0	0	1	↑ First rising edge because both $\overline{\text{LD}}$ and $\overline{\text{REN}}$ are low	X	X	Parallel write to first register
1	0	0	1	↑ Second rising edge	X	X	Parallel write to second register
1	0	0	1	↑ Third rising edge	X	X	Parallel write to third register
1	0	0	1	↑ Fourth rising edge	X	X	Parallel write to fourth register
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	↑ Tenth rising edge	X	X	Parallel write to tenth register
1	0	0	1	↑ Eleventh rising edge	X	X	Parallel write to first register (roll back)
1	0	1	0	X	↑ First rising edge since both $\overline{\text{LD}}$ and $\overline{\text{REN}}$ are low	X	Parallel read from first register
1	0	1	0	X	↑ Second rising edge	X	Parallel read from second register
1	0	1	0	X	↑ Third rising edge	X	Parallel read from third register
1	0	1	0	X	↑ Fourth rising edge	X	Parallel read from fourth register
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	↑ Tenth rising edge	X	Parallel read from tenth register

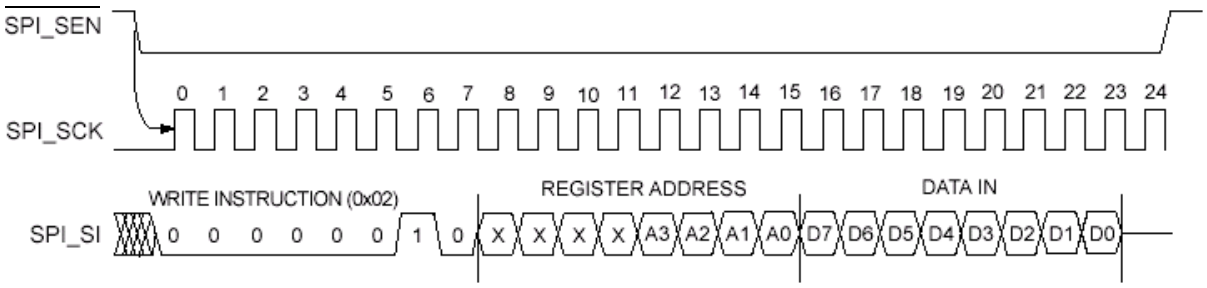
Table 3. Writing and Reading Configuration Registers in Parallel Mode (continued)

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SPI_SCLK	Operation
1	0	1	0	X	↑ Eleventh rising edge	X	Parallel read from first register (roll back)
1	X	1	1	X	X	X	No operation
X	1	0	X	↑ Rising edge	X	X	Write to FIFO memory
X	1	X	0	X	↑ Rising edge	X	Read from FIFO memory
0	0	X	1	X	X	X	Illegal operation

Table 4. Writing into Configuration Registers in Serial Mode

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SCLK	Operation
0	1	X	X	X	X	↑ Rising edge	Each rising of the SCLK clocks in one bit from the SI (Serial In). Any of the 10 registers can be addressed and written to, following the SPI protocol.
X	1	0	X	↑ Rising edge	X	X	Parallel write to FIFO memory.
X	1	X	0	X	↑ Rising edge	X	Parallel read from FIFO memory.
1	0	1	1	X	X	X	This corresponds to parallel mode (refer to Table 3).

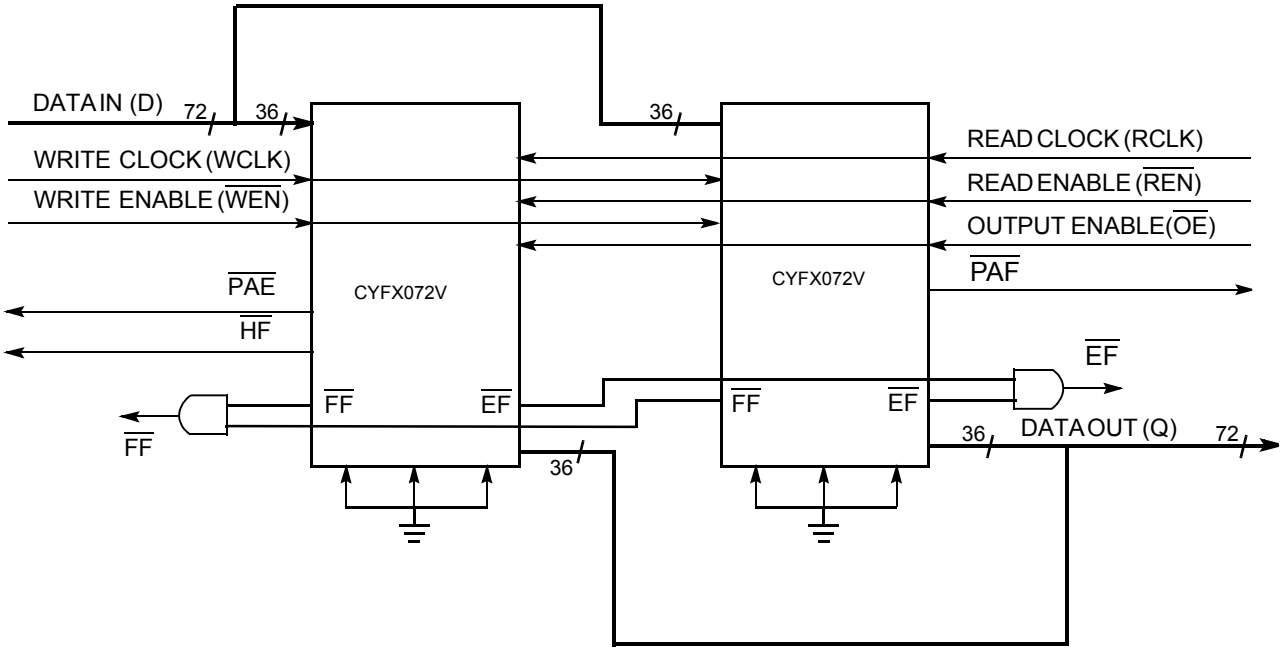
Figure 2. Serial WRITE to Configuration Register



Width Expansion Configuration

The width of CYFX072V can be expanded to provide word widths greater than 36 bits. During width expansion mode, all control line inputs are common and all flags are available. Empty (Full) flags are created by ANDing the Empty (Full) flags of every FIFO; the PAE and PAF flags can be detected from any one device. This technique avoids reading data from or writing data to the FIFO that is “staggered” by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 3 on page 11 demonstrates an example of 72 bit-word width by using two 36-bit word CYFX072Vs.

Figure 3. Using Two CYFX072V for Width Expansion



Memory Organization for Different Port Sizes

The 72-Mbit memory has different organization for different port sizes. Table 5 shows the depth of the FIFO for all port sizes.

Note that for all port sizes, four to eight locations are not available for writing the data and are used to safeguard against false synchronization of empty and full flags.

Table 5. Word Size Selection

PORTSZ[2:0]	Word Size	FIFO Depth	Memory Size
000	x9	8 Meg	72 Mbit
001	x12	4 Meg	48 Mbit
010	x16	4 Meg	64 Mbit
011	x18	4 Meg	72 Mbit
100	x20	2 Meg	40 Mbit
101	x24	2 Meg	48 Mbit
110	x32	2 Meg	64 Mbit
111	x36	2 Meg	72 Mbit

Read/Write Clock Requirements

The read and write clocks must satisfy the following requirements:

- Both read (RCLK) and write (WCLK) clocks should be free-running.
- The clock frequency for both clocks should be between the minimum and maximum range given in Table 10 on page 13.
- The WCLK to RCLK ratio should be in the range of 0.5 to 2.

For proper FIFO operation, the device must determine which of the input clocks – RCLK or WCLK – is faster. This is evaluated by using counters after the MRS cycle. The device uses two 10-bit counters inside (one running on RCLK and other on WCLK), which count 1,024 cycles of read and write clock after MRS. The clock of the counter which reaches its terminal count first is used as master clock inside the FIFO.

When there is change in the relative frequency of RCLK and WCLK during normal operation of FIFO, user can specify it by using “Fast CLK bit” in the configuration register (0xA).

“1” - indicates f_{req} (WCLK) > f_{req} (RCLK)

“0” - indicates f_{req} (WCLK) < f_{req} (RCLK)

The result of counter evaluated frequency is available in this register bit. User can override the counter evaluated frequency for faster clock by changing this bit.

Whenever there is a change in this bit value, user must wait t_{PLL} time before issuing the next read or write to FIFO.

JTAG Operation

CYFX072V has two devices connected internally in a JTAG chain as shown in Figure 4

Figure 4. Device Connection in a JTAG Chain

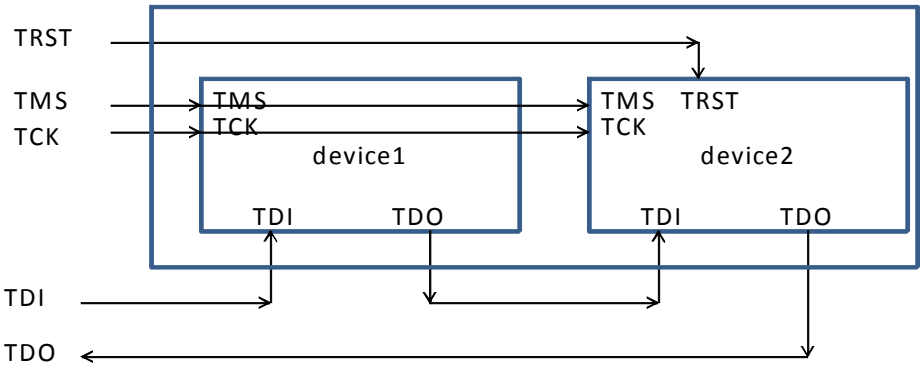


Table 6 shows the IR register length and device ID

Table 6. JTAG IDCODES

	IR Register Length	Device ID (HEX)	Bypass Register Length
Device-1	3	"Ignore"	1
Device-2	8	1E3261CF	1

Table 7. JTAG Instructions for Device-1

Device-1	Opcode (Binary)
BYPASS	111

Table 8. JTAG Instructions for Device-2

Device-2	Opcode (HEX)
EXTEST	00
HIGHZ	07
SAMPLE/PRELOAD	01
BYPASS	FF
IDCODE	0F

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature (without bias) ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Core supply voltage 1 (VCC1) to ground potential.....–0.3 V to 2.5 V

Core supply voltage 2 (VCC2) to ground potential.....–0.3 V to 1.65 V

Latch up current .....>100mA

I/O port supply voltage (VCCIO) .....–0.3 V to 3.7 V

Voltage applied to I/O pins .....–0.3 V to 3.75 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL–STD–883, Method 3015)

Operating Range

Range	Ambient Temperature
Industrial	–40 °C to +85 °C

Table 9. Recommended DC Operating Conditions

Parameter	Description		Min	Typ	Max	Unit
VCC1	Core supply voltage 1		1.70	1.80	1.90	V
VCC2	Core supply voltage 2		1.425	1.5	1.575	V
Vref	Reference voltage (irrespective of I/O standard used)		0.7	0.75	0.8	V
VCCIO	I/O supply voltage, read and write banks.	LVCMOS33	3.00	3.30	3.60	V
		LVCMOS18	1.70	1.8	1.90	V

Table 10. Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{cc}	Active current	VCC1=$VCC1_{MAX}$,	–	–	300	mA
		VCC2=$VCC2_{MAX}$, All I/O switching, 133 MHz)	–	–	600	mA
		VCCIO = $VCCIO_{MAX}$ (All outputs disabled)	–	–	100	mA
I_I	Input pin leakage current	V_{IN} = $VCCIO_{max}$ to 0 V	–15	–	15	µA
I_{OZ}	I/O pin leakage current	V_O = $VCCIO_{max}$ to 0 V	–15	–	15	µA
C_P	Capacitance for TMS and TCK	–	–	–	16	pF
C_{PIO}	Capacitance for all other pins except TMS and TCK	–	–	–	8	pF

Table 11. I/O Characteristics

(Over the operating range)

I/O standard	Nominal I/O supply voltage	Input Voltage (V)		Output voltage (V)		Output Current (mA)	
		V_{IL}(max)	V_{IH}(min)	V_{OL}(max)	V_{OH}(min)	I_{OL}(max)	I_{OH}(max)
LVCMOS33	3.3 V	0.80	2.20	0.45	2.40	24	24
LVCMOS18	1.8 V	30% VCCIO	65% VCCIO	0.45	VCCIO – 0.45	16	16

Table 12. Latency Table

Latency Parameter	Number of cycles	Detail
$L_{\overline{FF}\_ASSERT}$	Min=0 Max=4	Last data write to $\overline{FF}$ going low
$L_{\overline{EF}\_ASSERT}$	0	Last data read to $\overline{EF}$ going low
$L_{\overline{PRS}\_TO\_ACTIVE}$	1	$\overline{PRS}$ to normal operation
$L_{MAILBOX}$	2	Latency from write port to read port when MB = 1 (wrt WCLK)
$L_{\overline{REN}\_TO\_DATA}$	4	Latency when $\overline{REN}$ is asserted low to first data output from FIFO
$L_{\overline{REN}\_TO\_CONFIG}$	4	Latency when $\overline{REN}$ is asserted along with $\overline{LD}$ to first data read from configuration registers
$L_{\overline{WEN}\_TO\_\overline{PAE}\_HI}$	5	Write to $\overline{PAE}$ going low
$L_{\overline{WEN}\_TO\_\overline{PAF}\_LO}$	5	Write to $\overline{PAF}$ going low
$L_{\overline{REN}\_TO\_\overline{PAE}\_LO}$	7	Read to $\overline{PAE}$ going high
$L_{\overline{REN}\_TO\_\overline{PAF}\_HI}$	7	Read to $\overline{PAF}$ going high
$L_{\overline{FF}\_DEASSERT}$	8	Read to $\overline{FF}$ going high
$L_{RT\_TO\_\overline{REN}}$	9	RT fifth cycle to $\overline{REN}$ going low for read
$L_{RT\_TO\_DATA}$	Min=19 Max=21	RT fifth cycle to valid data on Q[35:0]
L_{IN}	Min=25 Max=26	Initial latency for data read after FIFO goes empty during simultaneous read/write
$L_{\overline{EF}\_DEASSERT}$	Min=23 Max=24	Write to $\overline{EF}$ going high

Switching Characteristics

Parameter	Description		-133		Unit
			Min	Max	
t_{PU}	Power-up time after all supplies reach minimum value		–	2	ms
t_S	Clock cycle frequency	3.3 V LVCMOS	24	133	MHz
t_S	Clock cycle frequency	1.8 V LVCMOS	24	133	MHz
t_A	Data access time			10	ns
t_{CLK}	Clock cycle time		7.5	41.67	ns
t_{CLKH}	Clock high time		3.375	–	ns
t_{CLKL}	Clock low time		3.375	–	ns
t_{DS}	Data setup time		3	–	ns
t_{DH}	Data hold time		3	–	ns
t_{ENS}	Enable setup time		3	–	ns
t_{ENH}	Enable hold time		3	–	ns
t_{ENS_SI}	Setup time for SPI_SI and $\overline{\text{SPI\_SEN}}$ pins		5	–	ns
t_{ENH_SI}	Hold time for SPI_SI and $\overline{\text{SPI\_SEN}}$ pins		5	–	ns
t_{RATE_SPI}	Frequency of SCLK		–	25	MHz
t_{RS}	Reset pulse width		100	–	ns
t_{PZS}	Port size select to $\overline{\text{MRS}}$ seup time		25	–	ns
t_{PZH}	$\overline{\text{MRS}}$ to port size select hold time		25	–	ns
t_{RSF}	Reset to flag output time		–	50	ns
t_{PRT}	Retransmit pulse width		5	–	RCLK cycles
t_{OLZ}	Output enable to output in Low Z		4	15	ns
t_{OE}	Output enable to output valid		–	15	ns
t_{OHZ}	Output enable to output in High Z		–	15	ns
t_{WFF}	Write clock to $\overline{\text{FF}}$		–	8.5	ns
t_{REF}	Read clock to $\overline{\text{EF}}$		–	8.5	ns
t_{PAF}	Clock to $\overline{\text{PAF}}$ flag		–	17	ns
t_{PAE}	Clock to $\overline{\text{PAE}}$ flag		–	17	ns
t_{HF}	Clock to $\overline{\text{HF}}$ flag		–	17	ns
t_{PLL}	Time required to synchronize PLL		–	1024	cycles
t_{RATE_JTAG}	JTAG TCK cycle time		100	–	ns
t_{S_JTAG}	Setup time for JTAG TMS,TDI		5	–	ns
t_{H_JTAG}	Hold time for JTAG TMS,TDI		5	–	ns
t_{CO_JTAG}	JTAG TCK low to TDO valid		–	10	ns

Switching Waveforms

Figure 5. Write Cycle Timing

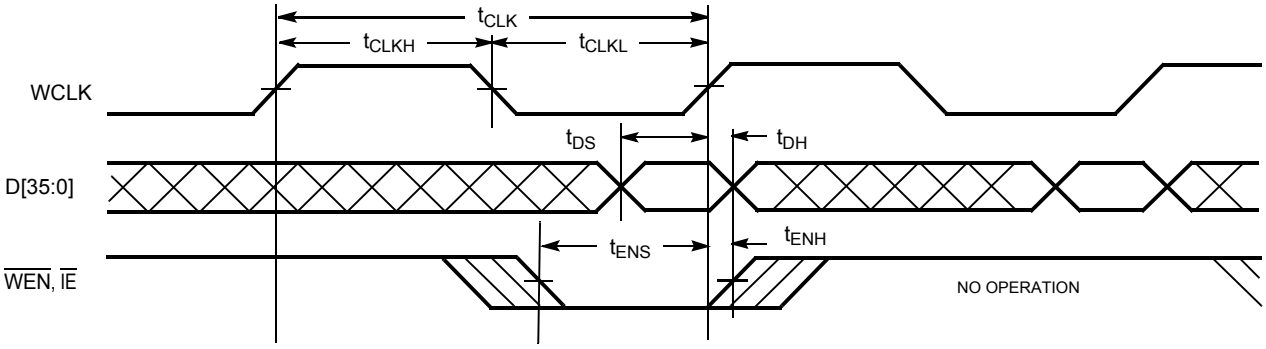
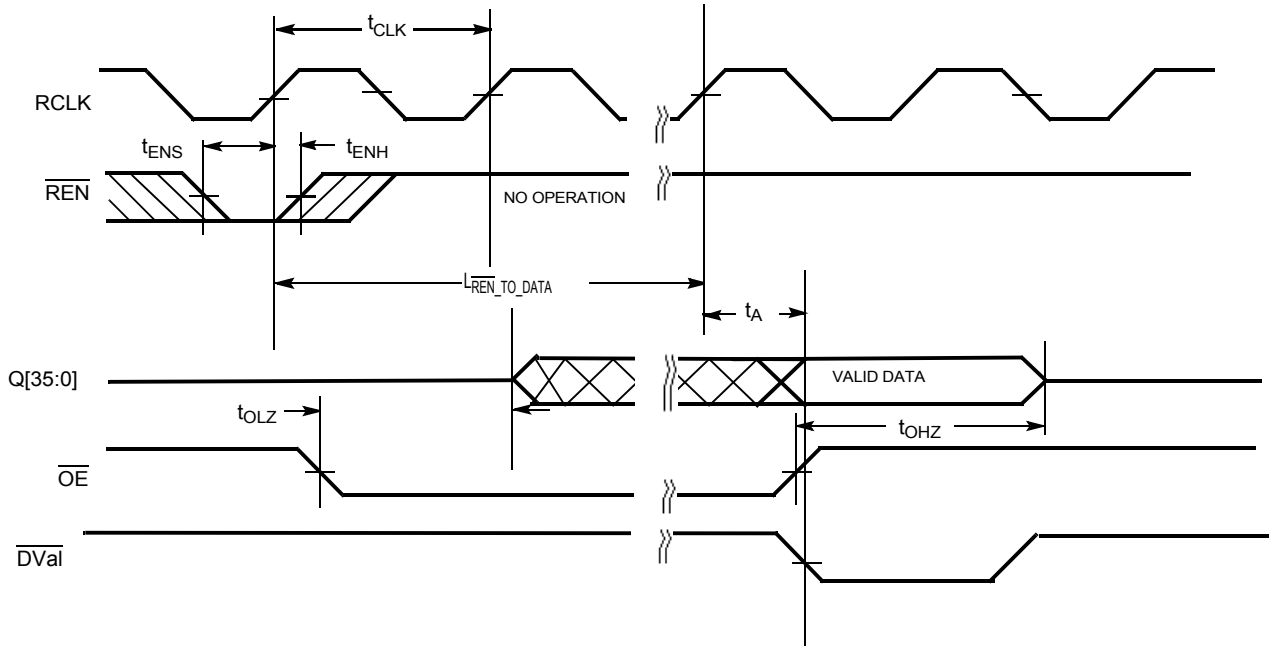


Figure 6. Read Cycle Timing



Switching Waveforms (continued)

Figure 7. Reset Timing

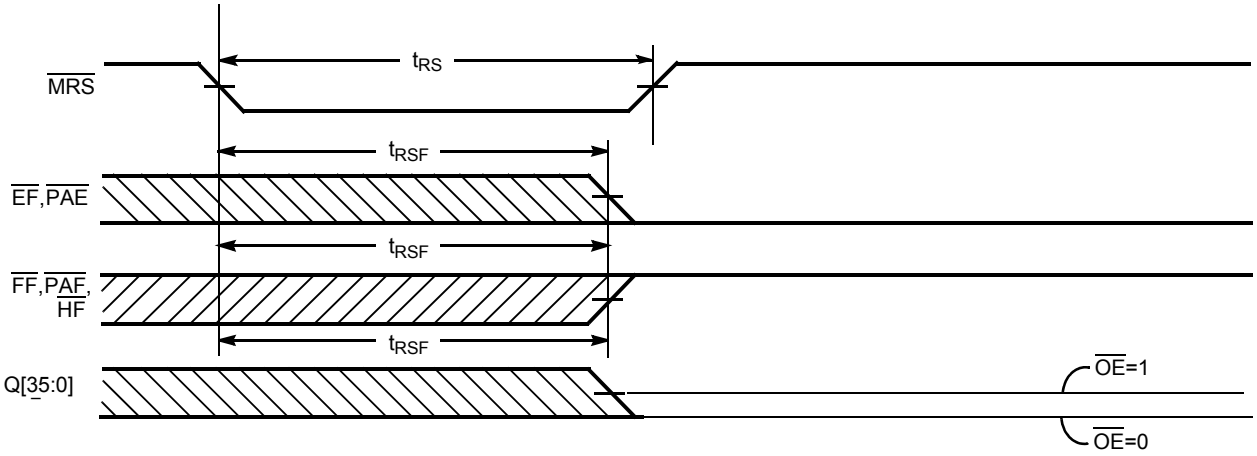
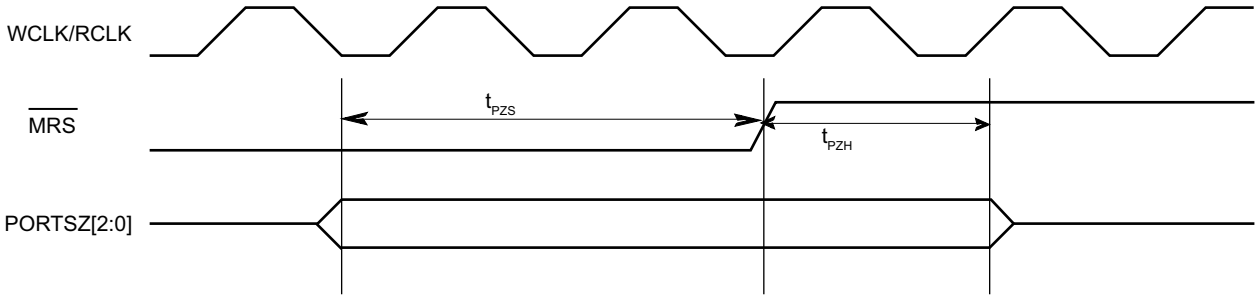


Figure 8. MRS to PORTSZ[2:0]



Switching Waveforms (continued)

Figure 9. Empty Flag Timing

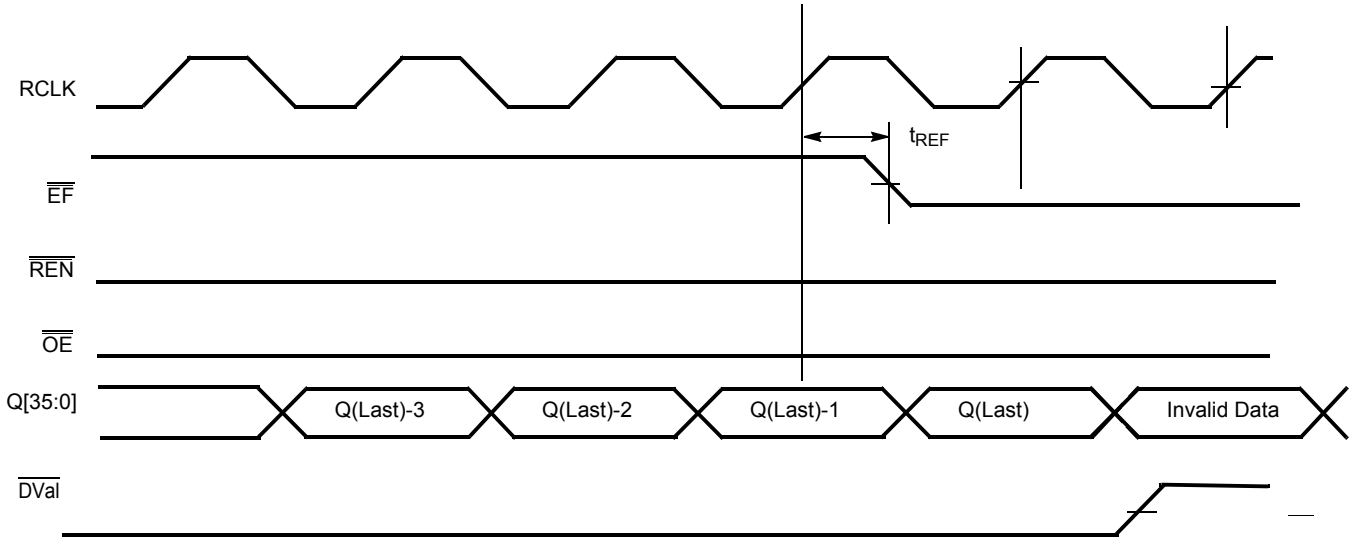


Figure 10. Full Flag Timing

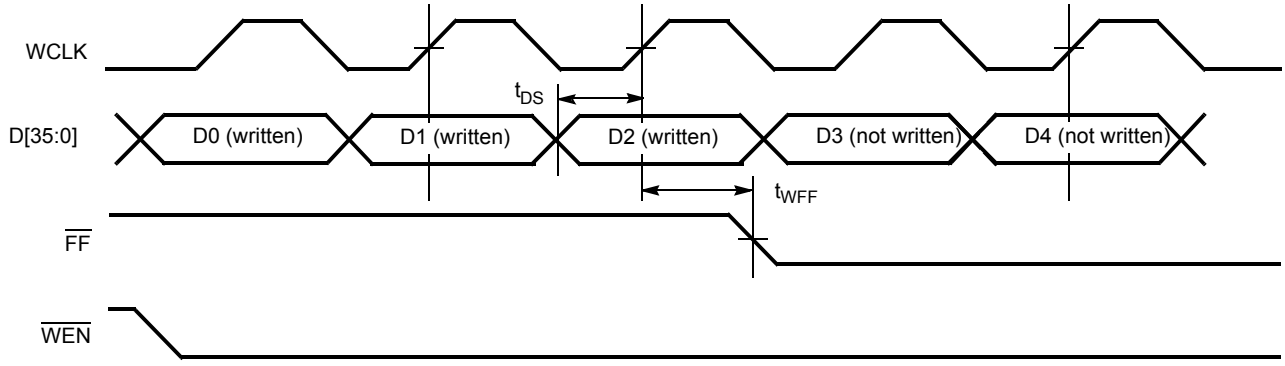


Figure 11. Initial Data Latency.

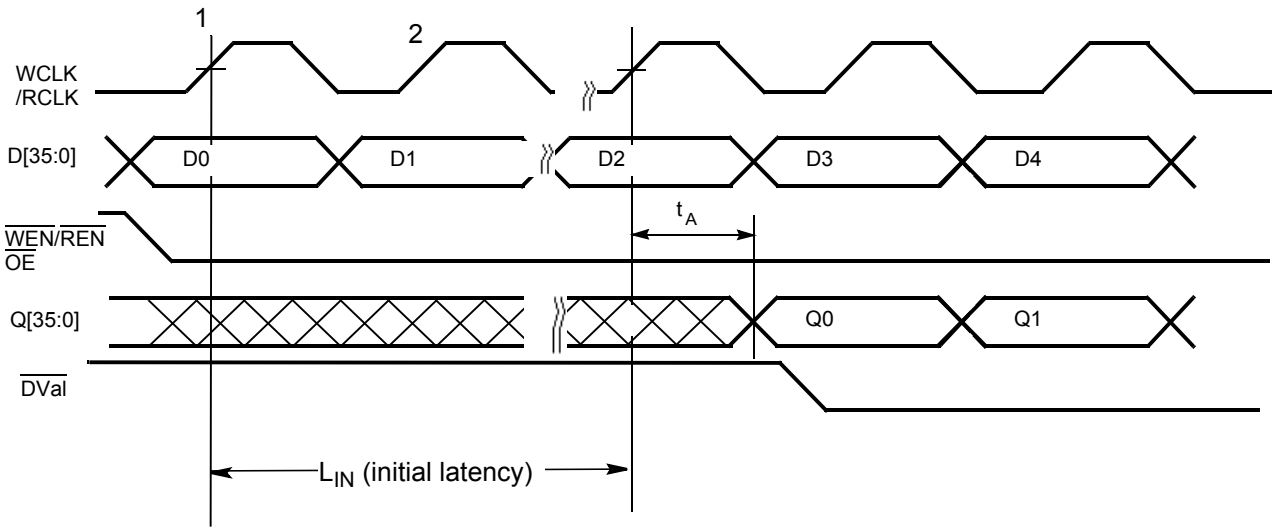


Figure 12. Flow-through Mailbox Operation

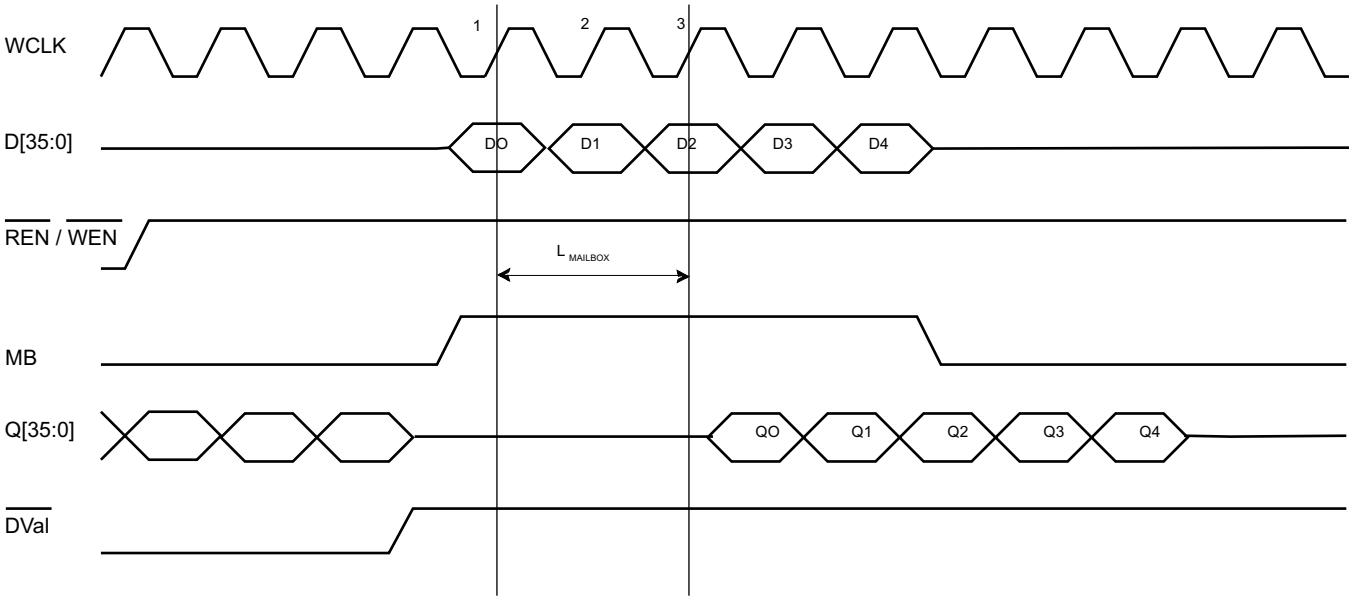


Figure 13. Configuration Register Write

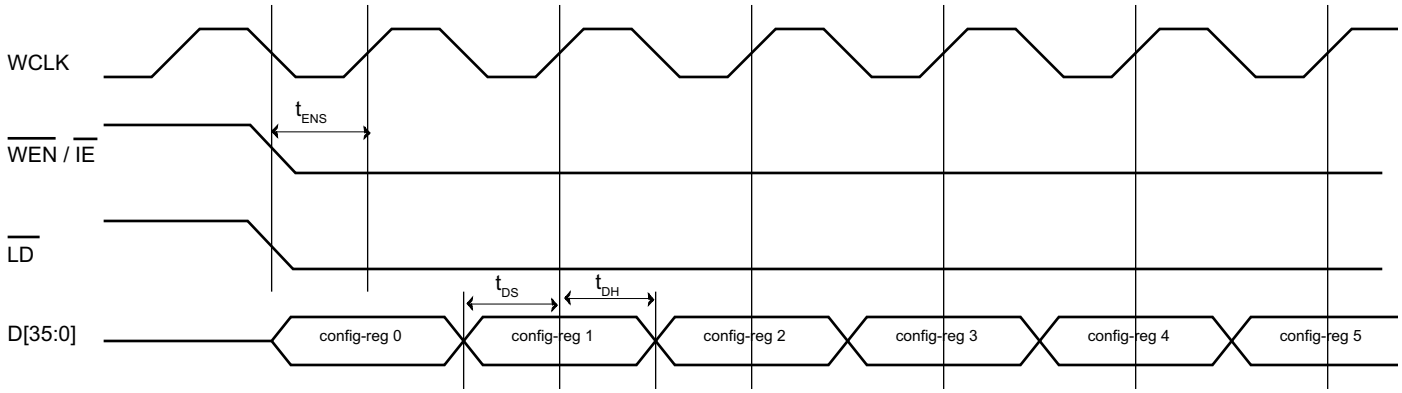


Figure 14. Configuration Register Read

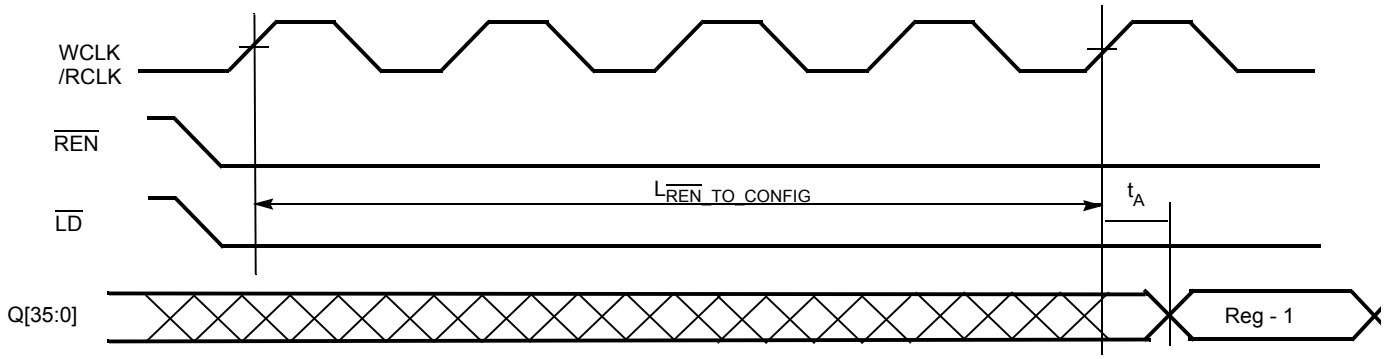


Figure 15. Empty Flag Deassertion

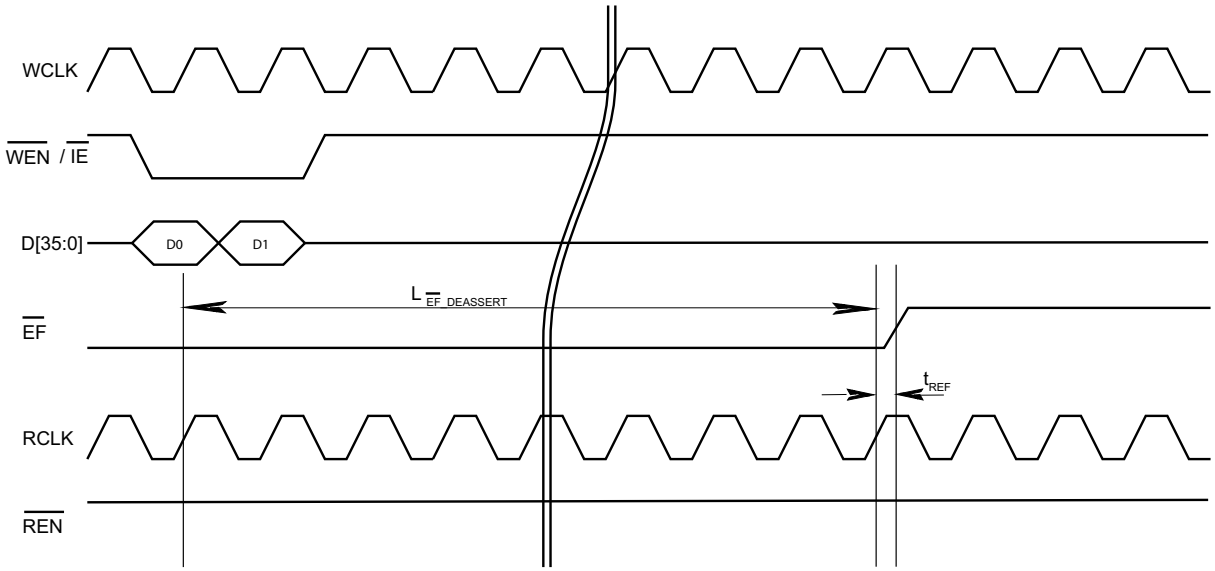


Figure 16. Empty Flag Assertion

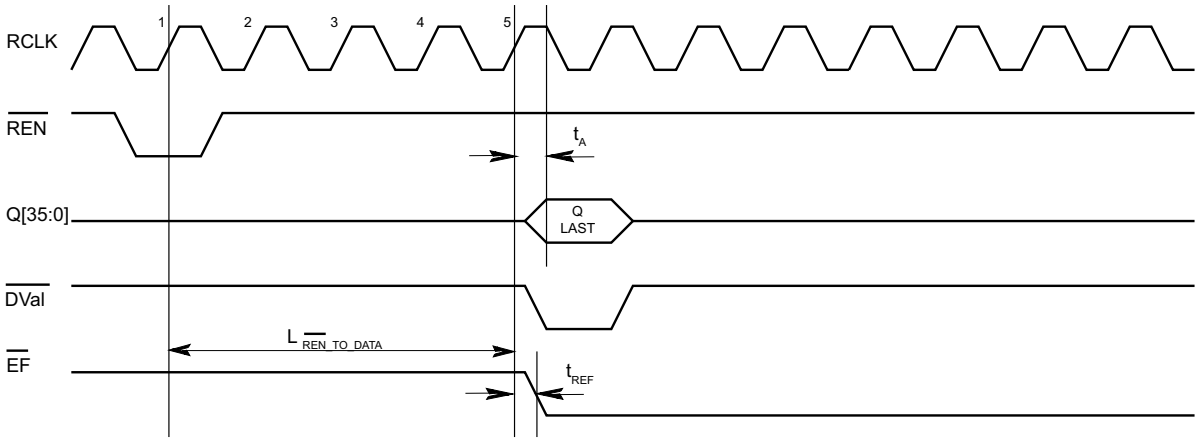


Figure 17. Full Flag Assertion

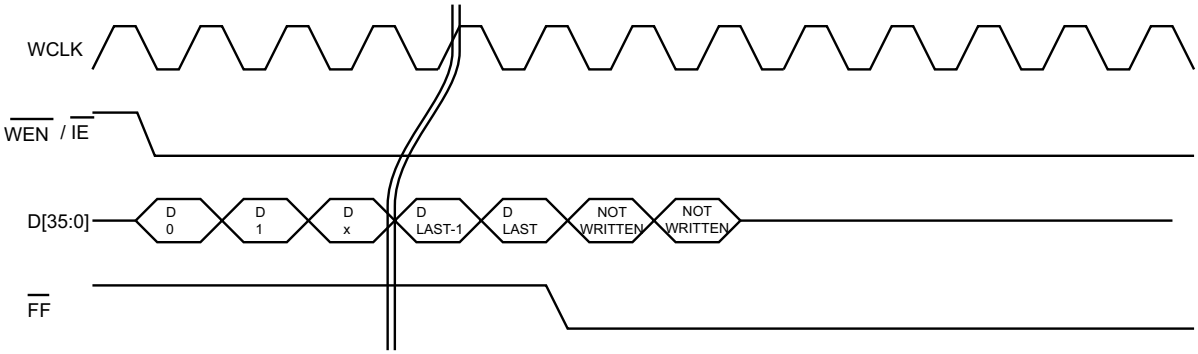


Figure 18. Full Flag Deassertion

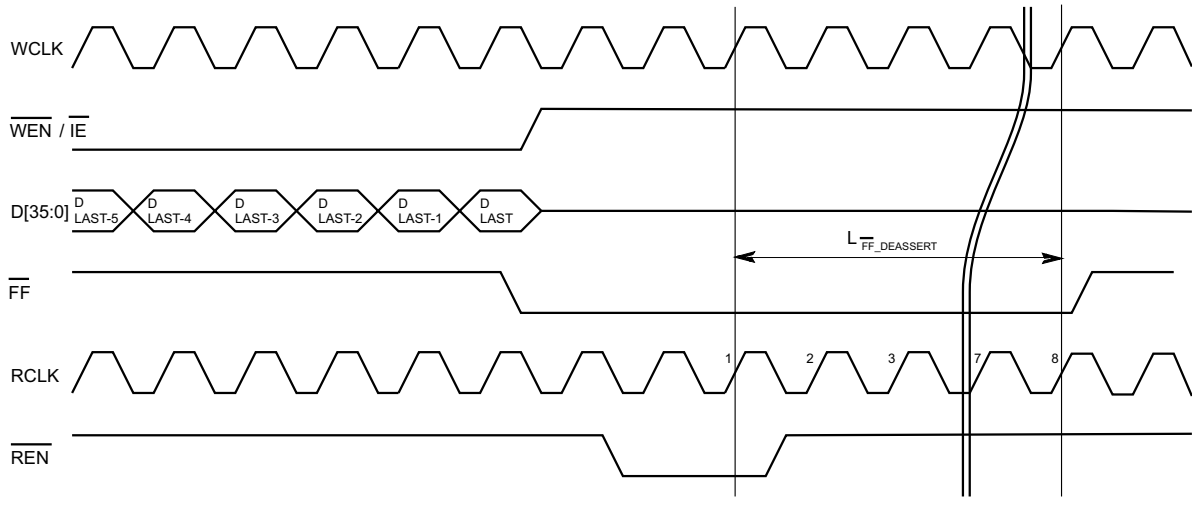


Figure 19. $\overline{\text{PAE}}$ Assertion and Deassertion

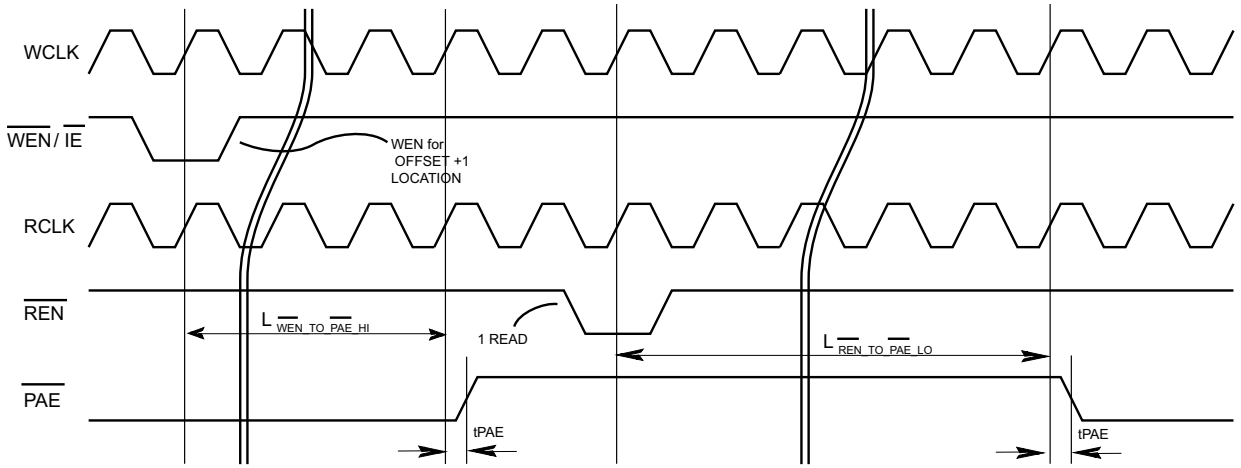


Figure 20. $\overline{\text{PAF}}$ Assertion and Deassertion

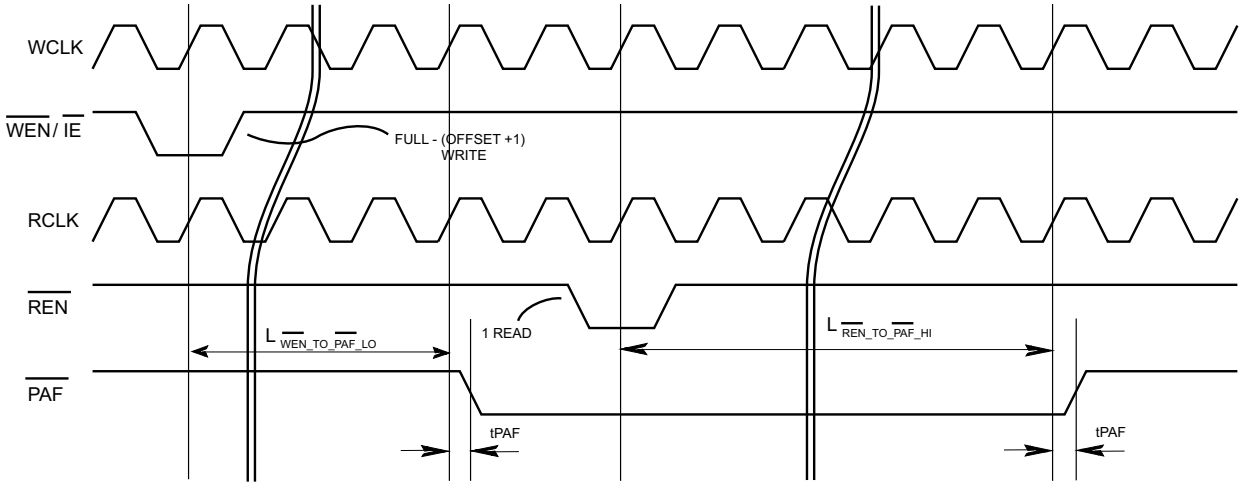


Figure 21. $\overline{\text{HF}}$ Assertion and Deassertion

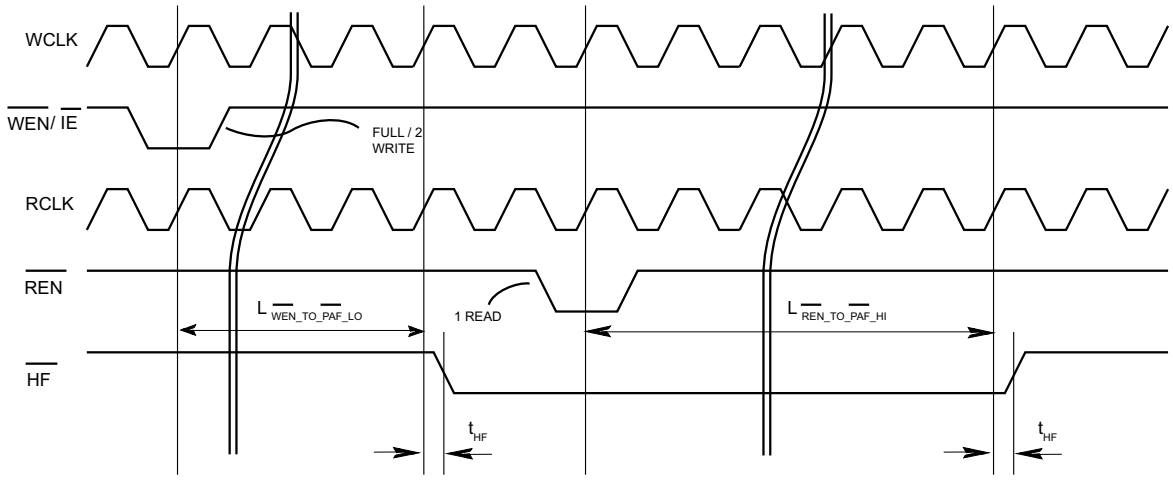


Figure 22. Mark

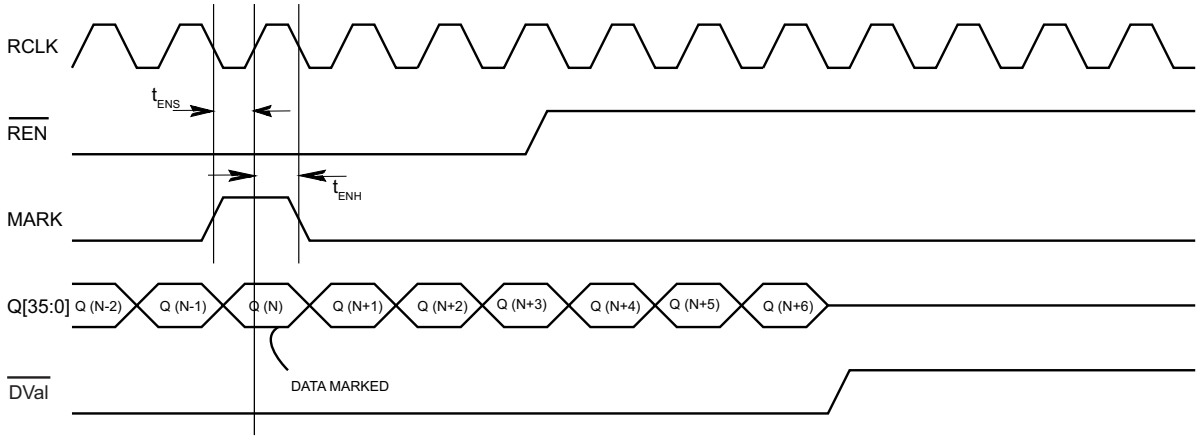
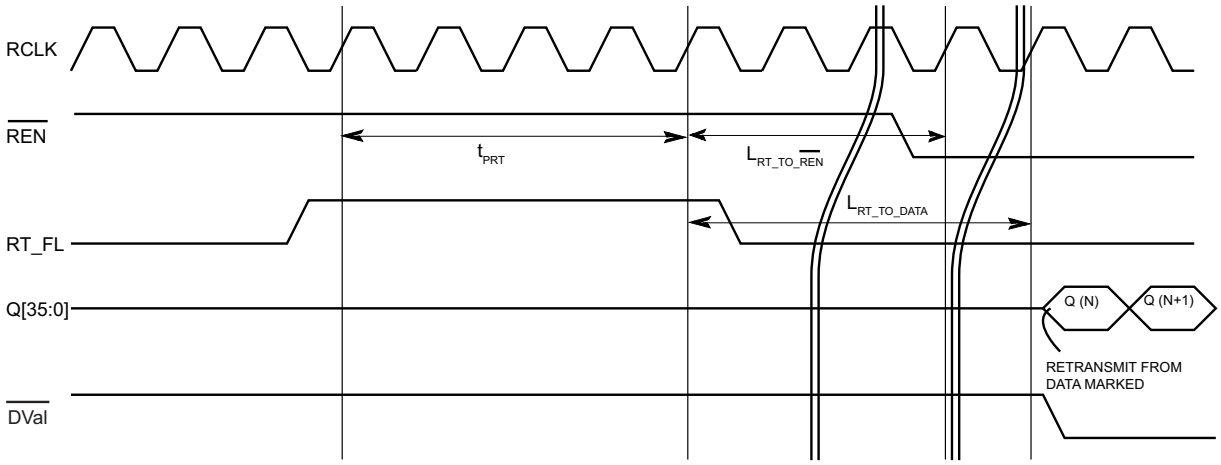


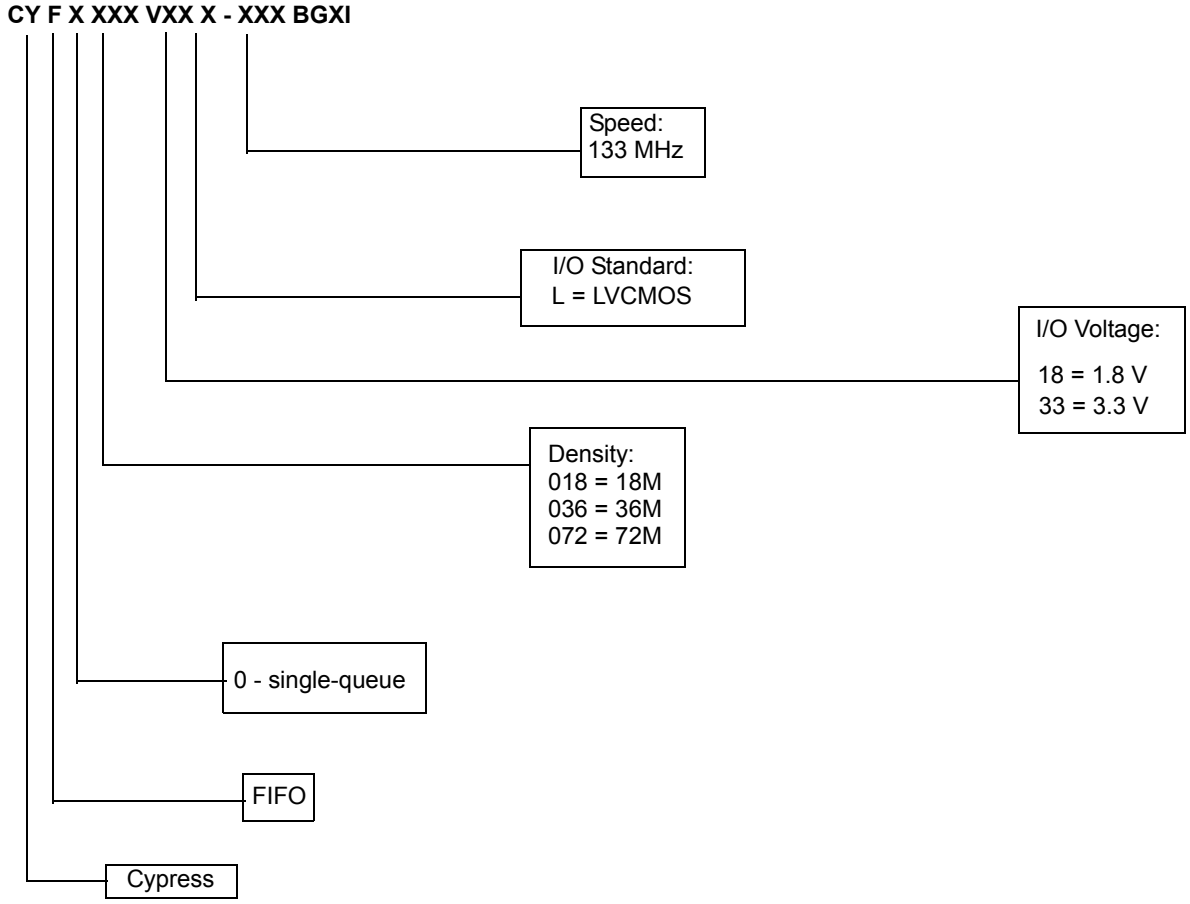
Figure 23. Retransmit



Ordering Information

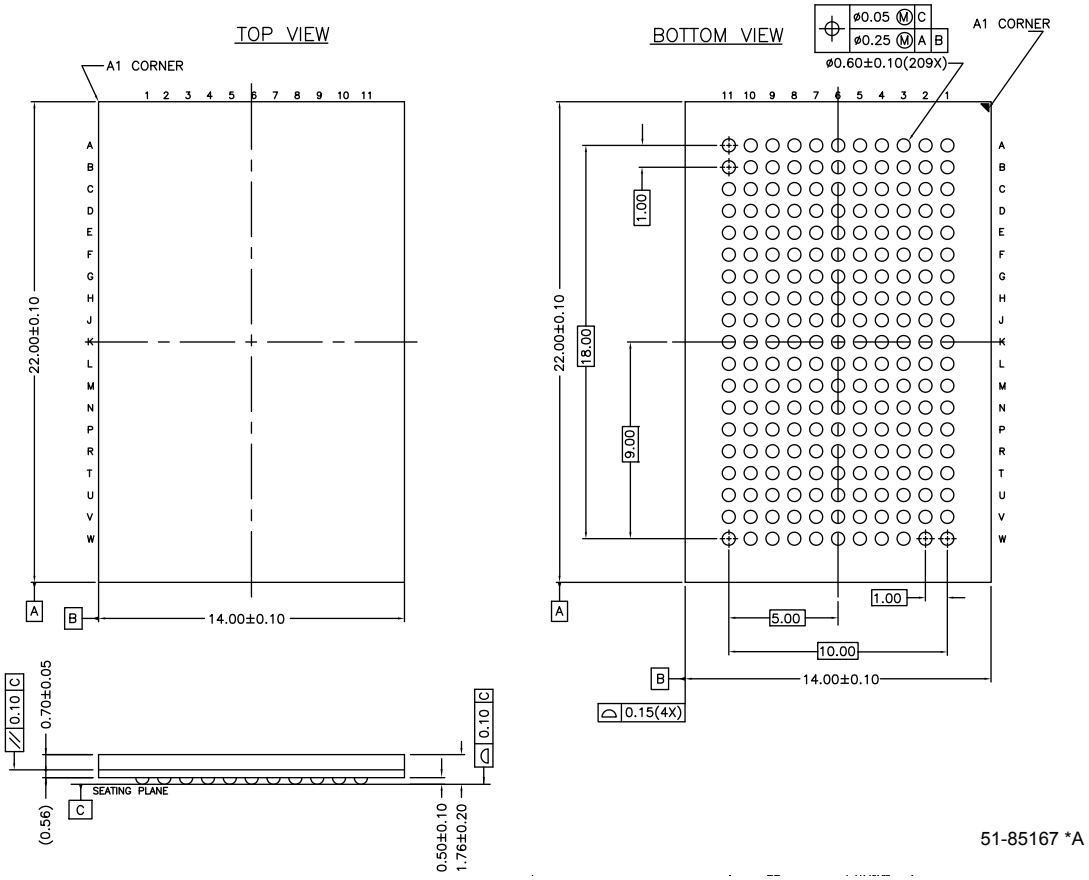
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CYF0018V33L-133BGXI	51-85167	209-ball fine-pitch ball grid array (FPBGA) (14 × 22 × 1.76 mm)	Industrial
	CYF0036V33L-133BGXI			
	CYF0072V33L-133BGXI			
	CYF0018V18L-133BGXI			
	CYF0036V18L-133BGXI			
	CYF0072V18L-133BGXI			

Ordering Code Definition



Package Diagram

Figure 24. 209-Ball FBGA (14 × 22 × 1.76 mm), 51-85167



Acronyms

Acronym	Description
$\overline{FF}$	Full flag
FIFO	First in first out
$\overline{HF}$	Half full
HSTL	High-speed transceiver logic
$\overline{IE}$	Input enable
I/O	Input/output
FPBGA	fine-pitch ball grid array
JTAG	Joint test action group
LVCMOS	Low voltage complementary metal oxide semiconductor
MB	Mailbox
$\overline{MRS}$	Master reset
$\overline{OE}$	Output enable
$\overline{PAF}$	Programmable almost-full
$\overline{PAE}$	Programmable almost-empty
$\overline{PRS}$	Partial reset
RCLK	Read clock
$\overline{REN}$	Read enable
RCLK	Read clock
SCLK	Serial clock
TDI	Test data in
TDO	Test data out
TCK	Test clock
TMS	Test mode select
WCLK	Write clock
$\overline{WEN}$	Write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microampere
mA	milliampere
ms	millisecond
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	pico Farad
V	volt
W	watt

Document History Page

Document Title: CYF0018V/CYF0036V/CYF0072V, 18/36/72 Mbit Programmable FIFOs Document Number: 001-53687				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2711566	VKN/PYRS	05/27/09	New data sheet
*A	2725088	NXR	06/26/2009	Included pinout, AC and DC specs, timing diagrams and package diagram
*B	2839536	NXR	01/28/2010	Changed Balls B5, D5, F6, K1, K2, K4, K8 and U2 from NC to DNU, Balls C5, C7, G6, H6, J6, L6, M6, N6, T5, T7 FROM NC to VCC1, Balls K9, K10, K11 From NC to VCCIOR Ball W9 from NC to Vref in pin configuration table Swapped Voltage range of $V_{SS}1$ and $V_{SS}2$ Updated ICC spec Removed T_{SKEW} parameter Added Ordering Information table Added Part Numbering Nomenclature. Changed title to CYF0018V/CYF0036V/CYF0072V/CYFX144VXXX, 18/36/72 Mbit Programmable FIFOs.
*C	2884377	HKV	02/25/2010	Post to external web.
*D	2963225	AJU/HPV	06/28/2010	Changed frequency of operation from 250 MHz to 150 MHz Removed Depth Expansion feature and changed associated pin functionality Removed Independent Port size selectability feature Added Data Valid (DVal) signal feature Updated Logic Block Diagram to reflect above changes. Pinout changes: Balls V5, V8, A7, B7, D7, and C6 renamed DNU Ball U1 changed from RXO to DVal Ball V2 changed from WXO/HF to HF Ball A5, A6, B6 changed from WPORTSZ to PORTSZ Ball A9 changed from RT/FL to RT Renamed pwr as POWER, gnd as GND Added Table 3 Table 6 – $\overline{LD}$ changed to '1' for serial writes Updated Electrical Characteristics and I/O Characteristics Switching Characteristics Table: Renamed tPC as tPU Min frequency changed from 110MH to 24MHz Changed t_{CLKH} and t_{CLKL} to 3.15 ns Changed All setup and hold times to 3 ns Changed t_{RSF} to 50 ns Removed t_{RSR} Changed All clock-to-flag timing to min=8 ns and max=14 ns T_{PLL} changed to 6 ms Changed all OE-related parameters to 15 ns Scaled ICC for reduced frequency Updated all waveforms Added the following tables: Word Size Selection, JTAG Operation, and Latency Table Added Acronyms.
*E	2994379	AJU	07/26/2010	Updated Ordering Information
*F	3101023	SIVS	12/03/2010	Added supply-wise current consumption data in Electrical Characteristics. Changed initial latency L_{IN} from 34 to 26 and added initial latency L_{IN} for 110 MHz part in Latency Table. Added 110 MHz part information in JTAG Operation Added details for the 110 MHz part in Switching Characteristics. Added details for the 110 MHz part in Ordering Information.
*G	3129722	HKV	01/06/2011	Post to external web.

Document Title: CYF0018V/CYF0036V/CYF0072V, 18/36/72 Mbit Programmable FIFOs
Document Number: 001-53687

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*H	3197271	SIVS	03/31/2011	Removed 144 Mbit parts from the data sheet Removed multi-queue information from data sheet Removed 2.5 V and 1.5 V options Removed HSTL I/II I/O standard Added clock ratio requirement between RCLK and WCLK Removed redundant Xs from part number to improve readability Removed tie to GND option on DNU pins in pin description Added information on Flag operations to add clarity Added explanation for flow-through mailbox operation Added details on active pins in various port sizes in Table 1. Added Configuration register write to normal operation latency details. Changed configuration register definitions and default values Changed number of unusable locations to four to eight Added JTAG related operation Added latch-up current parameter in maximum operating conditions. Removed 2.5 V and 1.5 V options from DC operating condition table 6. Removed 110 MHz part details and added Cpio parameter in table 7. Removed 2.5 V and 1.5 V options from Table 8. Added latency parameters in Table 9. changed Vol(max) value of LVCMOS33 in table11 Removed 110 MHz part detail from switching characteristics Added timing waveform to improve clarity. Modified ordering information and definition.

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