Am29C323

CMOS 32-Bit Parallel Multiplier

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- **32-Bit Three-Bus Architecture**
  - The device has two 32-bit input ports and one 32-bit output port with clocked multiply time of 100 ns
- **Speed Selects**
  - 80- and 55-ns speed-select parts
- **Single Clock with Register Enables**
  - The Am29C323 is controlled by one clock with individual register enables
- **Supports Multiprecision Multiplication**
  - The device has dual 32-bit registers on each data input port to perform multiprecision multiplication
- **Registers can be made transparent**
  - Input and output registers can be made transparent independently to eliminate unwanted pipeline delay
- **Supports Two's Complement, Unsigned or Mixed Numbers**
- **Data Integrity Through Master-Slave Mode and Parity Check/Generate**
  - Parity check/generate catches inter-device connection errors and master/slave mode provides complete function check

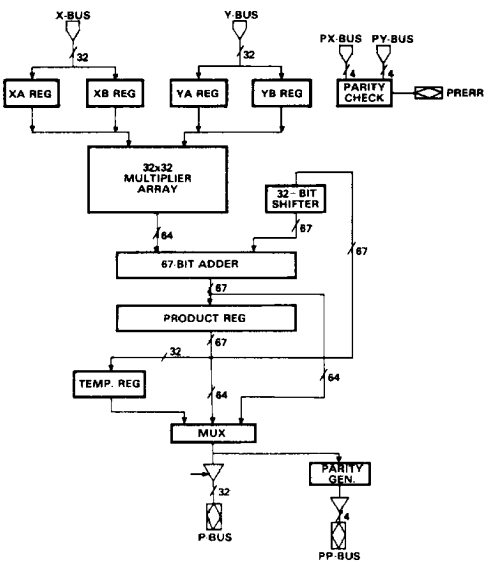
GENERAL DESCRIPTION

The Am29C323 is a high-speed 32 x 32-Bit CMOS Parallel Multiplier with 67-Bit Accumulator. The part is designed to maximize system level performance by providing a 32-bit three bus architecture and a single clock with register enables.

The Am29C323 further enhances system throughput by providing individual register feedthrough controls, byte parity checking on both input ports and generation on the output port, and dual input registers on each data input bus to support multiprecision multiplication. The Am29C323 can manage a wide variety of data types, including two's complement, unsigned, or mixed mode input formats. A 64 x 64-bit multiplication can be performed in seven clock cycles, including input and output. Additional features provided are a format adjust control allowing for standard output or left shifted output suitable for fractional two's complement arithmetic, rounding, and master/slave operation.

The Am29C323 is designed in low-power, high-speed CMOS with TTL-compatible I/O. The device is housed in a 169-lead pin-grid-array package.

SIMPLIFIED BLOCK DIAGRAM



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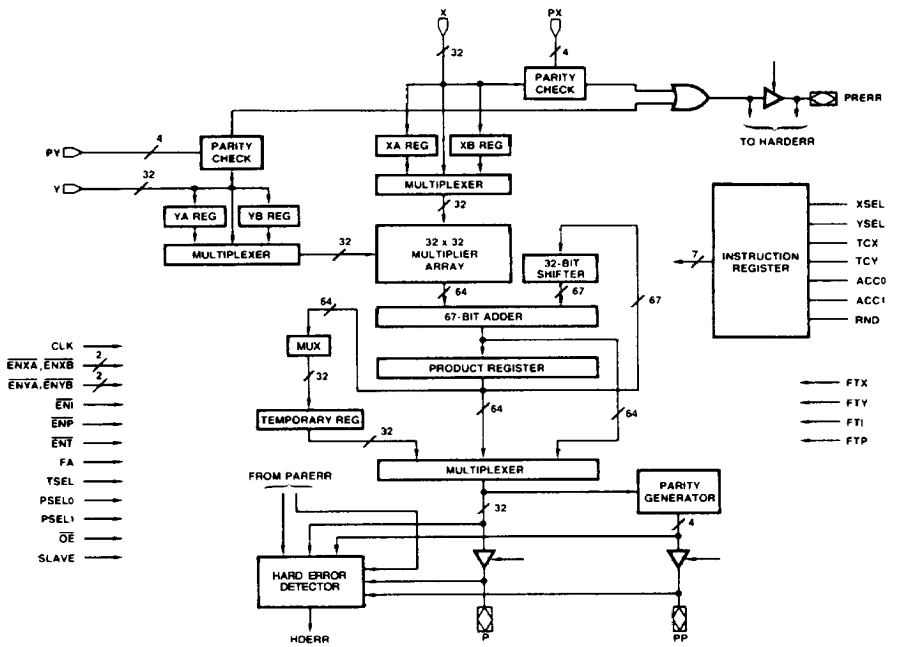
RELATED AMD PRODUCTS

Part No.	Description
Am29C01	CMOS 4-Bit Microprocessor Slice
Am29C10A	CMOS 12-Bit Sequencer
Am29C101	CMOS 16-Bit Microprocessor
Am29112	8-Bit Cascadable Microprogram Sequencer
Am29114	Real-Time Interrupt Controller
Am29C116	CMOS 16-Bit Microcontroller
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	64 x 18 Four-Port Dual Access Register File
Am29C334	CMOS 64 x 18 Four-Port Dual Access Register File
Am29337	16-Bit Bounds Checker
Am29338	32-Bit Byte Queue
Am29C516	CMOS 16 x 16 Multiplier
Am29C517	CMOS 16 x 16 Multiplier with Separate I/O

DETAILED BLOCK DIAGRAM



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CONNECTION DIAGRAM
169-Lead PGA
Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	PY_3	Y_{31}	Y_{30}	Y_{26}	Y_{24}	Y_{23}	Y_{20}	Y_{19}	Y_{15}	Y_{10}	Y_{11}	Y_7	Y_5	Y_3	GND	$\overline{ENYA}$	PX_3
2	GND	NC	Y_{29}	Y_{27}	PY_2	Y_{21}	Y_{18}	Y_{16}	PY_1	Y_{12}	Y_{09}	PY_0	Y_4	Y_2	Y_0	$\overline{ENYB}$	X_{31}
3	NC	PRERR	NC	Y_{28}	Y_{25}	Y_{22}	V_{CC}	Y_{17}	Y_{14}	Y_{13}	GND	Y_8	Y_6	Y_1	FTY	X_{30}	GND
4	V_{CC}	PP_3	NC	*											X_{29}	X_{28}	X_{27}
5	P_{30}	P_{31}	P_{29}												X_{26}	X_{24}	X_{25}
6	GND	P_{28}	P_{27}												PX_2	X_{23}	X_{22}
7	P_{25}	P_{26}	GND												V_{CC}	X_{19}	X_{21}
8	V_{CC}	P_{24}	PP_2												X_{18}	X_{17}	X_{20}
9	NC	NC	P_{23}												X_{15}	X_{16}	PX_1
10	GND	P_{22}	P_{21}												X_{14}	X_{13}	X_{11}
11	P_{19}	P_{20}	V_{CC}												GND	X_{10}	X_{12}
12	P_{16}	P_{18}	P_{17}												X_9	X_8	PX_0
13	V_{CC}	HDERR	FTP												X_7	X_5	X_6
14	NC	$\overline{ENP}$	NC												X_2	X_3	X_4
15	$\overline{ENT}$	$\overline{OE}$	SLAVE	P_{15}	P_{11}	P_{12}	GND	P_7	P_6	P_3	V_{CC}	P_1	FTI	TCY	FTX	X_1	X_0
16	PSEL1	FA	PP_1	P_{14}	P_{13}	P_9	GND	PP_0	P_5	P_4	V_{CC}	$\overline{EMI}$	CLK	ACC1	TCX	$\overline{ENXB}$	$\overline{ENXA}$
17	PSEL0	TSEL	GND	NC	V_{CC}	P_{10}	GND	P_8	GND	P_2	V_{CC}	P_0	V_{CC}	RND	ACC0	YSEL	XSEL

CD011030

*Pinout observed from pin side of package.
**Pin 169 for reference only.

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PIN DESIGNATIONS

(Sorted by Pin Number)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
1	**A1**	PY_3	75	**C9**	P_{23}	55	**J15**	P_6	117	**R10**	X_{14}
168	**A2**	GND	72	**C10**	P_{21}	51	**J16**	P_5	116	**R11**	GND
83	**A3**	NC	74	**C11**	V_{CC}	135	**J17**	GND	36	**R12**	X_9
81	**A4**	V_{CC}	153	**C12**	P_{17}	14	**K1**	Y_{10}	121	**R13**	X_7
80	**A5**	P_{30}	151	**C13**	FTP	13	**K2**	Y_{12}	40	**R14**	X_2
79	**A6**	GND	66	**C14**	NC	96	**K3**	Y_{13}	125	**R15**	FTX
160	**A7**	P_{25}	146	**C15**	SLAVE	50	**K15**	P_3	128	**R16**	TCX
77	**A8**	V_{CC}	145	**C16**	PP_1	134	**K16**	P_4	45	**R17**	ACC0
157	**A9**	NC	61	**C17**	GND	133	**K17**	P_2	105	**T1**	$\overline{ENYA}$
71	**A10**	GND	4	**D1**	Y_{26}	97	**L1**	Y_{11}	21	**T2**	$\overline{ENYB}$
154	**A11**	P_{19}	87	**D2**	Y_{27}	98	**L2**	Y_9	107	**T3**	X_{30}
69	**A12**	P_{16}	3	**D3**	Y_{28}	95	**L3**	GND	108	**T4**	X_{28}
68	**A13**	V_{CC}	62	**D15**	P_{15}	53	**L15**	V_{CC}	110	**T5**	X_{24}
67	**A14**	NC	144	**D16**	P_{14}	53	**L16**	V_{CC}	111	**T6**	X_{23}
65	**A15**	$\overline{ENT}$	60	**D17**	NC	53	**L17**	V_{CC}	113	**T7**	X_{19}
148	**A16**	PSEL1	5	**E1**	Y_{24}	16	**M1**	Y_7	114	**T8**	X_{17}
64	**A17**	PSEL0	89	**E2**	PY_2	99	**M2**	PY_0	31	**T9**	X_{16}
85	**B1**	Y_{31}	88	**E3**	Y_{25}	15	**M3**	Y_8	34	**T10**	X_{13}
84	**B2**	NC	142	**E15**	P_{11}	132	**M15**	P_1	119	**T11**	X_{10}
166	**B3**	PRERR	143	**E16**	P_{13}	47	**M16**	$\overline{ENI}$	120	**T12**	X_8
165	**B4**	PP_3	57	**E17**	V_{CC}	48	**M17**	P_0	122	**T13**	X_5
164	**B5**	P_{31}	6	**F1**	Y_{23}	17	**N1**	Y_5	123	**T14**	X_3
162	**B6**	P_{28}	7	**F2**	Y_{21}	101	**N2**	Y_4	124	**T15**	X_1
161	**B7**	P_{26}	90	**F3**	Y_{22}	100	**N3**	Y_6	42	**T16**	$\overline{ENXB}$
76	**B8**	P_{24}	59	**F15**	P_{12}	130	**N15**	FTI	127	**T17**	YSEL
73	**B9**	NC	141	**F16**	P_9	131	**N16**	CLK	22	**U1**	PX_3
156	**B10**	P_{22}	58	**F17**	P_{10}	49	**N17**	V_{CC}	106	**U2**	X_{31}
155	**B11**	P_{20}	91	**G1**	Y_{20}	18	**P1**	Y_3	23	**U3**	GND
70	**B12**	P_{18}	92	**G2**	Y_{18}	102	**P2**	Y_2	25	**U4**	X_{27}
152	**B13**	HDERR	11	**G3**	V_{CC}	19	**P3**	Y_1	26	**U5**	X_{25}
150	**B14**	$\overline{ENP}$	137	**G15**	GND	44	**P15**	TCY	28	**U6**	X_{22}
149	**B15**	$\overline{OE}$	137	**G16**	GND	129	**P16**	ACC1	112	**U7**	X_{21}
63	**B16**	FA	137	**G17**	GND	46	**P17**	RND	29	**U8**	X_{20}
147	**B17**	TSEL	8	**H1**	Y_{19}	20	**R1**	GND	115	**U9**	PX_1
2	**C1**	Y_{30}	93	**H2**	Y_{16}	103	**R2**	Y_0	35	**U10**	X_{11}
86	**C2**	Y_{29}	9	**H3**	Y_{17}	104	**R3**	FTY	118	**U11**	X_{12}
167	**C3**	NC	139	**H15**	P_7	24	**R4**	X_{29}	37	**U12**	PX_0
82	**C4**	NC	56	**H16**	PP_0	109	**R5**	X_{26}	38	**U13**	X_6
163	**C5**	P_{29}	140	**H17**	P_8	27	**R6**	PX_2	39	**U14**	X_4
78	**C6**	P_{27}	94	**J1**	Y_{15}	32	**R7**	V_{CC}	41	**U15**	X_0
158	**C7**	GND	10	**J2**	PY_1	30	**R8**	X_{18}	126	**U16**	$\overline{ENXA}$
159	**C8**	PP_2	12	**J3**	Y_{14}	33	**R9**	X_{15}	43	**U17**	XSEL

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PIN DESIGNATIONS

(Sorted by Pin Name)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
45	R17	ACC0	50	K15	P_3	89	E2	PY_2	110	T5	X_{24}
129	P16	ACC1	134	K16	P_4	1	A1	PY_3	26	U5	X_{25}
131	N16	CLK	51	J16	P_5	46	P17	RND	109	R5	X_{26}
47	M16	$\overline{ENI}$	55	J15	P_6	146	C15	SLAVE	25	U4	X_{27}
150	B14	$\overline{ENP}$	139	H15	P_7	128	R16	TCX	108	T4	X_{28}
65	A15	$\overline{ENT}$	140	H17	P_8	44	P15	TCY	24	R4	X_{29}
126	U16	$\overline{ENXA}$	141	F16	P_9	147	B17	TSEL	107	T3	X_{30}
42	T16	$\overline{ENXB}$	58	F17	P_{10}	68	A13	V_{CC}	106	U2	X_{31}
105	T1	$\overline{ENYA}$	142	E15	P_{11}	81	A4	V_{CC}	43	U17	XSEL
21	T2	$\overline{ENYB}$	59	F15	P_{12}	77	A8	V_{CC}	103	R2	Y_0
63	B16	FA	143	E16	P_{13}	74	C11	V_{CC}	19	P3	Y_1
130	N15	FTI	144	D16	P_{14}	57	E17	V_{CC}	102	P2	Y_2
151	C13	FTP	62	D15	P_{15}	11	G3	V_{CC}	18	P1	Y_3
125	R15	FTX	69	A12	P_{16}	53	L15	V_{CC}	101	N2	Y_4
104	R3	FTY	153	C12	P_{17}	53	L16	V_{CC}	17	N1	Y_5
71	A10	GND	70	B12	P_{18}	53	L17	V_{CC}	100	N3	Y_6
168	A2	GND	154	A11	P_{19}	49	N17	V_{CC}	16	M1	Y_7
79	A6	GND	155	B11	P_{20}	32	R7	V_{CC}	15	M3	Y_8
61	C17	GND	72	C10	P_{21}	41	U15	X_0	98	L2	Y_9
158	C7	GND	156	B10	P_{22}	124	T15	X_1	14	K1	Y_{10}
137	G15	GND	75	C9	P_{23}	40	R14	X_2	97	L1	Y_{11}
137	G16	GND	76	B8	P_{24}	123	T14	X_3	13	K2	Y_{12}
137	G17	GND	160	A7	P_{25}	39	U14	X_4	96	K3	Y_{13}
135	J17	GND	161	B7	P_{26}	122	T13	X_5	12	J3	Y_{14}
95	L3	GND	78	C6	P_{27}	38	U13	X_6	94	J1	Y_{15}
20	R1	GND	162	B6	P_{28}	121	R13	X_7	93	H2	Y_{16}
116	R11	GND	163	C5	P_{29}	120	T12	X_8	9	H3	Y_{17}
23	U3	GND	80	A5	P_{30}	36	R12	X_9	92	G2	Y_{18}
152	B13	HDERR	164	B5	P_{31}	119	T11	X_{10}	8	H1	Y_{19}
157	A9	NC	166	B3	PRERR	35	U10	X_{11}	91	G1	Y_{20}
60	D17	NC	56	H16	PP_0	118	U11	X_{12}	7	F2	Y_{21}
73	B9	NC	145	C16	PP_1	34	T10	X_{13}	90	F3	Y_{22}
82	C4	NC	159	C8	PP_2	117	R10	X_{14}	6	F1	Y_{23}
83	A3	NC	165	B4	PP_3	33	R9	X_{15}	5	E1	Y_{24}
84	B2	NC	64	A17	PSEL0	31	T9	X_{16}	88	E3	Y_{25}
66	C14	NC	148	A16	PSEL1	114	T8	X_{17}	4	D1	Y_{26}
167	C3	NC	37	U12	PX_0	30	R8	X_{18}	87	D2	Y_{27}
67	A14	NC	115	U9	PX_1	113	T7	X_{19}	3	D3	Y_{28}
149	B15	$\overline{OE}$	27	R6	PX_2	29	U8	X_{20}	86	C2	Y_{29}
48	M17	P_0	22	U1	PX_3	112	U7	X_{21}	2	C1	Y_{30}
132	M15	P_1	99	M2	PY_0	28	U6	X_{22}	85	B1	Y_{31}
133	K17	P_2	10	J2	PY_1	111	T6	X_{23}	127	T17	YSEL

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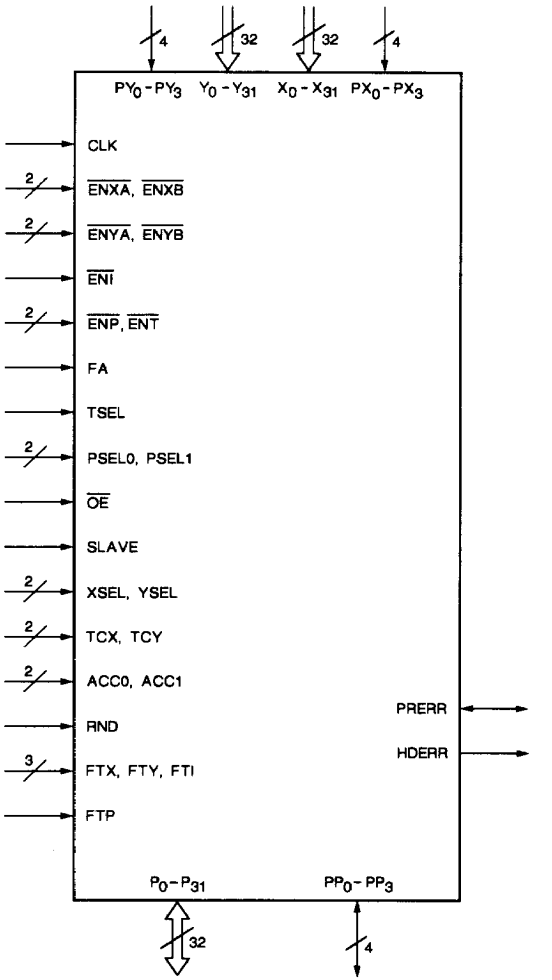
LOGIC SYMBOL



LS002803

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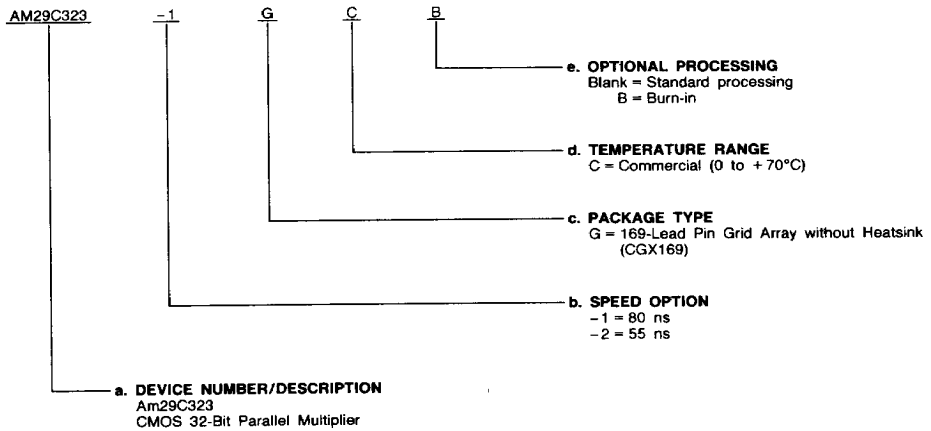
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C323	GC, GCB
AM29C323-1	
AM29C323-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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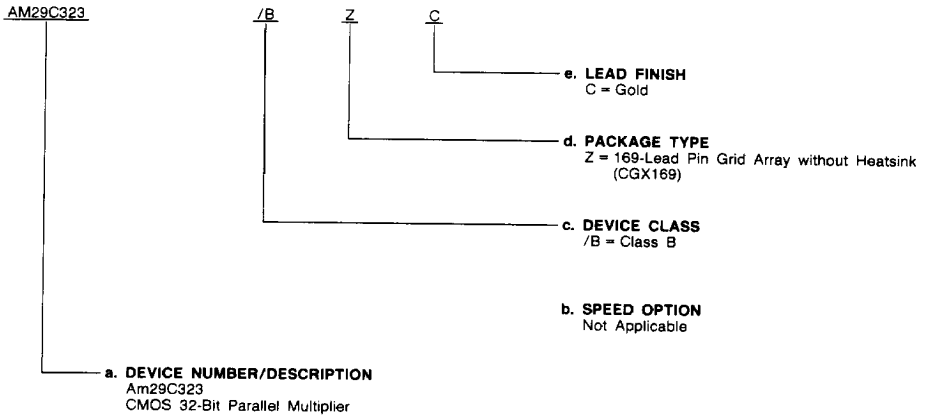
ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C323	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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PIN DESCRIPTION

ACC0, ACC1 Accumulator Control (Input)
Accumulator control lines used to determine accumulator function; PASS, ACCUMULATE, and SHIFT and ACCUMULATE.

CLK Clock (Input)
Clock input for all registers.

$\overline{ENI}$ Instruction Register Enable (Input; Active LOW)
Register enable for instruction register I.

$\overline{ENP}$ Accumulator Register Enable (Input; Active LOW)
Register enable for product register P.

$\overline{ENT}$ Temporary Register Enable (Input; Active LOW)
Register enable for temporary register T.

$\overline{ENXA}$, $\overline{ENXB}$ Multiplicand Register Enable (Input; Active LOW)
Register enables for multiplicand data input registers XA and XB.

$\overline{ENYA}$, $\overline{ENYB}$ Multiplier Register Enable (Input; Active LOW)
Register enables for multiplier data input registers YA and YB.

FA Format Adjust (Input)
Format adjust selects either a full 64-bit product (HIGH) or a left shifted 63-bit product suitable for fractional two's complement arithmetic (LOW).

FTP Feedthrough Control (Input; Active HIGH)
Feedthrough control for product register.

FTX, FTY, FTI Feedthrough Control (Input; Active HIGH)
Feedthrough control lines for X, Y, and I registers.

HDERR Hard Error Flag (Output)
Used when two Am29C323s are configured as master and slave to indicate hardware errors.

$\overline{OE}$ Output Enable Control (Input; Active LOW)
Used to enable (LOW) or disable (HIGH) the P output port.

$P_0 - P_{31}$ Product Output (Input/Output; Three State)
Product output for P port.

PRRER Parity Error Flag (Input/Output; Three State)
Indicates a parity error on the input buses.

$PP_0 - PP_3$ Byte Parity (Input/Output; Three State)
Byte parity generated on P output port (even parity).

PSEL0, PSEL1 Product Control (Input)
Used to select desired output including disabling P and PP output ports.

$PX_0 - PX_3$ Byte Parity (Input)
Byte parity inputs on X input port (even parity).

$PY_0 - PY_3$ Byte Parity (Input)
Byte parity inputs on Y input port (even parity).

RND Round Control (Input; Active HIGH)
Round control for rounding the most significant product.

SLAVE $\overline{Master}$/Slave Control (Input)
Used to determine mode of operation.

TCX, TCY Mode Control (Input)
Mode control inputs for each input data word; LOW for unsigned data and HIGH for two's complement format.

TSEL Select Control (Input)
Used to route the most significant product register (HIGH) or the least significant product register (LOW) into the temporary register.

$X_0 - X_{31}$ Multiplicand Data (Input)
Multiplicand data input for X port.

XSEL X Register Select (Input)
Control line used to route the contents of either the XA register (HIGH) or XB register (LOW) into the multiplier array.

$Y_0 - Y_{31}$ Multiplier Data (Input)
Multiplier data input for Y port.

YSEL Y Register Select (Input)
Control line used to route the contents of either the YA register (HIGH) or YB register (LOW) into the multiplier array.

FUNCTIONAL DESCRIPTION

Architecture

The Am29C323 comprises a high speed 32 by 32-bit multiplier array, a 67-bit accumulator, and a 32-bit data path.

Multiplier Array

The multiplier is a 32 by 32-bit array that produces a 64-bit product. This product is then fed to the accumulator section.

Accumulator

The accumulator is 67 bits wide. It performs accumulation for sum of product operations and multiprecision multiplication operations. The accumulator can perform three operations: store product without accumulation, accumulate product, and shift accumulator value and accumulate with product.

The shift and accumulate shifts the value in the product register 32 bits to the right (effectively moving the most significant 32 bits to the least significant 32 bits) and sign extends to a full 64 bits. This shifted value is then accumulated with the output of the multiplier array.

The 67-bit width is necessary to contain overflows in internal accumulations. These overflows are maintained and used when the product register is right shifted in the multiprecision multiplies. The lower 64 bits contain the 64-bit output while the upper 3 bits contain the overflow.

Data Path

The 32-bit data path consists of X and Y input buses; the P output bus; data registers XA, XB, YA, YB, and the product accumulator; two multiplier input multiplexers; byte parity input checkers; byte parity output generators; and master/slave comparators. Input operands enter the device through the two 32-bit input buses, $X_0 - X_{31}$ and $Y_0 - Y_{31}$. These operands may then be stored in one of the two registers for each bus (XA or XB for X, YA or YB for Y) or they may be fed directly through to the multiplier array. Input parity checking is performed as soon as the operands are put on the input buses. The signals used for output parity generation are taken from the input side of the output translator. In case of parity error, PRERR is enabled HIGH.

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Operational Modes

The Am29C323 can perform signed, unsigned, or mixed mode multiplication. These different numerical representations are controlled by TCX and TCY. A HIGH input on one of these lines indicates to the device that the respective input should be treated as a two's complement number; a LOW, an unsigned number. The output format is unsigned when both inputs are unsigned. The output format is two's complement when either or both inputs are two's complement.

Slave Mode

Each output has an associated comparator which compares the signal on the output pin with the signal provided to the output driver. If any of these outputs do not agree, the HDERR is asserted. When not in slave mode, this enables the multiplier to check for contention and bus shorts. However, when in slave mode, one multiplier can be used to detect faults in both internal functions and interconnections of the other multiplier. This is accomplished through the master/slave configuration, where the two multipliers operate in parallel. One multiplier is the master and operates normally; the other operates in slave mode.

In slave mode all outputs are turned into inputs from the master, except for the HDERR signal. Since the slave is operated in parallel with the master, it can compare the results it generates to those of the master and signal an error if they differ.

Command Description and Formats

The accumulator is controlled by ACC0 and ACC1. These lines are used to select any of the three operations that the accumulator can perform. This instruction set is described in Table 1.

The temporary output register is controlled by TSEL and FA. These lines are used to select any of the four different sets of data that can be stored in the temporary register. This instruction set is described in Table 2.

The output multiplexer is controlled by PSEL0, PSEL1, and FA. These lines are used to select any of the five different sets of data that can be output through the P port. PSEL0 and PSEL1 can also be used to disable the outputs. (This instruction is independent of $\overline{OE}$.) This instruction set is described in Table 3.

Format Adjust (FA) is used to select either a full 64-bit product or a left-shifted 63-bit product suitable for fractional two's complement arithmetic. This shifting increases the precision of the upper half of the product word by eliminating the redundant sign bit. Output Data Formats show the effect of FA.

Round (RND) is used to round the upper 32 bits of the 64-bit product. If only the upper 32 bits of the product are being used, then the lower 32 bits are truncated when rounding is not used (RND = 0). If rounding is used (RND = 1), then a "1" is added to the most significant of the lower 32 bits. This results in a smaller possible error. This should only be used when the lower 32 bits are to be truncated.

User Visible Register Descriptions

The Am29C323 contains seven different register sets, each with its own clock enable. Two 32-bit registers are attached to each of the input data buses. These registers are differentiated by the suffix A or B. For example, the X bus has registers XA and XB. The 67-bit accumulator register can be used as a regular product register when the part is used as a multiplier only or as the register part of the accumulator section. The 32-bit temporary output register is included to aid in the pipelining of multiprecision operations. An instruction register is also provided.

All of these registers can be made transparent with the exception of the accumulator register and the temporary register. The product from the multiplier can be fed directly to the output by using the FTP control line.

TABLE 1. ACCUMULATOR OPERATION INSTRUCTIONS

ACC1	ACC0	Accumulator Operation
0	0	PASS
0	1	ACCUMULATE
1	0	INVALID
1	1	SHIFT AND ACCUMULATE

TABLE 2. INPUT SELECT INSTRUCTIONS FOR TEMPORARY (T) REGISTER

TSEL	FA	Temp Reg Input
0	0	P_{i-1}
0	1	P_i
1	0	$P_i + 31$
1	1	$P_i + 32$

TABLE 3. OUTPUT SELECT INSTRUCTIONS FOR PRODUCT (P) PORT

PSEL1	PSEL0	FA	P Port Output
0	0	X	TEMP REGISTER
0	1	0	P_{i-1}
0	1	1	P_i
1	0	0	$P_i + 31$
1	0	1	$P_i + 32$
1	1	X	DISABLE

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Am29C323 X AND Y INPUT DATA FORMATS

Fractional Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

Integer Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

TCX, TCY = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer

TCX, TCY = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

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Am29C323 P-PORT OUTPUT DATA FORMATS

Fractional Two's Complement (Shifted)*

FA = 0, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

FA = 0, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}						2^{-60}	2^{-61}	2^{-62}	2^{-63}**

Fractional Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}						2^{-27}	2^{-28}	2^{-29}	2^{-30}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-31}	2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}						2^{-59}	2^{-60}	2^{-61}	2^{-62}

Integer Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}	2^{-38}						2^{-61}	2^{-62}	2^{-63}	2^{-64}

Unsigned Integer

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

*In this format, an overflow occurs in the attempted multiplication of the two's complement number −1.000 with itself, yielding a product of +1.000 which cannot be represented in this format. **This bit position (2^{-63}) equals zero in this format.

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64 x 64 Multiplication

To perform a 64 x 64-bit multiplication using the Am29C323, each 64-bit input must be split into two 32-bit inputs; a most significant half and a least significant half (XW1 and XW0 or YW1 and YW0, respectively). These 32-bit inputs are then used to perform the four multiplications needed to obtain the 128-bit product. This product is represented in four 32-bit words, $PW_3 - PW_0$, the least significant word being PW_0. The product is output 32 bits at a time through the product (P) port. The following equation shows the required multiplications:

$$X * Y = ((XW1 * YW1) * 2^{64}) + ((XW0 * YW1) * 2^{32}) + ((XW1 * YW0) * 2^{32}) + ((XW0 * YW0) * 2^{0})$$

$$P = (PW3 * 2^{96}) + (PW2 * 2^{64}) + (PW1 * 2^{32}) + (PW0 * 2^{0})$$

The Am29C323 uses an internal accumulator to sum these intermediate products. The previous equation, in a slightly different form, is shown with the necessary instructions below:

X →				XW1	XW0	
Y →			*	YW1	YW0	
				XW0	* YW0	← Multiply only
		XW1	* YW0			← Mult & Shift/Acc
		XW0	* YW1			← Mult & Accumulate
	XW1	* YW1				← Mult & Shift/Acc
P →	PW3		PW2	PW1	PW0	

Table 4 details the movement of the input operands through the Am29C323. Table 5 defines the microcode required to perform a signed 64 x 64-bit multiplication. For an unsigned multiplication, TCX and TCY are LOW for all cycles. The operations and data movement are scheduled to produce a single product in seven clock cycles or a new pipelined product every four clock cycles.

TABLE 4. BUS AND REGISTER CONTENTS FOR A 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6
X BUS	XW0	XW1			XW0	XW1	
XA REG	XW0	XW0	XW0	XW0	XW0	XW0	XW0
XB REG	XW1	XW1	XW1	XW1	XW1	XW1	XW1
Y BUS	YW0	YW1			YW0	YW1	
YA REG	YW0	YW0	YW0	YW0	YW0	YW0	YW0
YB REG	YW1	YW1	YW1	YW1	YW1	YW1	YW1
MPY OP	XW1•YW1	XW0•YW0	XW1•YW0	XW0•YW1	XW1•YW1	XW0•YW0	XW1•YW0
ACC OP	S/A	PASS	S/A	ACC	S/A	PASS	S/A
T REG		PW3	PW0			PW3	
P BUS	PW1	PW2	PW3	PW0	PW1	PW2	PW3

Note: MPY OP = Operation of multiplier array (X•Y)
ACC OP = Operation of internal accumulator
PASS = Pass through multiplier product
ACC = Add previous result to current product
S/A = Shift previous result then add to current product

TABLE 5. INSTRUCTION MICROCODE FOR 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6	7	8	9	A	B	C	D
$\overline{ENXA}$	0	1	1	1	0	1	1	1	0	1	1	1	0	1
$\overline{ENXB}$	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCX	0	1	0	1	0	1	0	1	0	1	0	1	0	1
XSEL	1	0	1	0	1	0	1	0	1	0	1	0	1	0
$\overline{ENYA}$	0	1	1	1	0	1	1	1	0	1	1	1	0	1
$\overline{ENYB}$	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCY	0	0	1	1	0	0	1	1	0	0	1	1	0	0
YSEL	1	1	0	0	1	1	0	0	1	1	0	0	1	1
$\overline{ENI}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{ENT}$	1	0	0	1	1	0	0	1	1	0	0	1	1	0
TSEL	X	1	0	X	X	1	0	X	X	1	0	X	X	1
ACC0	0	1	1	1	0	1	1	1	0	1	1	1	0	1
ACC1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$\overline{ENP}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PSEL0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PSEL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.3 to +7.0 V
DC Voltage Applied to Outputs For
High Output State ..... −0.3 to +V_{CC} + 0.3 V
DC Input Voltage ..... −0.3 to +V_{CC} + 0.3 V
DC Output Current, Into LOW Outputs ..... 30 mA
DC Input Current ..... −10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military* (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_A = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} I_{OH} = −0.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−10	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} −0.5 V			10	μA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V		10	μA
			V_O = 0.5 V		−10	
I_{CC}	Static Power Supply Current	V_{CC} = Max., V_{IN} = V_{CC} or GND, I_O = 0 μA	COM'L		25	mA
			MIL		25	
C_{PD}	Power Dissipation Capacitance (Note 3)	V_{CC} = 5.0 V, T_A = 25°C, No Load		3000 pF Typical		

Notes: 1. V_{CC} conditions shown as Min. or Max., refer to the military or commercial V_{CC} limits.
2. These input levels provide zero noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. C_{PD} determines the no-load dynamic current consumption:
I_{CC} (Total) = I_{CC} (Static) + C_{PD} V_{CC} f, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency. This specification is not tested.

PRELIMINARY

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Symbol	Parameter Description	Test Conditions	29C323		29C323-1		29C323-2		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
UNCLOCKED MODE										
1	t_{MUC}	Unclocked Multiply Time $X_0 - X_{31}$, $Y_0 - Y_{31}$ to $P_0 - P_{31}$	FTX/Y/P = HIGH		120		100		70	ns
2	t_{MUCPP}	Unclocked Multiply Time $X_0 - X_{31}$, $Y_0 - Y_{31}$ to $PP_0 - PP_3$	FTX/Y/P = HIGH		125		105		75	ns
3	t_{IP}	Instruction to $P_0 - P_{31}$ (Note 1)	Output Taken From Adder FTI = HIGH		120		100		70	ns
4	t_{IPP}	Instruction to $PP_0 - PP_3$	Output Taken From Adder FTI = HIGH		125		105		75	ns
CLOCKED MODE										
5	t_{MC}	Clocked Multiply Time	FTX/Y/P = LOW		100		80		55	ns
6	t_{PDP}	Clock to $P_0 - P_{31}$	Output Taken from Temp or Product Reg.		38		30		25	ns
7	t_{PDPP}	Clock to $PP_0 - PP_3$	Output Taken from Temp or Product Reg.		43		35		30	ns
8	t_{PAP}	Clock to $P_0 - P_{31}$	Output Taken from Adder, FTX/Y/I = LOW		135		115		80	ns
9	t_{PAPP}	Clock to $PP_0 - PP_3$	Output Taken from Adder, FTX/Y/I = LOW		140		120		85	ns
10	t_{SP}	Data to Product Register Setup Time	FTX/Y = HIGH	110		90		65		ns
11	t_{HP}	Data to Product Register Hold Time	FTX/Y = HIGH	0		0		0		ns
12	t_{SIPT}	Instruction to Product Register Setup Time	FTI = HIGH	110		90		65		ns
13	t_{HIPT}	Instruction to Product Register Hold Time	FTI = HIGH	0		0		0		ns
14	t_{PWH}	Clock Pulse Width HIGH		20		20		15		ns
15	t_{PWL}	Clock Pulse Width LOW		20		20		15		ns
SETUP AND HOLD TIMES										
16	t_{SXY}	Register XA, XB, YA, YB Setup Time		21		18		15		ns
17	t_{HXY}	Register XA, XB, YA, YB Hold Time		0		0		0		ns
18	t_{SI}	Instruction Register Setup Time		18		15		10		ns
19	t_{HI}	Instruction Register Hold Time		0		0		0		ns
20	t_{SEN}	Register Enable Setup Time		18		15		10		ns
21	t_{HEN}	Register Enable Hold Time		0		0		0		ns
22	t_{STS}	TSEL Setup Time		18		15		10		ns
23	t_{HTS}	TSEL Hold Time		0		0		0		ns
COMMON PARAMETERS										
24	t_{PP}	PSEL0 – PSEL1 to $P_0 - P_{31}$	To Active State Only		35		30		25	ns
25	t_{PPP}	PSEL0 – PSEL1 to $PP_0 - PP_3$	To Active State Only		35		30		25	ns
26	t_{OEP1}	$\overline{OE}$ to $P_0 - P_{31}$, $PP_0 - PP_3$ Output Enable			35		30		25	ns
27	t_{OD}	$\overline{OE}$ or PSEL0 – PSEL1 to $P_0 - P_{31}$, $PP_0 - PP_3$ Output Disable			35		30		25	ns
28	t_{DPE}	Data to PRERR			35		35		30	ns
29	t_{DHE}	Data to HDERR	Slave = HIGH		40		40		35	ns

Notes: 1. Instruction signals are XSEL, YSEL, TCX, TCY, ACC0, ACC1, and RND.

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SWITCHING CHARACTERISTICS over **MILITARY** operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	29C323 Min.	29C323 Max.	Unit
UNCLOCKED MODE						
1	t_{MUC}	Unclocked Multiply Time $X_0 - X_{31}$, $Y_0 - Y_{31}$ to $P_0 - P_{31}$	FTX/Y/P = HIGH		140	ns
2	t_{MUCPP}	Unclocked Multiply Time $X_0 - X_{31}$, $Y_0 - Y_{31}$ to $PP_0 - PP_3$	FTX/Y/P = HIGH		145	ns
3	t_{IP}	Instruction to $P_0 - P_{31}$ (Note 1)	Output Taken From Adder FTI = HIGH		140	ns
4	t_{IPP}	Instruction to $PP_0 - PP_3$	Output Taken From Adder FTI = HIGH		145	ns
CLOCKED MODE						
5	t_{MC}	Clocked Multiply Time	FTX/Y/P = LOW		120	ns
6	t_{PDP}	Clock to $P_0 - P_{31}$	Output Taken from Temp or Product Reg.		45	ns
7	t_{PDPP}	Clock to $PP_0 - PP_3$	Output Taken from Temp or Product Reg.		50	ns
8	t_{PAP}	Clock to $P_0 - P_{31}$	Output Taken from Adder, FTX/Y/I = LOW		150	ns
9	t_{PAPP}	Clock to $PP_0 - PP_3$	Output Taken from Adder, FTX/Y/I = LOW		155	ns
10	t_{SP}	Data to Product Register Setup Time	FTX/Y = HIGH	135		ns
11	t_{HP}	Data to Product Register Hold Time	FTX/Y = HIGH	0		ns
12	t_{SIPT}	Instruction to Product Reg. Setup Time	FTI = HIGH	135		ns
13	t_{HIPT}	Instruction to Product Reg. Hold Time	FTI = HIGH	0		ns
14	t_{PWH}	Clock Pulse Width HIGH		20		ns
15	t_{PWL}	Clock Pulse Width LOW		20		ns
SETUP AND HOLD TIMES						
16	t_{SXY}	Register XA, XB, YA, YB Setup Time		24		ns
17	t_{HXY}	Register XA, XB, YA, YB Hold Time		0		ns
18	t_{SI}	Instruction Register Setup Time		20		ns
19	t_{HI}	Instruction Register Hold Time		0		ns
20	t_{SEN}	Register Enable Setup Time		20		ns
21	t_{HEN}	Register Enable Hold Time		0		ns
22	t_{STS}	TSEL Setup Time		20		ns
23	t_{HTS}	TSEL Hold Time		0		ns
COMMON PARAMETERS						
24	t_{PP}	PSEL0 - PSEL1 to $P_0 - P_{31}$	To Active State Only		40	ns
25	t_{PPP}	PSEL0 - PSEL1 to $PP_0 - PP_3$	To Active State Only		40	ns
26	t_{OEP1}	$\overline{OE}$ to $P_0 - P_{31}$, $PP_0 - PP_3$ Output Enable			40	ns
27	t_{OD}	$\overline{OE}$ or PSEL0 - PSEL1 to $P_0 - P_{31}$, $PP_0 - PP_3$ Output Disable			40	ns
28	t_{DPE}	Data to PRERR			40	ns
29	t_{DHE}	Data to HDERR	Slave = HIGH		45	ns

Notes: 1. Instruction signals are XSEL, YSEL, TCX, TCY, ACC0, ACC1, and RND.

PRELIMINARY

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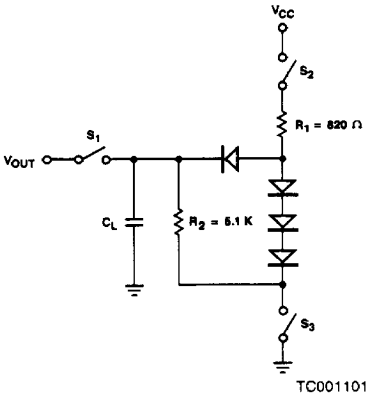
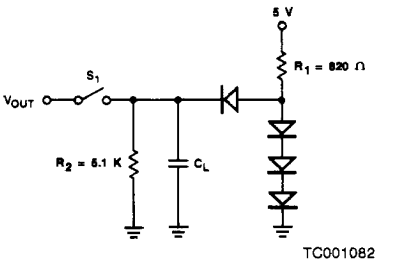
SWITCHING TEST CIRCUITS



A. Three-State Outputs

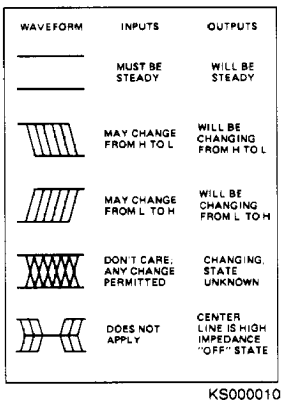


B. Normal Outputs

Notes: 1. C_L = 50 PF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = TBD for output disable tests.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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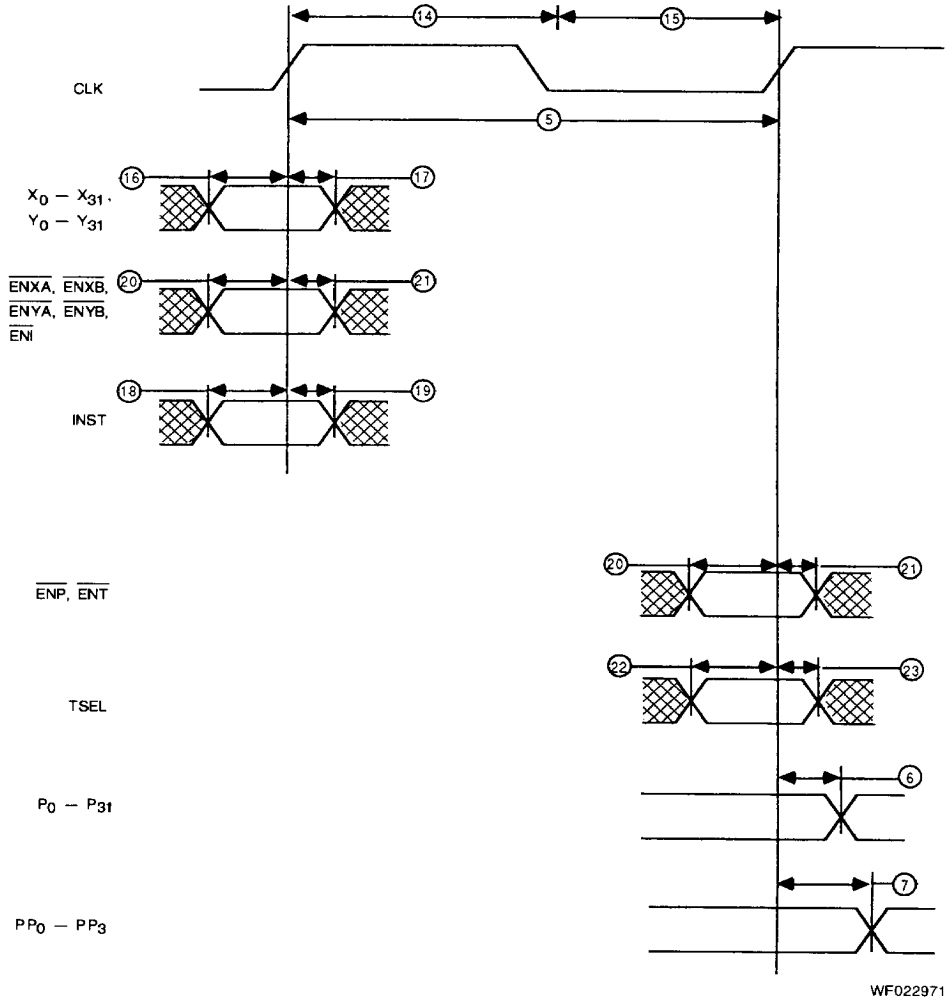
SWITCHING WAVEFORMS (Cont'd.)



Clocked Operation: FTX, Y, P, I = LOW

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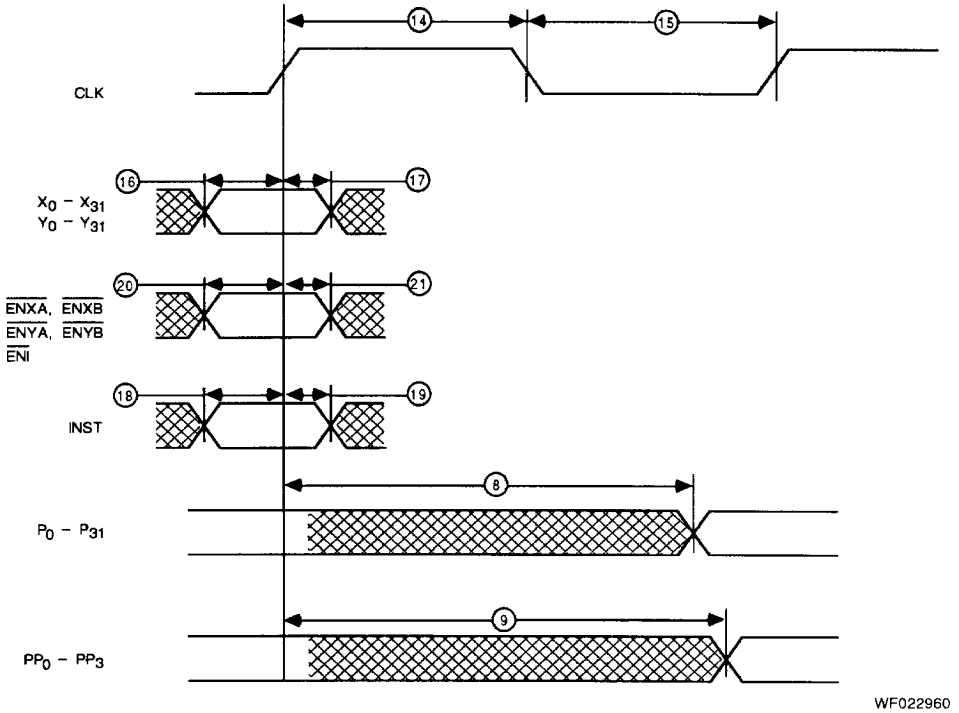
SWITCHING WAVEFORMS (Cont'd.)



Clocked Operation: Output Taken from Adder
(FTX, Y, I = LOW; FTP = HIGH; PSEL1 ≠ PSEL0)

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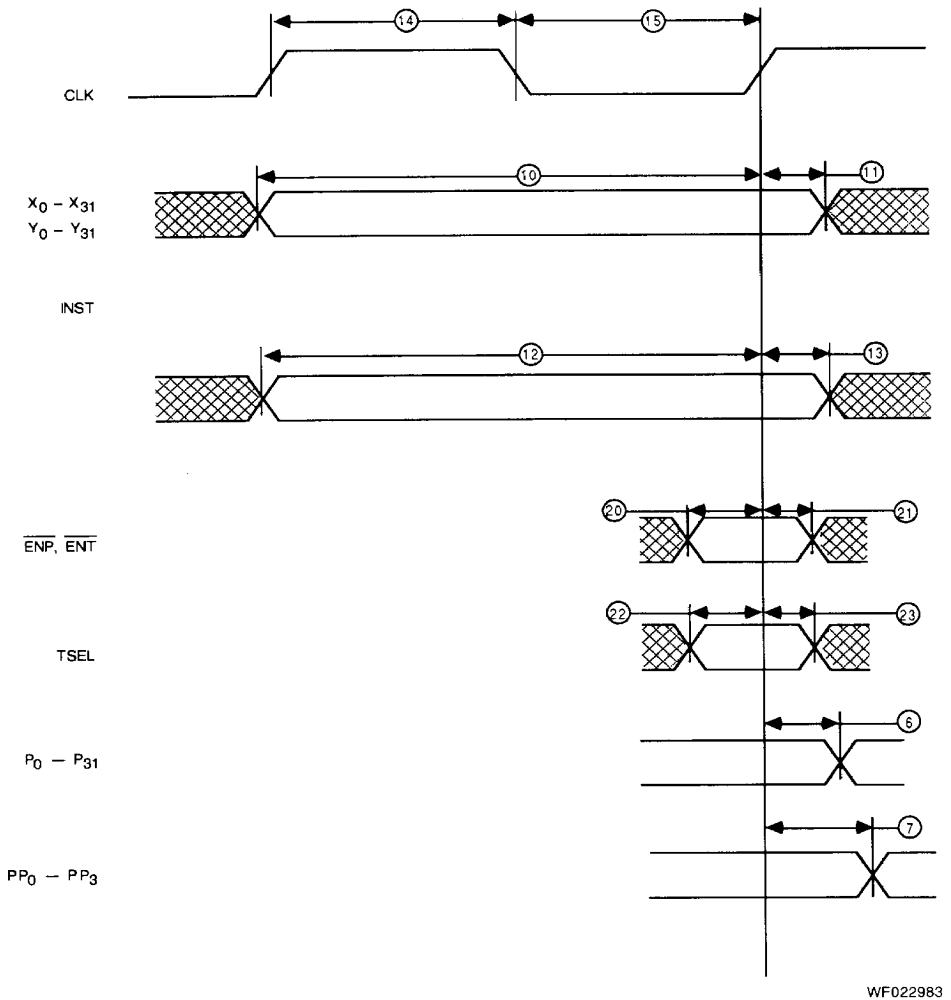
SWITCHING WAVEFORMS (Cont'd.)



Clocked Operation: Input Registers Bypassed (FTX, Y, I = HIGH; FTP = LOW)

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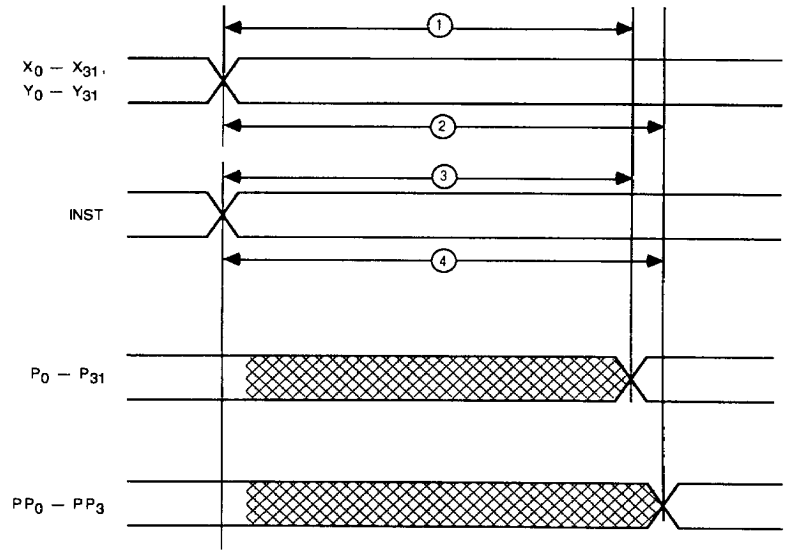
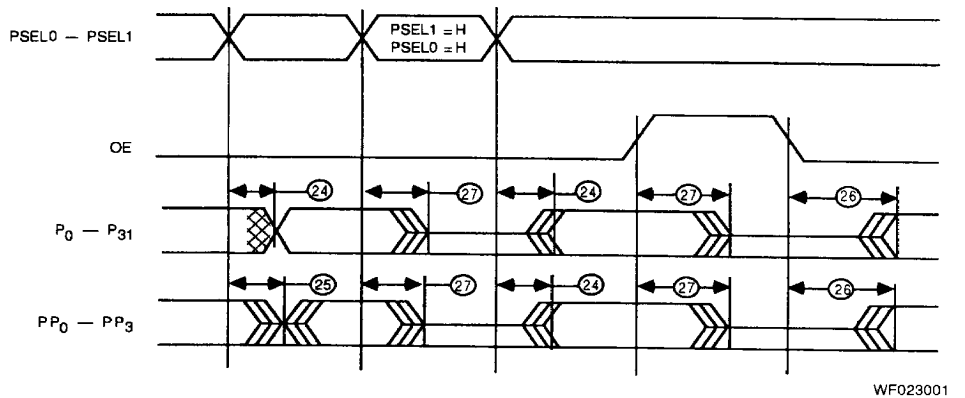
SWITCHING WAVEFORMS (Cont'd.)



WF022990

Unclocked Mode: FTX, Y, I, P = HIGH



WF023001

Output Select Timing

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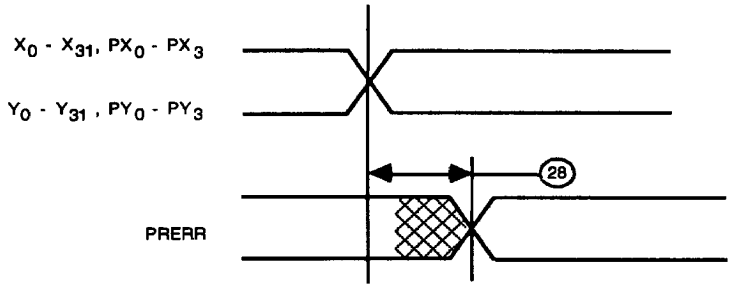
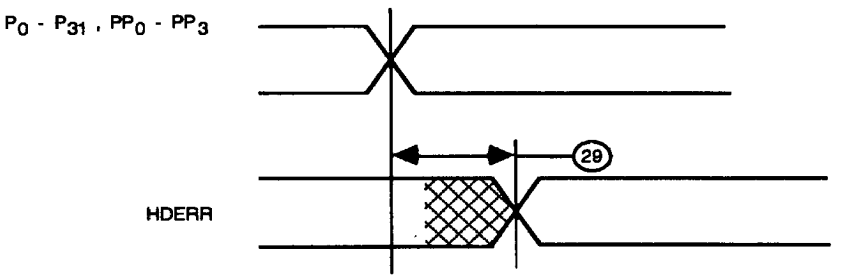
SWITCHING WAVEFORMS (Cont'd.)



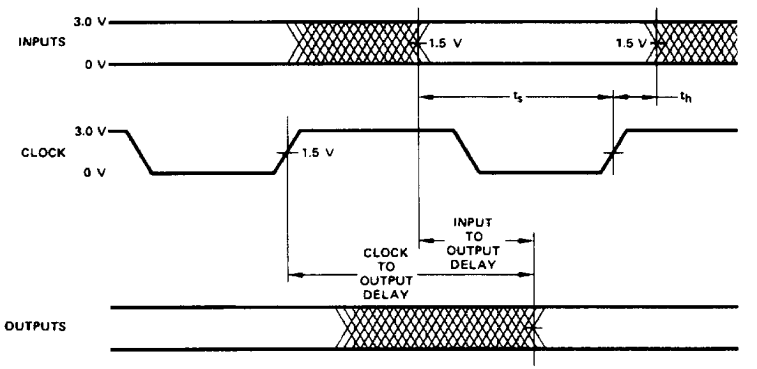
WF023013

PRERR Timing



WF023024

Slave Mode Timing



WFR02990

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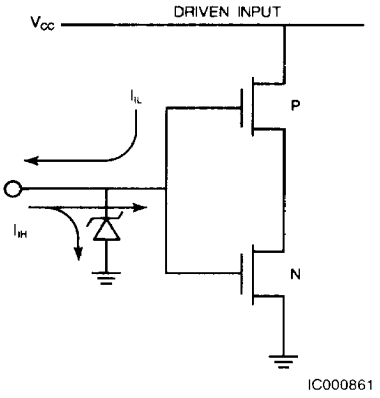
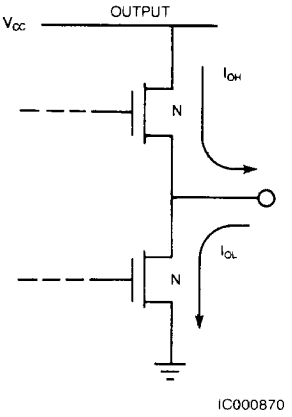
INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS



$C_I \approx 5.0$ pF, all inputs



$C_O \approx 5.0$ pF, all outputs

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