μPD42274
Dual-Port Graphics Buffer

Description

The μPD42274 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42274 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42274 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

- Three functional blocks
  - 256K x 4-bit random access storage array
  - 2048-bit data register
  - 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt ±10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Write-per-bit option regarding four I/O bits
  - Write bit selection multiplexed on IO_0-IO_3
- Flash write option with write-per-bit control
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42274LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42274V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
FWE	Flash write enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

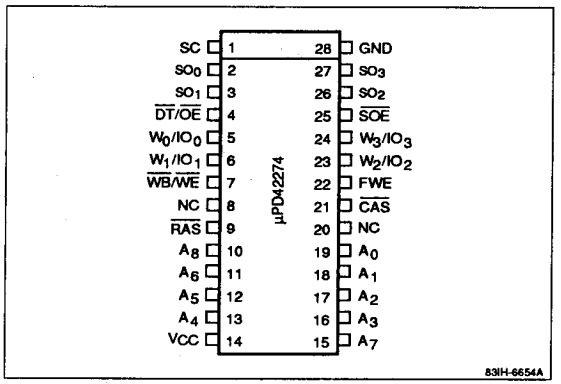
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

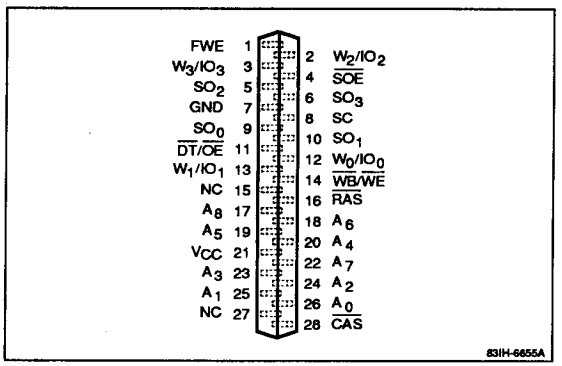
Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write or flash write cycle, and then updated at the next falling edge of $\overline{RAS}$.

In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, and FWE are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and FWE inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write- per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$ and FWE are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

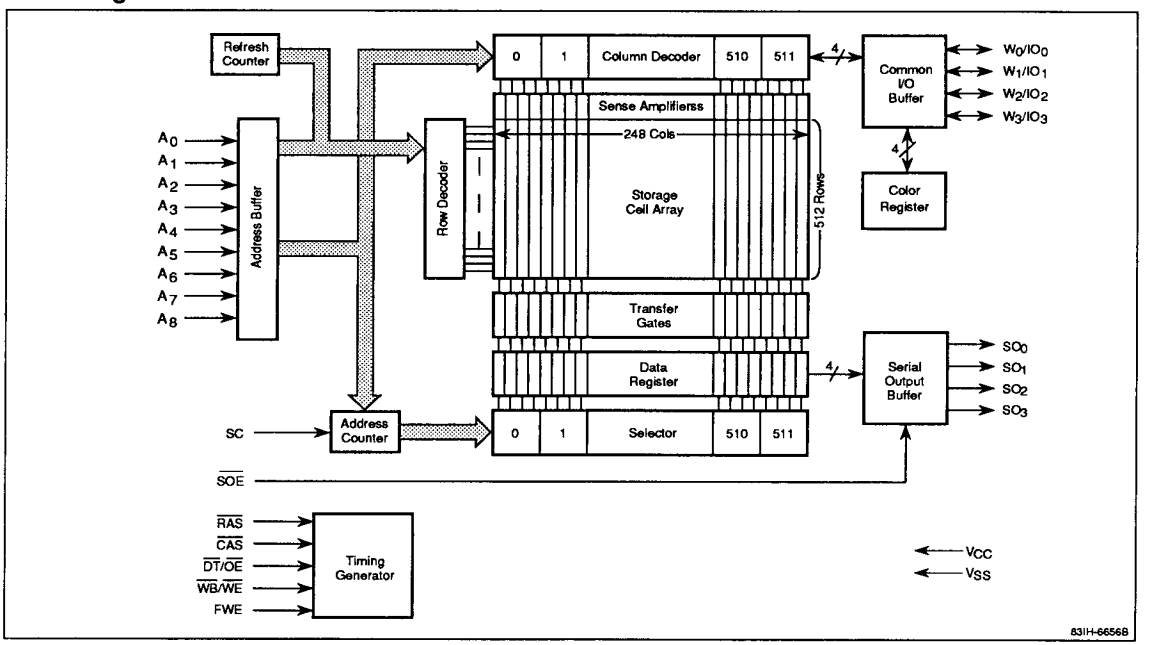
FWE (Flash Write Enable). If this signal is low and $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, a read or write cycle is initiated. If FWE, $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, either a color register set cycle or flash write cycle is initiated, depending on the level of $\overline{WB/WE}$.

SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

Block Diagram



OPERATION

The μPD42274 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location (unless the flash write option is used to write an entire row of data to predetermined values). The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT/OE}$
- $\overline{WB/WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42274 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	FWE	Cycle
H	H	H	L	Read or write (Note 1)
H	H	L	L	Mask write (Note 2)
H	L	X	L	Read data transfer (Note 3)
H	L	H	H	
L	X	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 4)
H	H	H	H	Color register set (Note 5)
H	H	L	H	Flash write/write-per-bit (Note 6)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per- bit capability.

(2) Enables the write-per-bit capability, where individual bits can be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at the rising edge of $\overline{RAS}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB/WE}$, $\overline{DT/OE}$ and FWE = don't care.

(5) Defines a color register set cycle, where data in the register can be accessed in a read or write cycle.

(6) Initiates a flash write cycle, where the storage cells on an entire selected row can be set with write-per-bit control to the same data stored in the color register. As $\overline{RAS}$ falls, $\overline{DT/OE}$ = don't care. To avoid un-intended flash write operation, the FWE pin should be grounded. If grounding the FWE pin is not possible, use the non-flash write version μPD42273.

(7) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $(\overline{WB}/)\overline{WE}$ while $\overline{CAS}$ is active. The $(W_i/)IO_i$ pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to ±CAS delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing (WB/)WE low during the RAS/CAS cycle. The falling edge of CAS or (WB/)WE strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, WB(/WE) must be low as RAS falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of RAS.

For those data bits of W_i(/IO_i) that are kept low as RAS falls, write operation is inhibited on the chip. If WB(/WE) is high as RAS falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing (WB/)WE low before CAS falls. Data is strobed by CAS, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As RAS falls, (DT/)OE must meet the setup and hold times of a high DT, but otherwise (DT/)OE does not affect any circuit operation while CAS is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing (WB/)WE low with the RAS and CAS signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when (DT/)OE goes high. The data to be written is strobed by (WB/)WE, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of (DT/)OE, which can be activated just after (WB/)WE falls, even when (WB/)WE is brought low after CAS.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, or flash write) refreshes the 2048 bits selected by the RAS addresses or by the on-chip refresh address counter.

RAS-Only Refresh Cycle. A cycle having only RAS active refreshes all cells in one row of the storage array. A high CAS is maintained while RAS is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when RAS-only refresh cycles are executed.

CAS Before RAS Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever CAS is low as RAS falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on CAS is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next CAS before RAS cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by CAS and OE. After the read cycle, CAS is held low while RAS goes high for precharge. A RAS-only cycle is then executed (except that CAS is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as CAS before RAS refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining RAS low while successive CAS cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the (W_i/)IO_i data pin (i = 0, 1, 2, or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ and FWE low as $\overline{RAS}$ falls. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Color Register Set Cycle. A color register set cycle is executed in the same fashion as a conventional read or write cycle, with the level of $\overline{WE}$ high as $\overline{RAS}$ falls. In this cycle, read or write operation is available to the color register under the control of $\overline{WE}$. In read operation, color register data is read out on the common IO_i pins. In write operation, common IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8 in this cycle.

Flash Write Cycle. A flash write cycle can clear or set each of the four 512-bit data sets on the one row selected from among the 512 possible rows according to data stored in the color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Serial Read Port

The serial read port is only used to serially read the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this cycle, the serial read port can operate asynchronously. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42274 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(FWE)}$	8	pF	FWE
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation						
Random Access	Serial Read	Parameter	μPD42274-10 (max)	μPD42274-12 (max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	4	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	95	85	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	90	80	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min ; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	95	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	135	120	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	105	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Standby	Active	I_{CC8}	30	25	mA	$\overline{CAS}$ = $\overline{RAS}$ = V_{IH}; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	105	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; FWE low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Fast-page cycle	Active	I_{CC10}	115	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min ; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	105	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Data transfer cycle	Active	I_{CC12}	160	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Color register set cycle	Standby	I_{CC13}	95	85	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	95	85	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IH}; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	120	105	mA	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min
Flash write cycle	Active	I_{CC16}	120	105	mA	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Notes 3 and 18)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	(Note 18)
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)

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AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh interval	t_{REF}		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	80		90		ns	(Note 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Write-per-bit hold time	t_{WBH}	15		20		ns	
Flash write enable setup time	t_{FWS}	0		0		ns	
Flash write enable hold time	t_{FWH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameter in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Improvement in parameters t_{RDH}, t_{RP} and t_{SCA} are planned for process versions "x" and "m". Please contact your NEC sales office for details.

(19) Ac measurements assume t_T = 5 ns.

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Figure 1. Input Timing

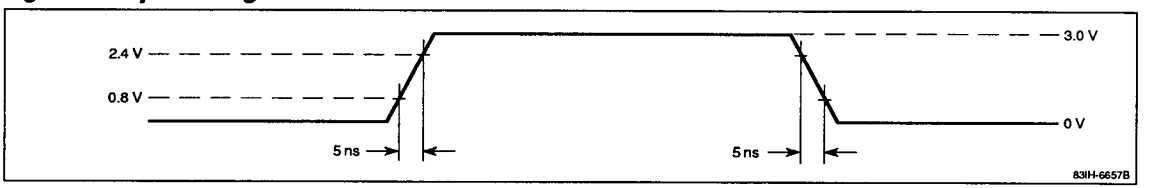


Figure 2. Output Timing

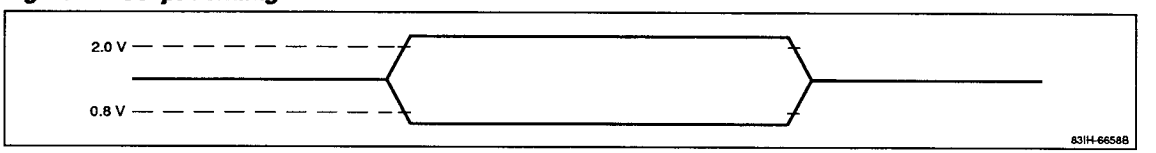


Figure 3. Output Load in Random Access Port

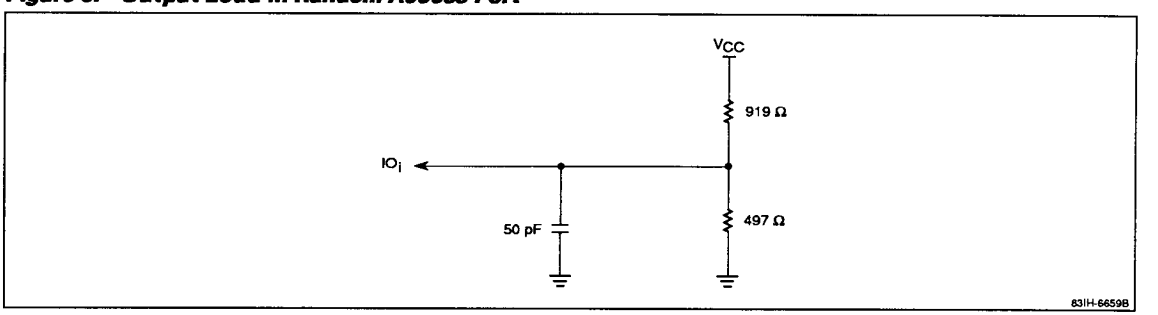
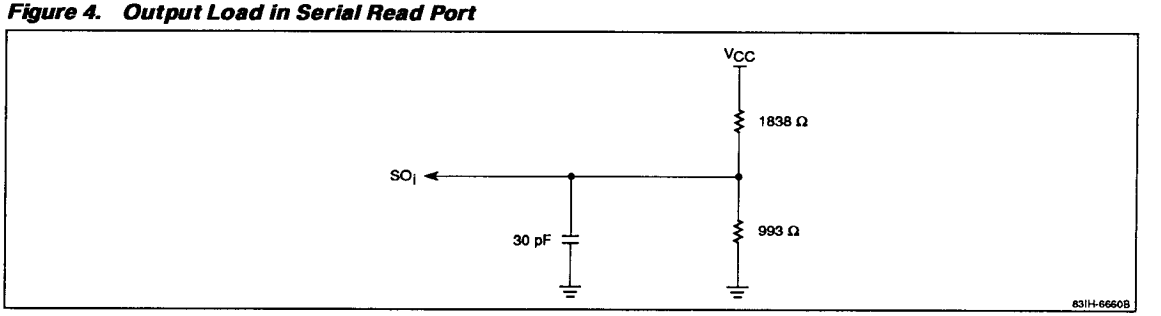
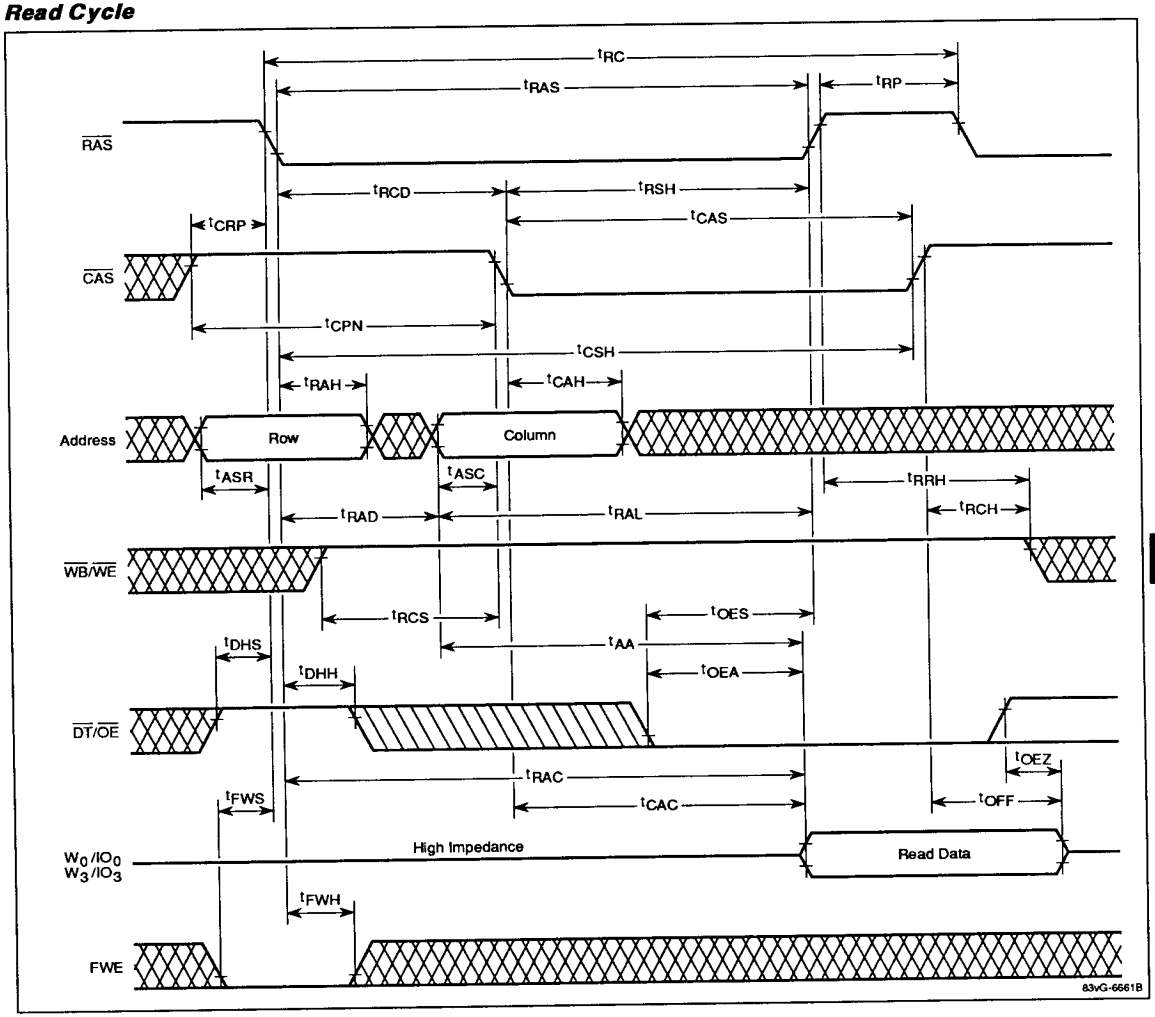


Figure 4. Output Load in Serial Read Port



Timing Waveforms

Read Cycle



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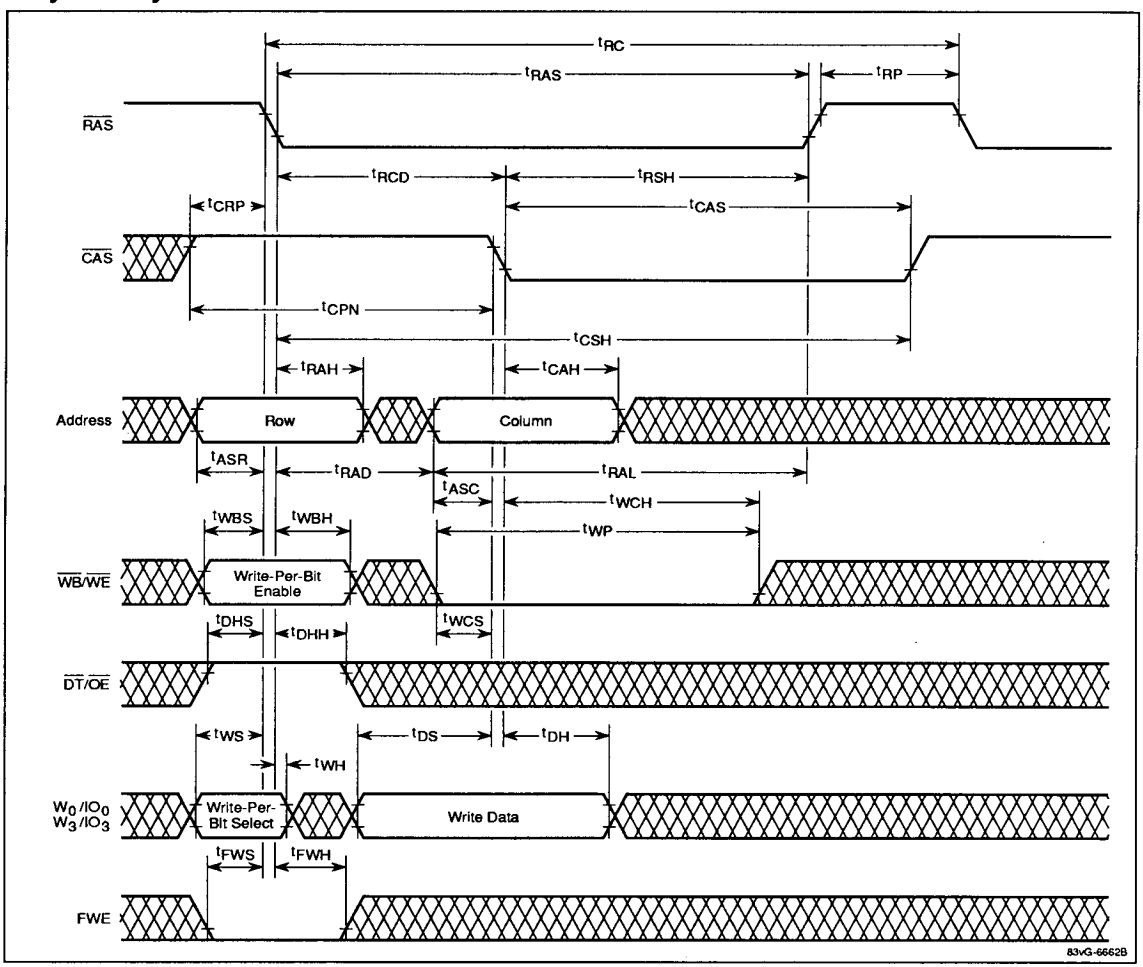
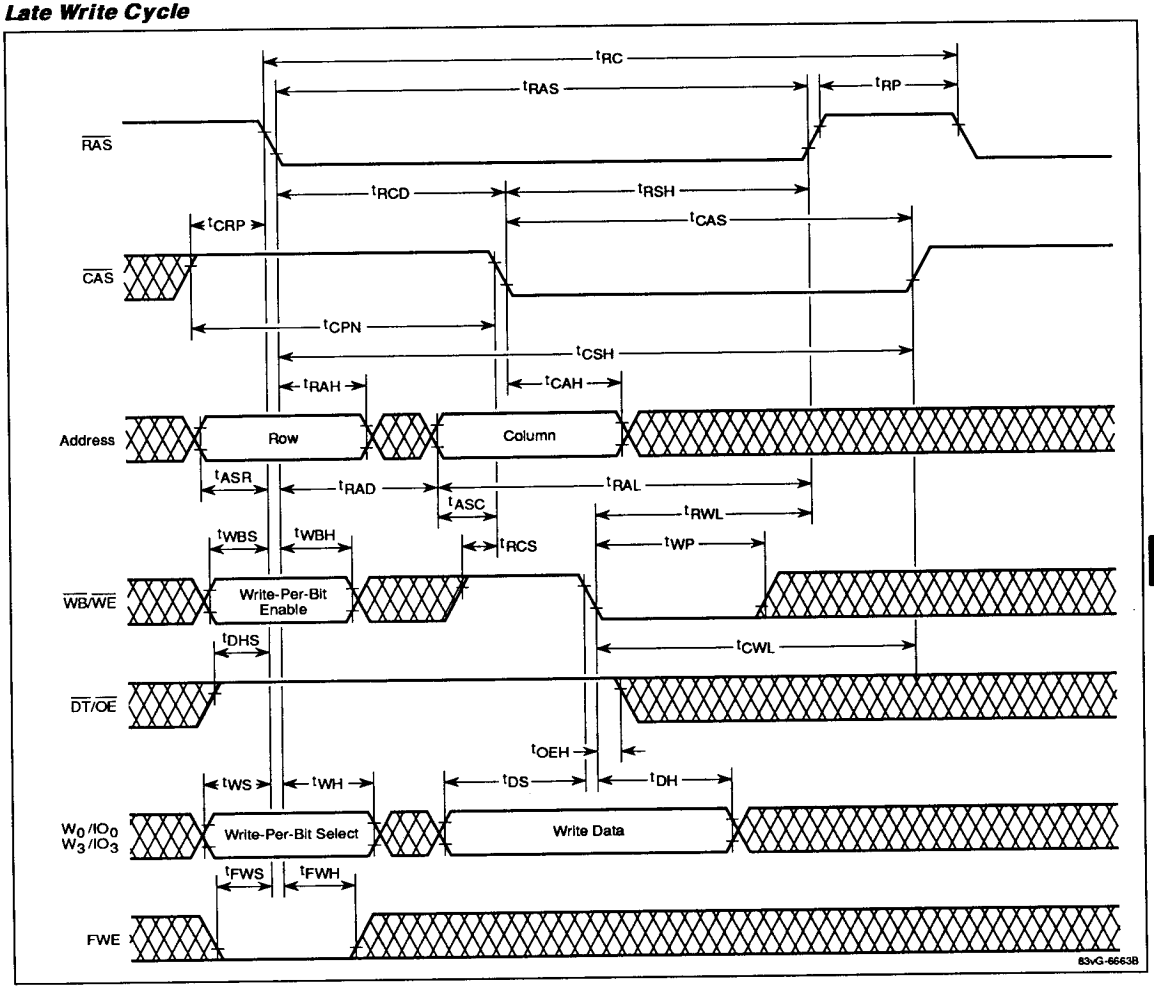
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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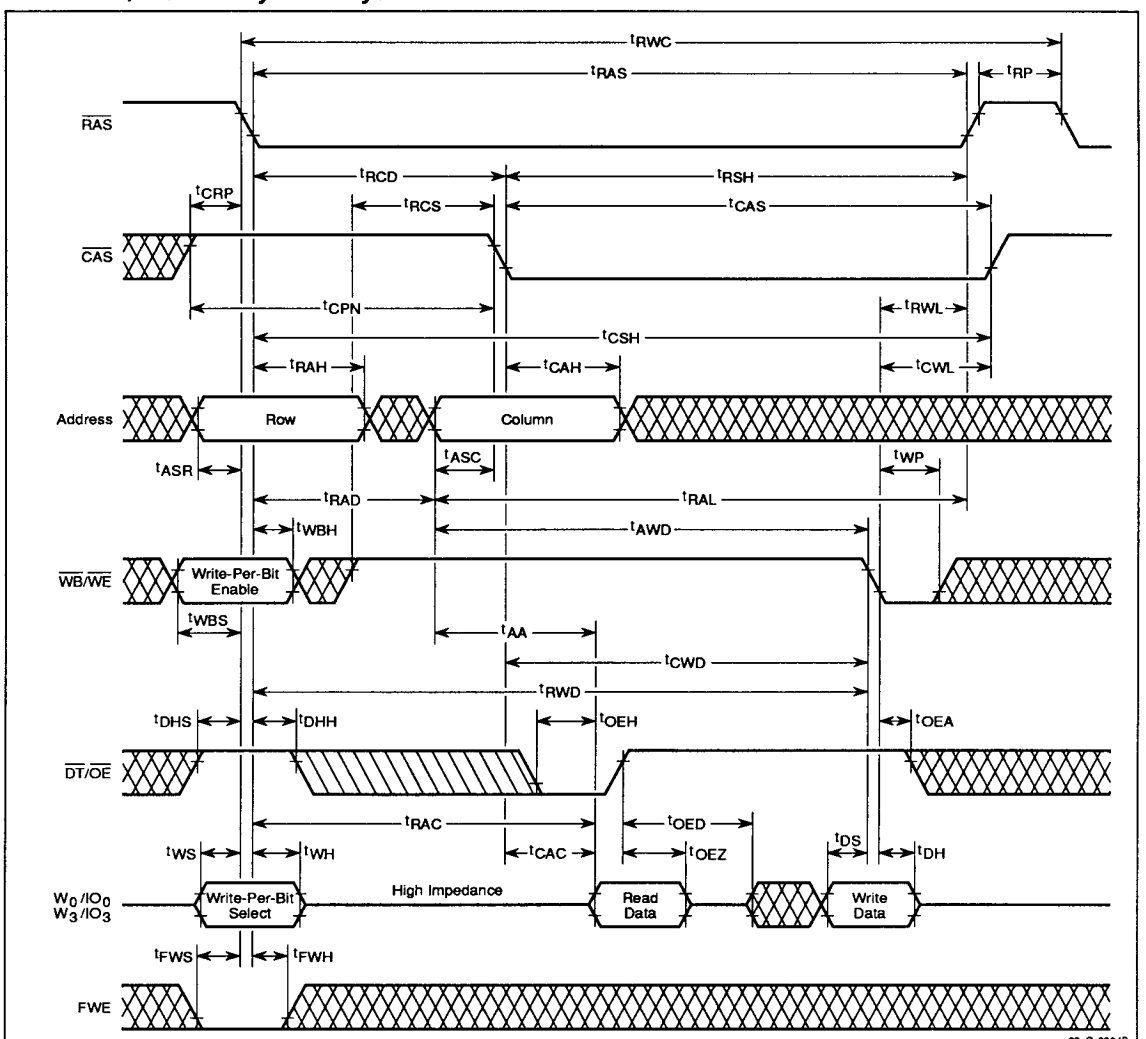
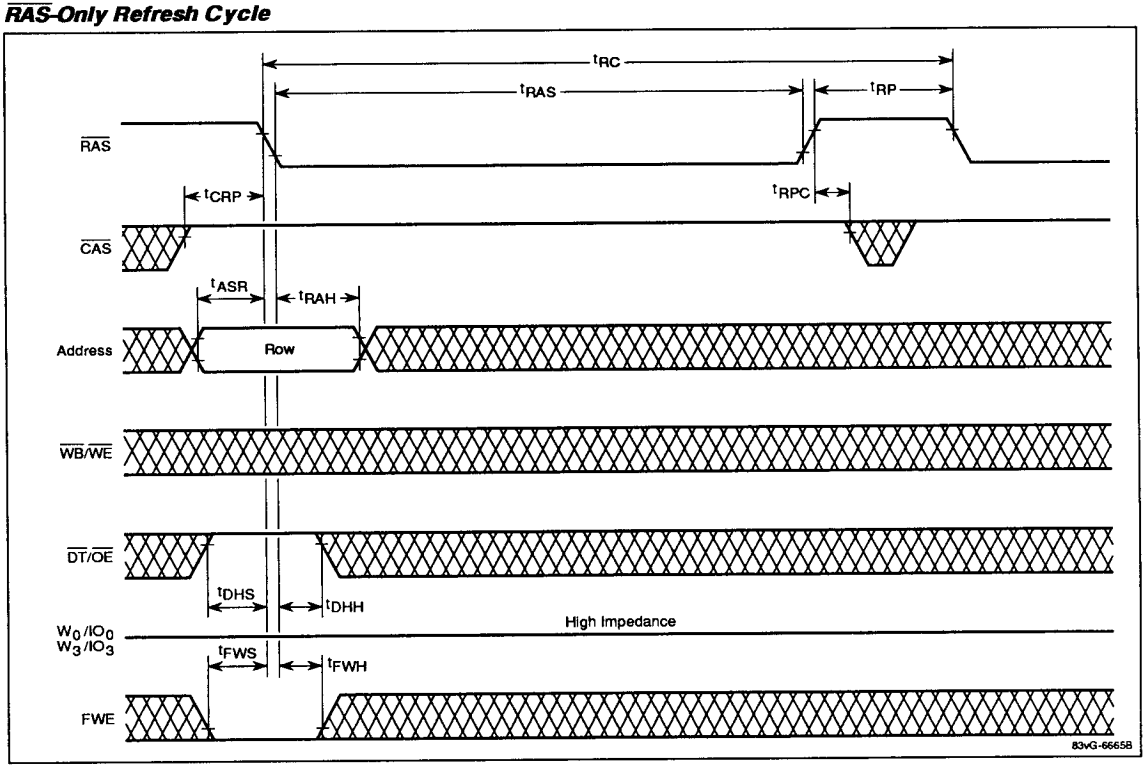
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



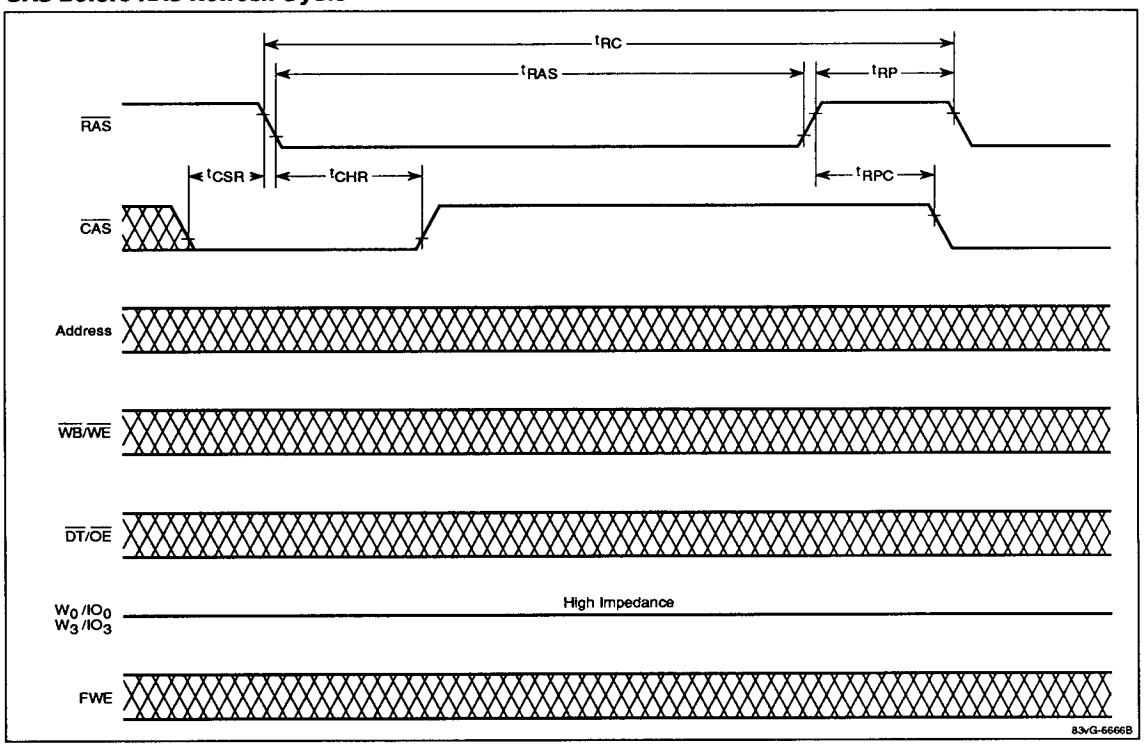
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



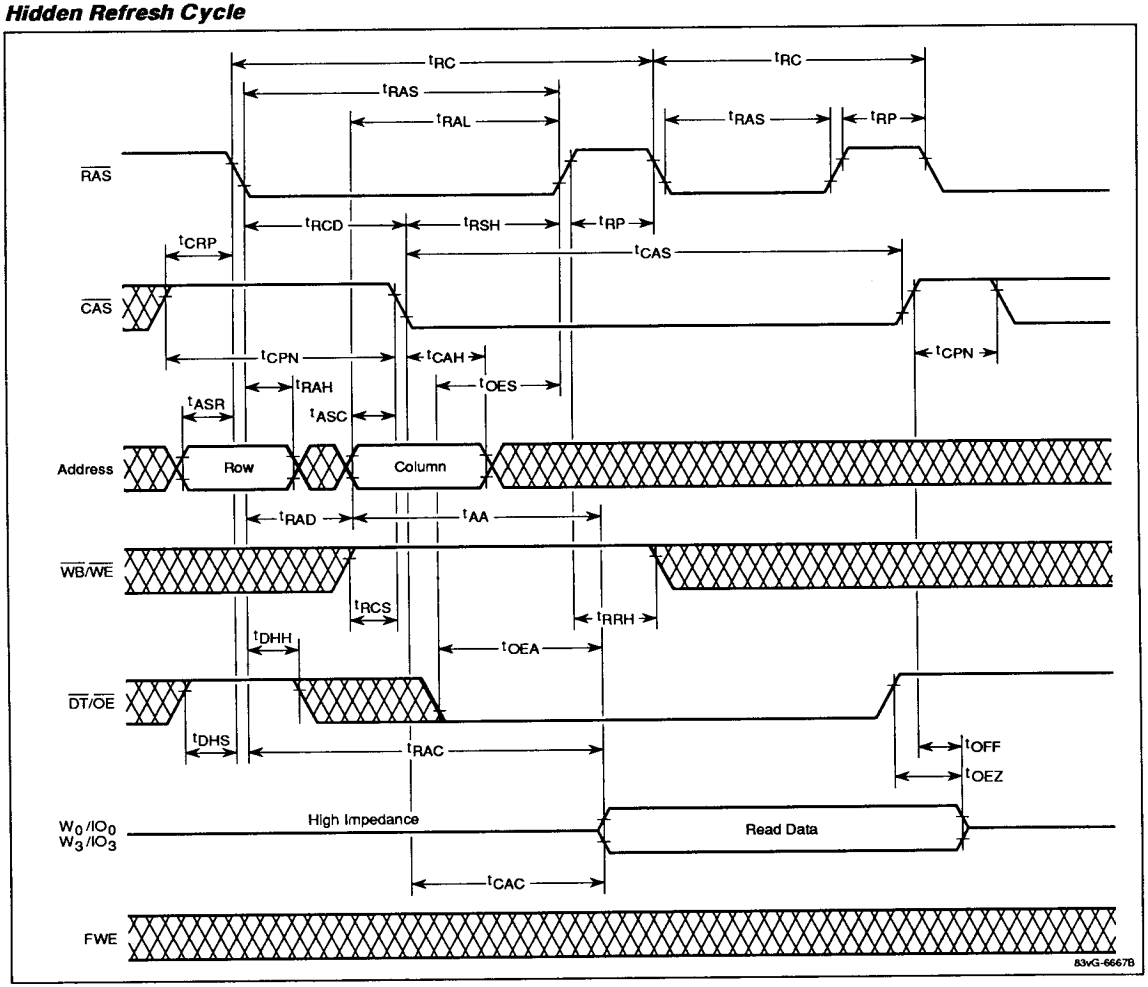
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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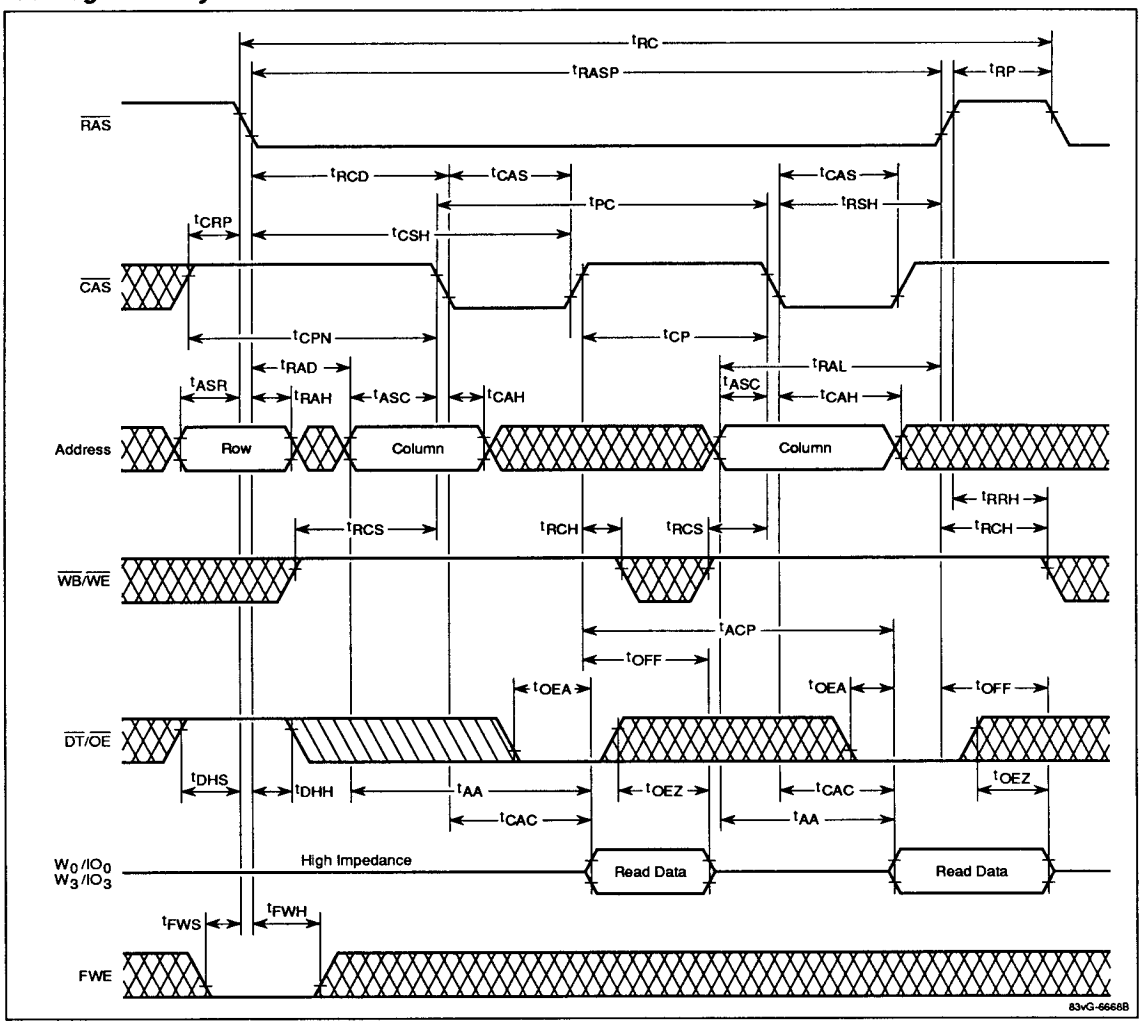
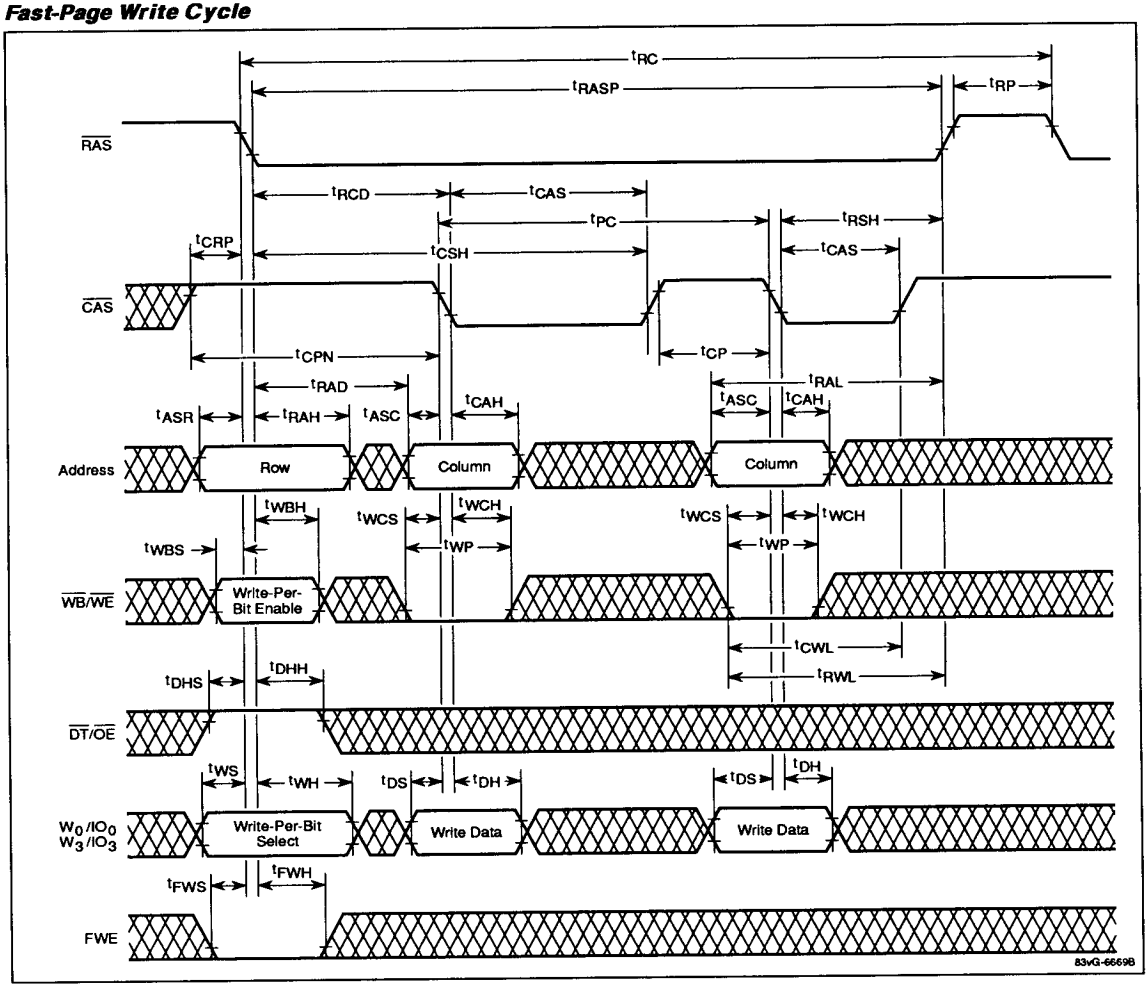
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle



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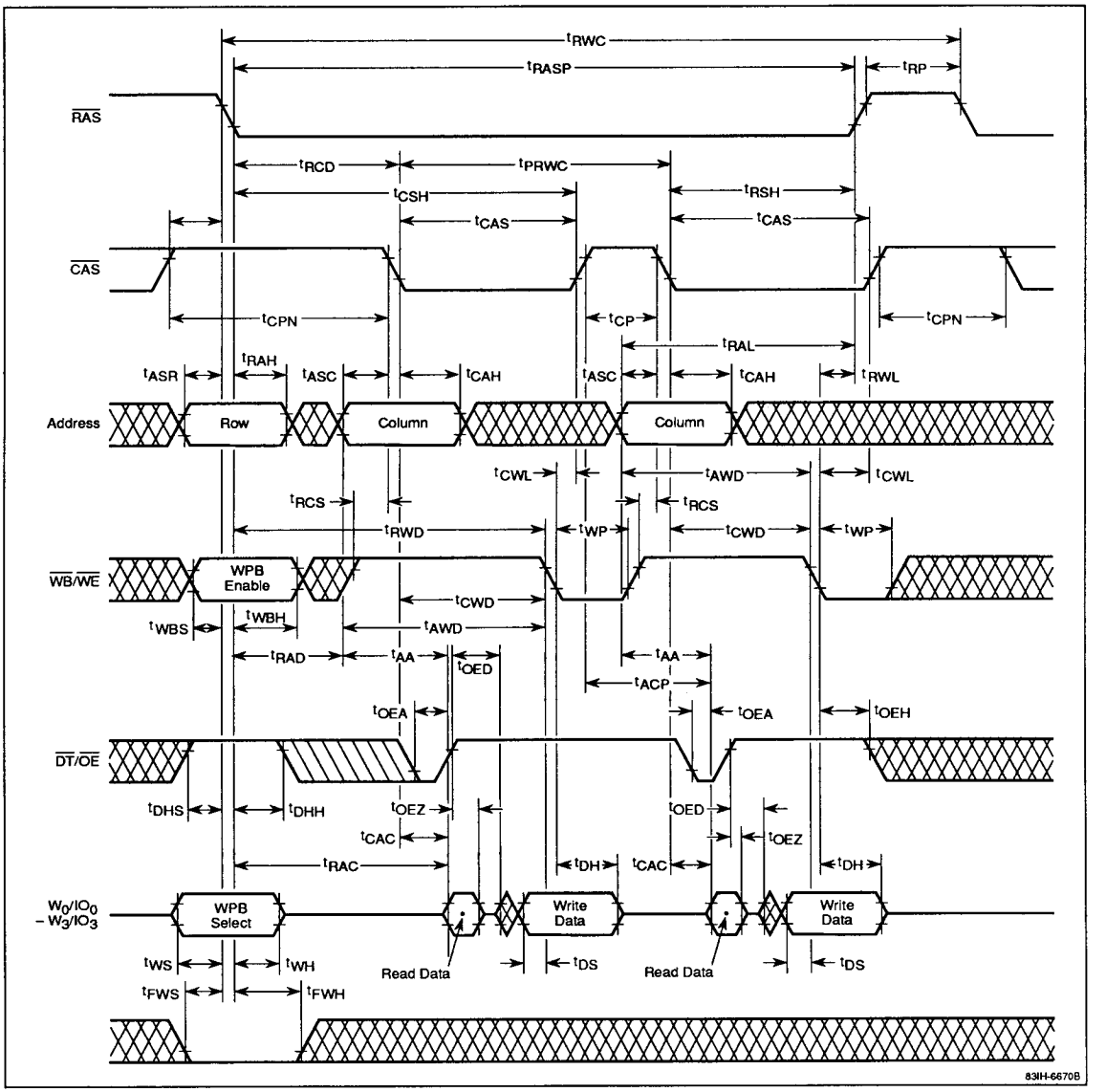
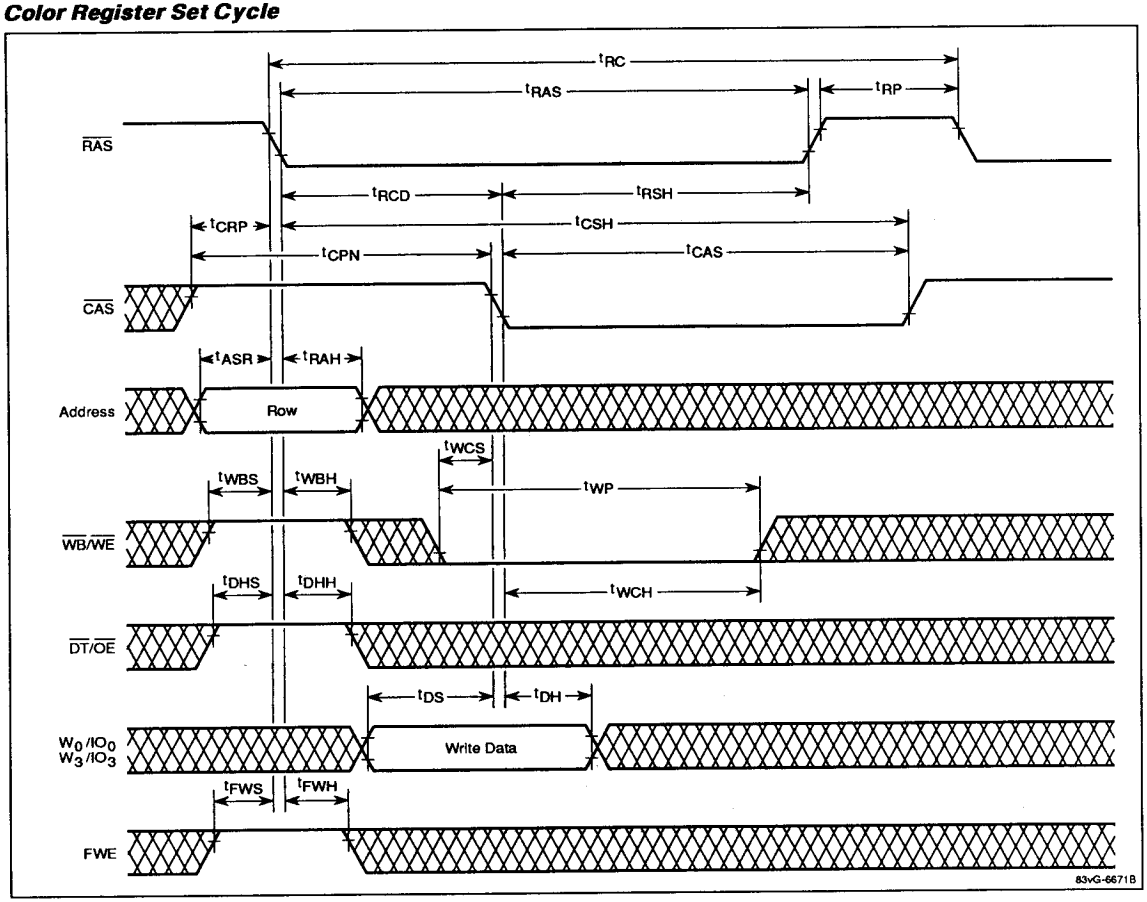
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



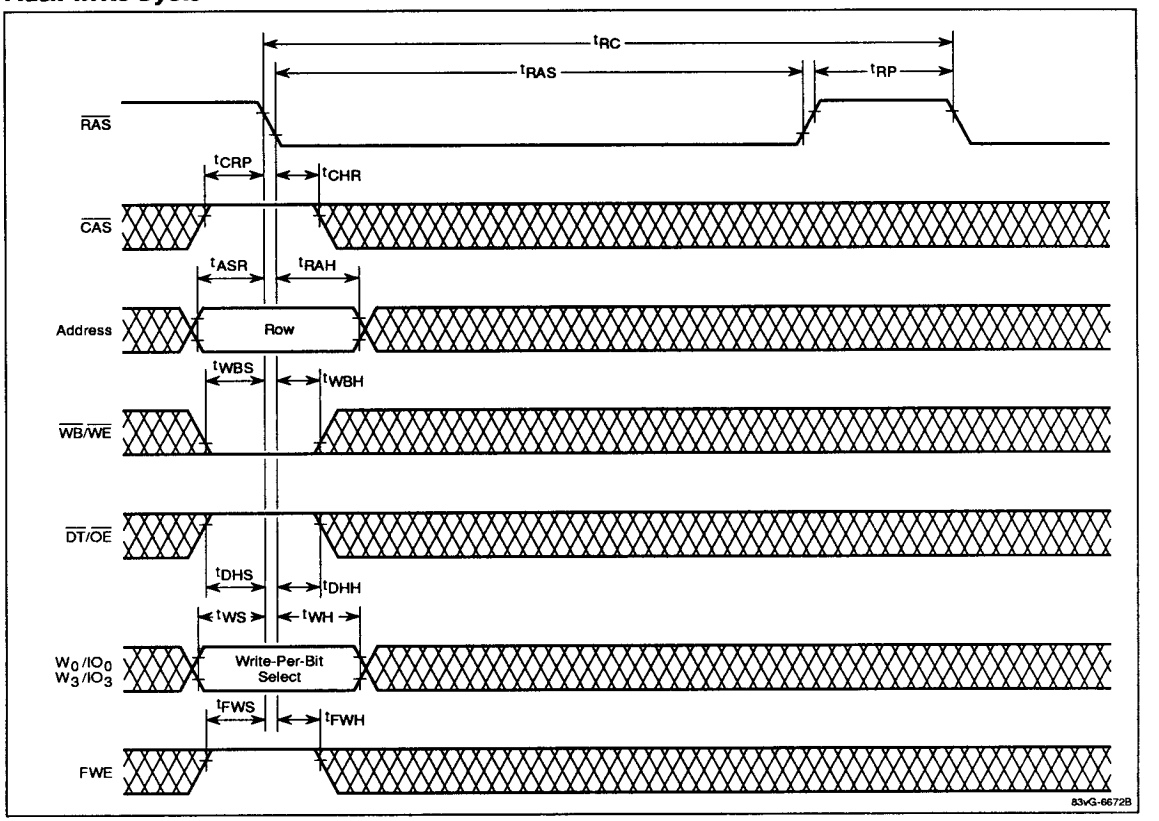
Timing Waveforms (cont)

Color Register Set Cycle



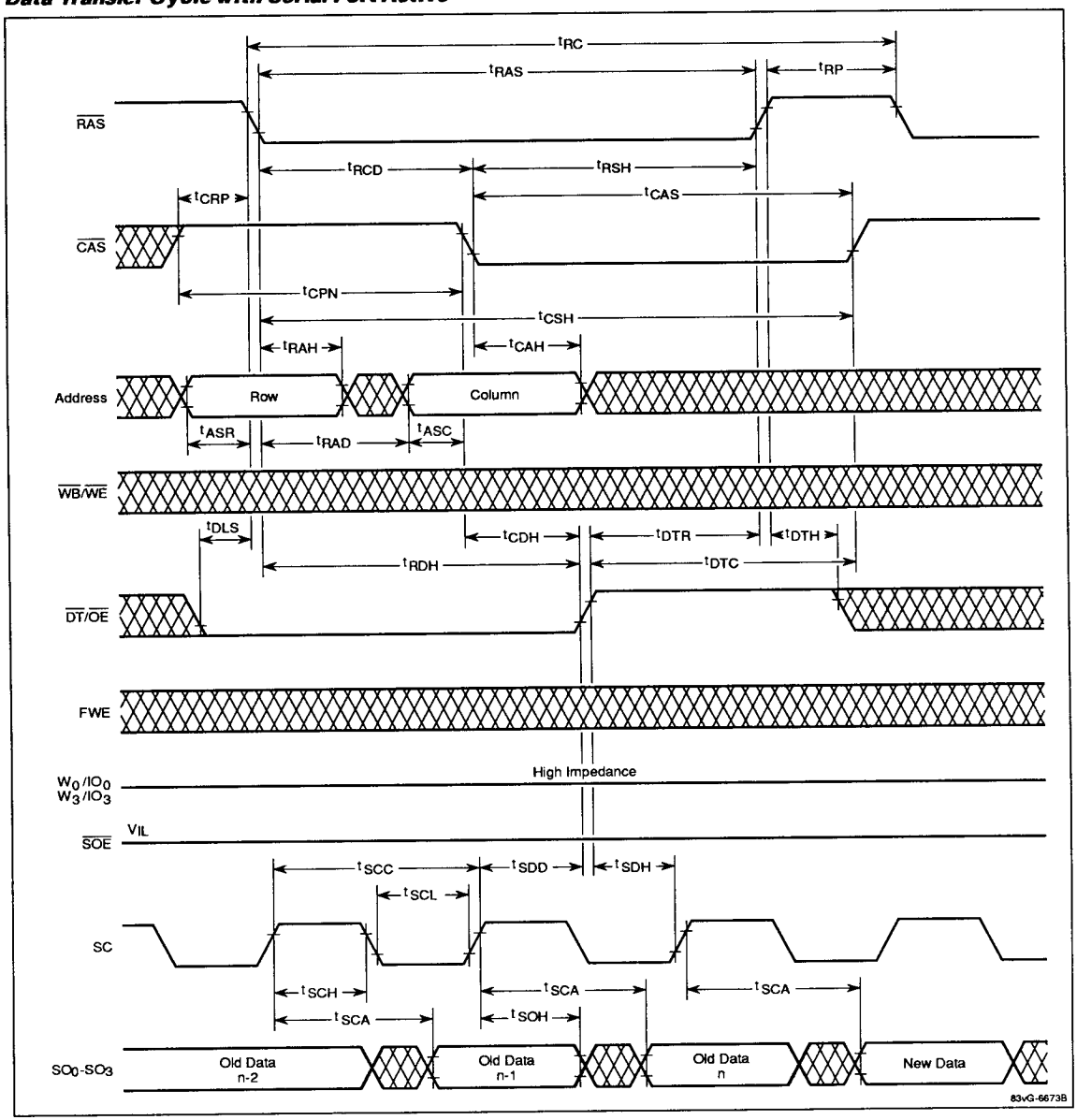
Timing Waveforms (cont)

Flash Write Cycle



Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



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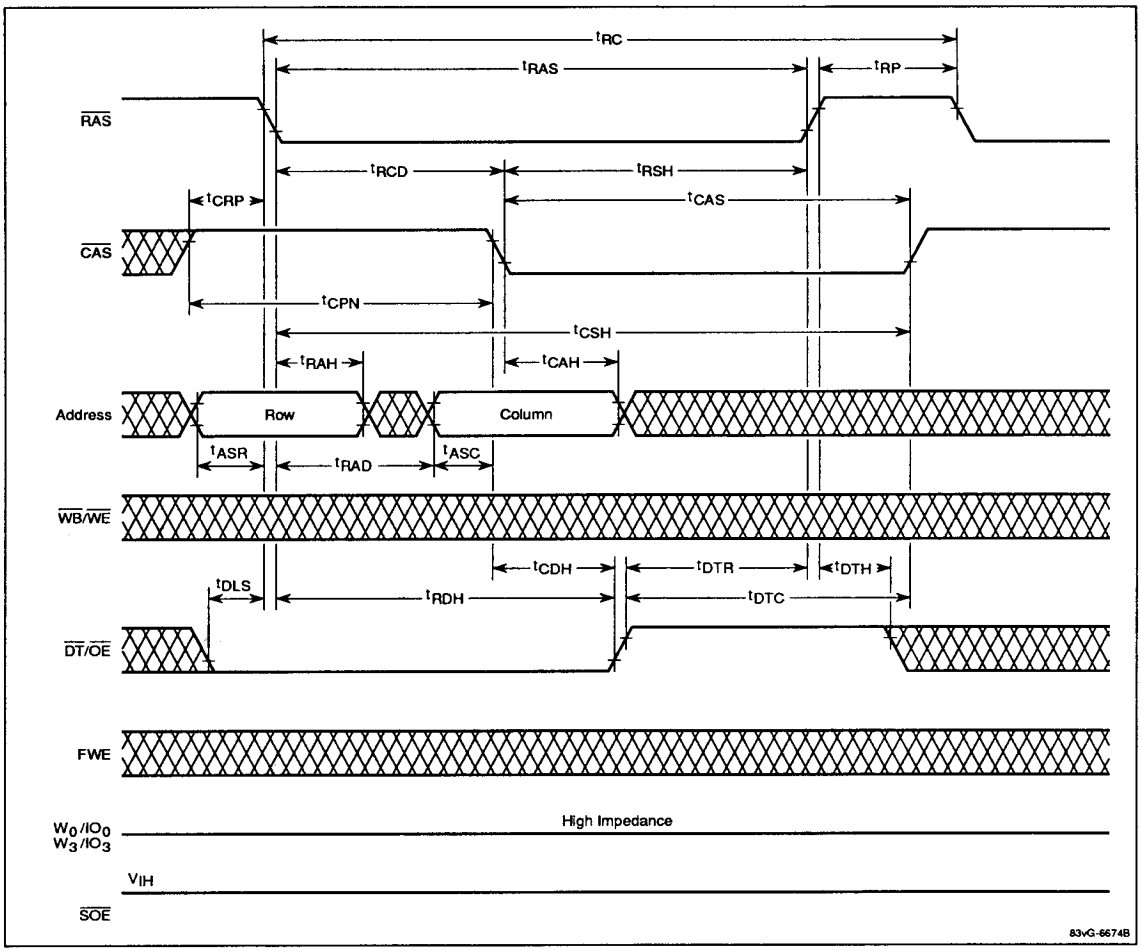
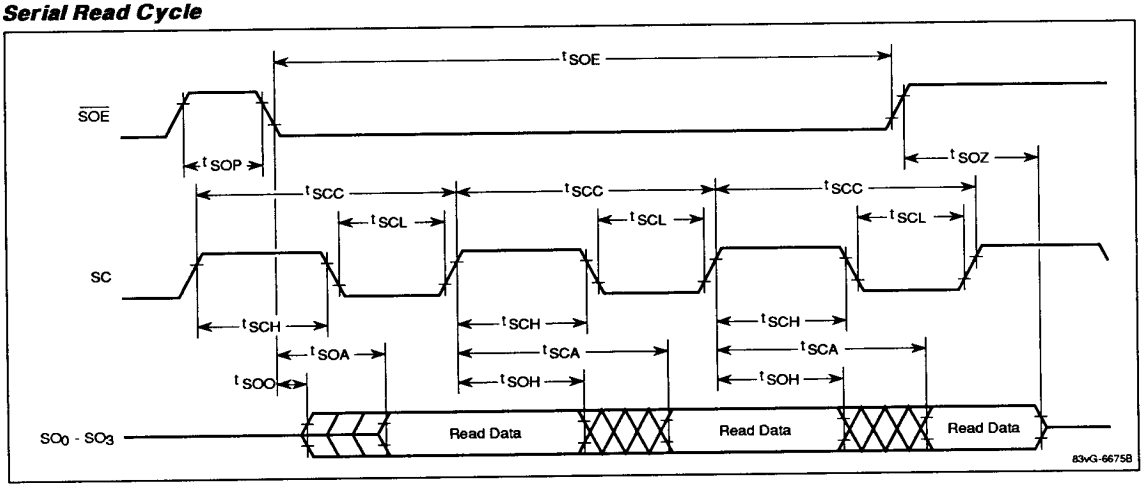
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



Timing Waveforms (cont)

Serial Read Cycle



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