Eagle SPECIFICATION

(Compact Spec. Version)

Samsung Electronics Co., LTD

Semiconductor Flash Memory Product Planning & Applications

1. FEATURES

☞ Architecture

? Design Technology : 0.25?m

? Voltage Supply

- Main : 1.8V / 2.5V
- Host Interface & NAND Flash Interface : 1.8V / 2.5V

? Organization

- Host Interface : 16-bit
- NAND Flash Interface : 8bit
- Little endian addressing

? Internal BufferRAM(4K Bytes)

- BootRAM at booting, Cache-like at normal operation

? Integrated ring oscillator providing clock for NAND Flash operations

? Voltage detector generating internal reset signal from Vcc

☞ Performance

? Host Interface type

- Synchronous Random Read
  : Clock Frequency : up to 45Mhz @30pF
- Synchronous Burst Read
  : Clock Frequency : up to 45MHz @30pF
  : Burst Length : 4words/ 8 words/ 16 words/ 32 words/ Continuous Linear Burst(2k words)
- Asynchronous Random Read
- Asynchronous Page Read : 4words
- Asynchronous Random Write

? Programmable Read latency

? Multiple Page Read

- Read multiple pages by Page Count Register(up to 8 times)

? Normal ECC mode / Bypass ECC mode is supportable

- Normal ECC mode : Hidden ECC code generation and comparison and 1bit correction
- Bypass ECC mode : Hidden ECC code generation and comparison and readable of ECC result

? Multiple Reset

- Cold Reset / Warm Reset / Hot Reset / NAND Flash Reset

? Internal Bootloader supports Booting Solution in system

? Data Protection

- Write Protection mode for BufferRAM

  : Write protection of Buffer RAM(first 2pages of Buffer RAM)

- Write Protection mode for NAND Flash

  : Block based write protection of NAND Flash

- Write protection during power-up

☞ Software

? Handshaking Feature

- INT pin : Indicates Ready/Busy of Eagle
- Polling method : Provides a software method of detecting the Ready/Busy status of Eagle

? Interface Chip ID Read

- Detailed chip information by additional controller ID register

☞ Packaging

? Package

- 64ball , 6mm X 6mm X 1.2mm FBGA

? Pin Out

Host Interface	*Flash Interface*	*Power*	*NC, DNU*	*Total pin[ea]*
35 pins	16 pins	4 pins	9 pins	64 pins

2.GENERAL DESCRIPTION

EAGLE (Flash Interface chip) allows standard NAND-flash chips to interface with Eagle bus without performance penalty. This device is 1.8V/2.5V operation and comprised of about 10,000 gates and 4KB internal BufferRAM. This 4KB BufferRAM is used as BootRAM during cold reset, and is used as cache RAM after cold reset. The operating clock frequency is up to 45MHz. This device is X16 interface with Host and X8 interface with NAND Flash. (Notice, in this specification, address is expressed by the byte order)

Also this device has the speed of ~40ns random access time. Actually, it is accessible with minimum 2clock latency(host-driven clock for synchronous read), but this device adopts the appropriate wait cycles by programmable read latency. EAGLE interface chip provides the multiple page read operation by assigning the number of pages to be read in the page counter register. The device is offered in the single type of package ; 6mmX6mmX1.2mm 64ball FBGA.

3. PIN DESCRIPTION

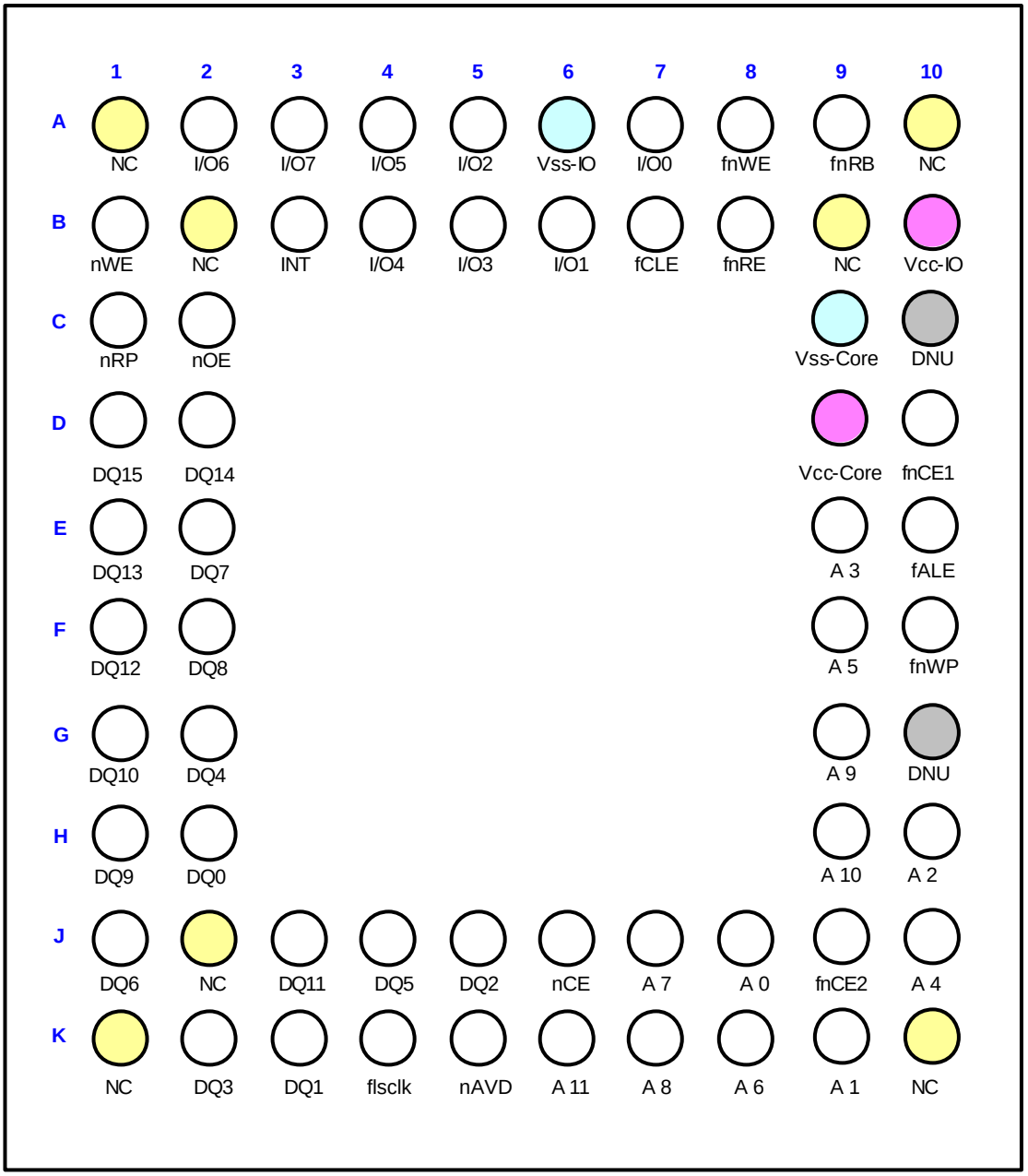
Pin Name	Type	Name and Description
Host Interface		
A11~A0	I	**Address Inputs** - Inputs for addresses during read operation, which are for addressing BufferRAM & Register .
INT	O	**Interrupt** Notifying Host when a command has completed. CMOS type driver output.
DQ15~DQ0	I/O	**Data Inputs/Outputs** - Inputs data during program and commands during all operations, outputs data during memory array/register read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled.
CLK	I	**Clock** CLK synchronizes the device to the system bus frequency in synchronous read mode. The first rising edge of FlsCLK in conjunction with nAVD low latches address input.
nWE	I	**Write Enable** nWE controls writes to the bufferRAM and registers. Datas are latched on the nWE pulse's rising edge
nAVD	I	**Address Valid Detect** Indicates valid address presence on address inputs. During asynchronous read operation, all addresses are transparent during nAVD's low, and during synchronous read operation, all addresses are latched on FlsCLK's rising edge while nAVD is held low for one clock cycle. > Low : for asynchronous mode, indicates valid address ;for burst mode, causes starting address to be latched on rising edge on FlsCLK > High : device ignores address inputs
nRP	I	**Reset Pin** When low, nRP resets internal operation of Eagle and NAND Flash. nRP status is don't care during power-up and bootloading.
nCE	I	**Chip Enable** nCE-low activates internal control logic, and nCE-high deselects the device, places it in standby state, and places A/DQ in Hi-Z

nOE	I	**Output Enable** nOE-low enables the device's output data buffers during a read cycle.
NAND Flash Interface		
I/O 0~I/O7	I/O	**Flash Input/Output** Multiplexed command/address/data bus
fnCE	O	**Flash Chip Enable** fnCE output is NAND Flash selection control. When NAND Flash is in the Busy state, fnCE high is ignored, and the device does not return to standby mode.
fnRE	O	**Flash Read Enable** fnRE output is the serial data-out control, and when active drives the data onto the NAND Flash I/O bus
fnWE	O	**Flash Write Enable** fnWE output controls writes to the NAND Flash I/O port. Commands, address and data are latched on the rising edge of the fnWE signal
fCLE	O	**Flash Command Latch Enable** fCLE output controls the activating path for commands sent to the command register of NAND Flash. When active high, commands are latched into the command register of NAND Flash through the I/O ports on the rising edge of the fnWE signal
fALE	O	**Flash Address Latch Enable** fALE output controls the activating path for address to the internal address registers of NAND Flash. Addresses are latched on the rising edge of fnWE with fALE high
fnWP	O	**Flash Write Protect** fnWP pin provides inadvertent program /erase protection during power transitions and is automatically controlled by Eagle. This pin status is activated to 'Low' only during power-up.
fR/nB	I	**Flash Ready/Busy** fR/nB input indicates the status of the NAND Flash operation. When low, it indicates that a program, erase or random read operation of NAND Flash is in process and returns to high state upon completion. It is an open drain output and 100K? pull-up resister is internally connected. So, it does not float to high-z condition when the chip is deselected or when outputs are disabled

Power Supply		
Vcc		**Power** This is the power supply for Eagle
Vss		**Ground**
etc		
DNU.		**Do Not Use** Leave it disconnected. These pins are used for testing.
NC		**No Connection** Lead is not internally connected.

NOTE : Do not leave power supply(Vcc, Vss) disconnected.

4. PIN CONFIGURATION



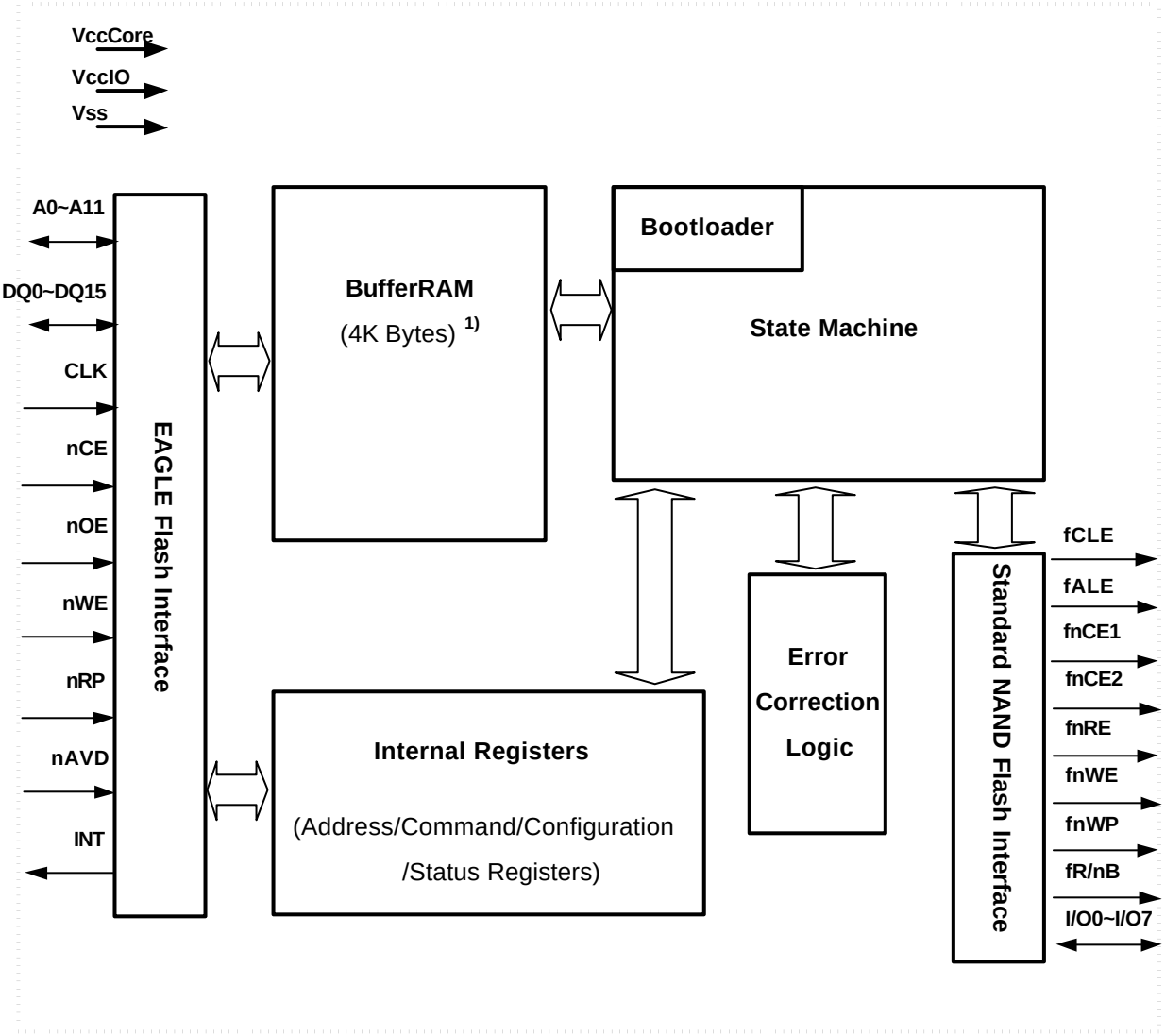
(TOPVIEW, Balls Facing Down)

64ball FBGA Eagle Chip

6 mm X 6 mm X 1.2mm , Ball Pitch : 0.5 mm

Notice: DNU (C10, G10)pins are used as test pin, so please leave these pins disconnected.

5. BLOCK DIAGRAM For Eagle Interface Chip



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- **EAGLE flash interface**
- **4KB BufferRAM**
- **Command and status registers**
- **State Machine (Bootloader is included)**
- **Error Correction Logic**
- **Standard NAND flash Interface**

Note: 1) At cold reset, bootloader copies bootcode(4K byte size) from NAND Flash to BufferRAM. and except cold reset host can use BufferRAM like cacheRAM.