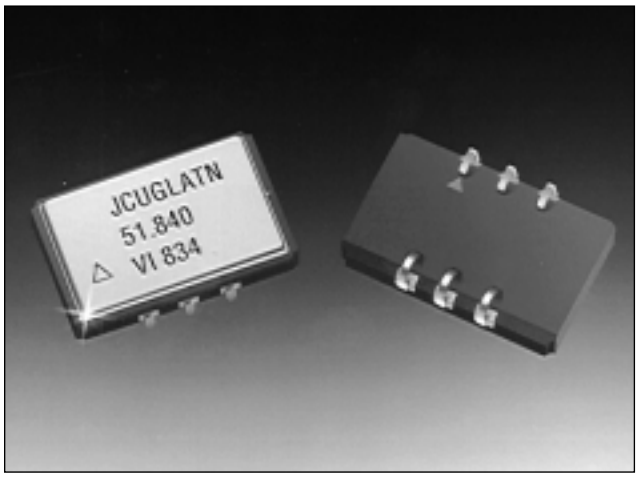
VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

J-Type
Voltage Controlled Crystal Oscillator



Features

- **Output Frequencies from 1.024 MHz to 170.000 MHz**
- **+3.3 or +5.0 volt options**
- **Small 14mm x 9mm J-type Package**
- **CMOS or PECL Outputs**
- **Low phase noise and custom options**
- **0/70° C or –40/85° C operating temperature**
- **Tri-State output (CMOS) Enable/Disable (PECL)**

Applications

- **Clock Smoothing**
- **Frequency Translation**
- **SONET, SDH, ATM, DSLAM, ADM**

Description

The J-type voltage controlled crystal oscillator incorporates VI's advanced VCXO performance capabilities while adhering to a package footprint compatible with the industry-common J-lead package.

The J-type VCXO is a quartz stabilized square wave generator with either a CMOS output for driving CMOS/TTL loads or a PECL output. The device is packaged in a 6 pin J-lead ceramic package and is hermetically sealed with a grounded conductive lid.

J-Type Voltage Controlled Crystal Oscillator

CMOS Output Option

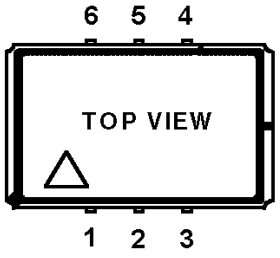
Electrical Performance @ 25°C for the CMOS output option

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage[1], +5 volt option +3.3 volt option		4.5 3.0	5.0 3.3	5.5 3.6	Vdc Vdc
Supply Current		10mA + 0.25mA per MHz, typical			
Center Frequency, *see ordering information*	FN	1.024		77.760	MHz
Operating Temperature, see ordering info	TOP	0/70, -40/85			°C
Absolute Pull Range over the operating temperature range, aging and power supply Vc=0.5 to 4.5 at 5V supply or 0.3 to 3.0 V at 3.3V supply *see ordering information for options*	APR	±50 to ±100			ppm
Gain Transfer (Frequency vs. Control Voltage)	KV	Positive			
Output Level High[2]	VOH	0.8*Vcc	-		V
Output Level Low[2]	VOL		-	0.1*Vcc	V
Output Rise/Fall Time[2]	tR/ tF			5	ns
Duty Cycle[3], *see ordering info*	SYM	45/55 or 40/60			%
Control Input Leakage	IL			1	uA
Control Voltage Modulation Bandwidth	BW	-	10	-	kHz
RMS Jitter, Output=12.0-77.760 MHz			3		ps
RMS Jitter, Output=12.0-77.760 MHz. Band=12.0 KHz - 20 MHz			<0.5		ps
Control Range		0		VDD	
Maximum Supply Voltage				7	V
Storage Temperature	TS	-55	-	125	°C
Soldering Temp./Time	TLS	-	-	220/10	°C/s

1. Power supply bypass is required and a 0.1uF in parallel with a 0.01uF high frequency capacitor is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the load used to test devices.
3. Duty cycle is defined as on-time versus period at 1.4 V for TTL, and 2.5 V for CMOS (5volt supply) and at 1.65 V for CMOS (3.3 volt operation)

Pin Out Information for the CMOS output option

Pin	Symbol	Function
1	Vc	VCXO Control Voltage.
2	Tri-State[1]	TTL logic low disables output TTL logic high, or no connect, enables output
3	GND	Case and electrical ground.
4	Output	VCXO Output
5	CMOS/TTL select[1,2]	TTL logic low optimizes symmetry for CMOS TTL logic high, or NC, optimizes symmetry for TTL.
6	VCC	Power Supply Voltage (5.0 V or 3.3V ±10%)

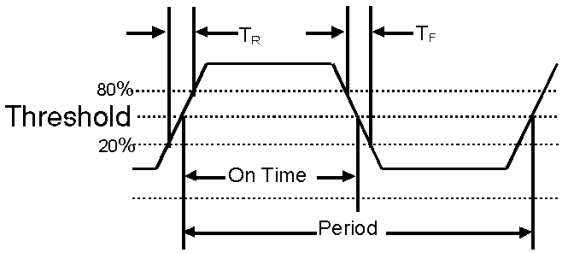


1. Standard option. Tri-State can be connected to pin 5 and CMOS/TTL select would be on pin 2.
2. Output is HCMOS. For frequencies >12MHz, this option optimizes symmetry for either CMOS or TTL thresholds. Ground this pin for frequencies < 12MHz.

J-Type Voltage Controlled Crystal Oscillator

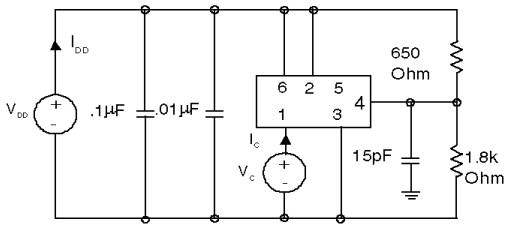
CMOS Output Option

Figure 1
Output Wave Form



Threshold = 1.4 volts for TTL and 50% for CMOS

Figure 2
Output Test Conditions



Output Test Conditions (25±5°C) for 5 volt devices. For 3.3V use 15pF cap only, no resistors needed.

Ordering Information for the CMOS output option (add frequency)[4]

Package		Supply Voltage		VCXO Type		APR (ppm)		Operating Temp. (°C)		Output/Duty Cycle Min/Max		Tri-State		Specials	
J	6 pin Ceramic SOJ	C	5V±10%	U	VCXO	G	±50	C	0/70	A	TTL/ CMOS 45/55%[1]	T	Tri State on pin 2	N	Standard
		D	3.3V±10%	L	±10% linear VCXO	N	±80	L	-40/85	J	CMOS 45/55%[2]				
						H	±100			K	CMOS 40/60%[3]				

1. Output is CMOS and symmetry is tested at TTL and CMOS thresholds.
2. Output is CMOS and symmetry is tested at CMOS threshold. This option is used for 3.3 V operation.
3. Output is CMOS and symmetry is tested at CMOS thresholds. This option is required for 3.3V, frequencies >51.840MHz.
4. Note: Not all combinations are possible.

Example: JDUGCKTN @ 77.76 MHz = 3.3 volt, VCXO@77.760, ±50 ppm APR, 0/70°C, 40/60% Symmetry, CMOS, Tri-State on pin 2.

Standard Frequencies, in MHz, for CMOS output option

1.024	1.544	2.000	2.048	3.088	3.580
3.686	4.000	4.032	4.096	4.434	5.000
6.144	6.176	6.312	6.400	8.000	8.192
8.448	10.000	12.000	12.288	12.352	13.000
14.318	15.360	15.440	16.000	16.384	18.432
19.44	20.000	20.480	24.000	24.576	24.704
27.000	30.000	32.000	32.768	34.368	35.328
38.880	40.000	40.960	44.736	50.000	51.840
52.000	65.536	77.760	155.520[1]		

1. Uses a PLL multiplier, jitter is 25ps rms typical vs 3ps rms typical for a HFF (High Frequency Fundemental) design. Available with 5 Vdc input only.

Other frequencies available upon request.

J-Type Voltage Controlled Crystal Oscillator

PECL Output Option

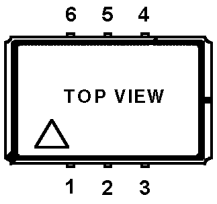
Electrical Performance @ 25°C for the PECL output option

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage[1], +5 volt option +3.3 volt option		4.5 3.0	5.0 3.3	5.5 3.6	Vdc Vdc
Supply Current (frequency dependent)				<65mA	
Center Frequency, *see ordering information*	FN	15		170	MHz
Operating Temperature, see ordering info	TOP	0/70, -40/85			°C
Absolute Pull Range over the operating temperature range, aging and power supply Vc= 0.5 to 4.5 at 5V supply or 0.3 to 3.0 V at 3.3 supply *see ordering information for options*	APR	±32 to ±50			ppm
Gain Transfer (Frequency vs. Control Voltage)	KV	Positive			
Output Level High[2] (0/70°C)	VOH	Vcc-1.025	-	Vcc-0.880	V
Output Level Low[2] (0/70°C)	VOL	Vcc-1.810	-	Vcc-1.620	V
Output Level High[2] (-40/+85°C)	VOH	Vcc-1.085	-	Vcc-0.880	V
Output Level Low[2] (-40/+85°C)	VOL	Vcc-1.830	-	Vcc-1.555	V
Output Rise/Fall Time[2]	tR/ tF			1	ns
Duty Cycle	SYM			45/55	%
Control Input Leakage	IL			0.1	mA
Control Voltage Modulation Bandwidth	BW	10			kHz
RMS Jitter		*see ordering information*			ps
RMS Jitter, 155.52 MHz, 12 kHz to 20 MHz (option P)			0.5	1.0	ps
Maximum Control Voltage		0		VDD	
Maximum Supply Voltage				7	V
Storage Temperature	TS	-55	-	125	°C
Soldering Temp./Time	TLS	-	-	220/10	°C/s

1. Power supply bypass is required and a 0.1uF in parallel with a 0.01uF high frequency capacitor is recommended.
2. Transition times are measured from 20% to 80% of a full 10K ECL level swing.

Pin Out Information for the PECL output option

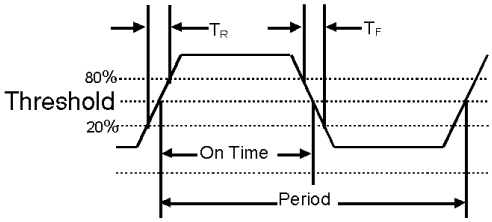
Pin	Symbol	Function
1	Vc	VCXO Control Voltage.
2	N/C or E/D[1]	No Connect or Output Disable option
3	GND	Case and electrical ground.
4	Output	VCXO Output
5	C_{Output}	VCXO Complementary Output
6	V_{CC}	Power Supply Voltage (5.0 V or 3.3V ±10%)



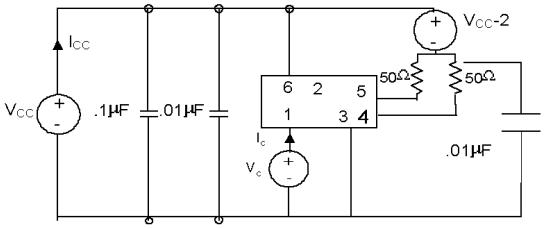
1. By setting pin 2 high, the outputs are disabled and output on pin 4 is held low while Complementary output on pin 5 is held high. Output is enabled by setting pin 2 at < Vcc -1.6V, See ordering information for enable/disable option.

PECL Output Option

Output Wave Form



Output Test Conditions



Output Test Conditions (25±5°C)

Ordering Information for the PECL output option (add frequency) [1]

Package		Supply Voltage		VCXO Type		APR (ppm)		Operating Temp. (°C)		Output/Duty Cycle Min/Max		Enable/ Disable		Specials	
J	6 pin Ceramic SOJ	C	5V±10%	U	VCXO	F	±32	C	0/70	M	PECL 45/55%	U	None	N	Standard
		D	3.3V±10%	L	±10% linear VCXO	G	±50	L	-40/85			E	Enable/ Disable on pin 2	P	6ps rms (<1ps rms 12 kHz-20 MHz) jitter
				M	±20ppm stability VCXO									R	12ps rms jitter
														T	20ps rms jitter

1. Note: Not all combinations are possible.

Example: JDUGLMEP @77.76 MHz = 3.3 volt, VCXO @77.760, ±50 ppm APR, -40/85°C, 45/55% Symmetry, PECL, Enable/Disable on pin 2, 6ps rms jitter

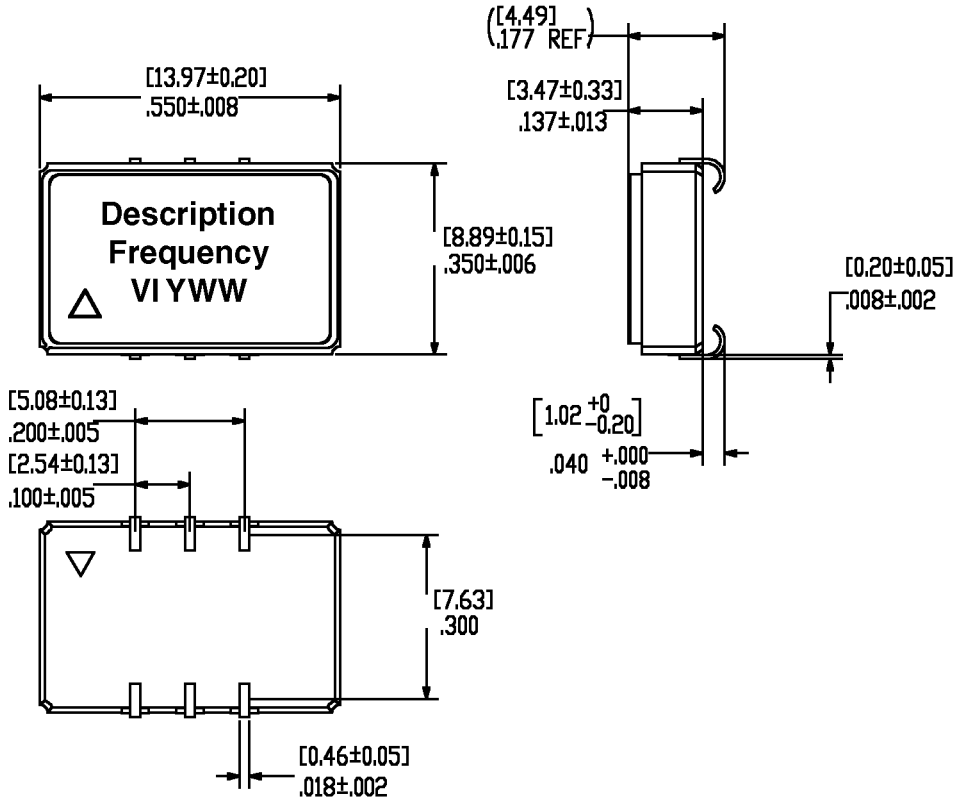
Standard Frequencies, in MHz, for PECL output options

77.760	82.944	155.52

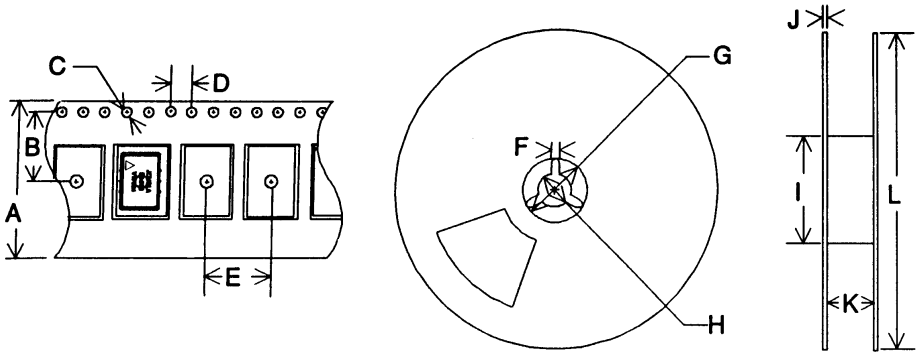
Other frequencies available upon request.

J-Type Voltage Controlled Crystal Oscillator

Outline Drawing



Tape and Reel

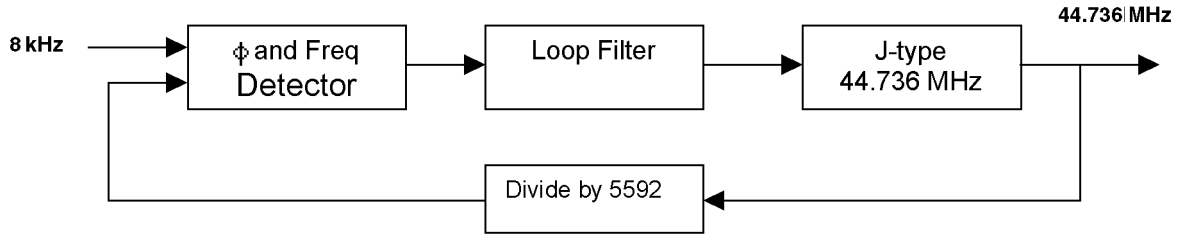


Tape and Reel Dimensions (mm)

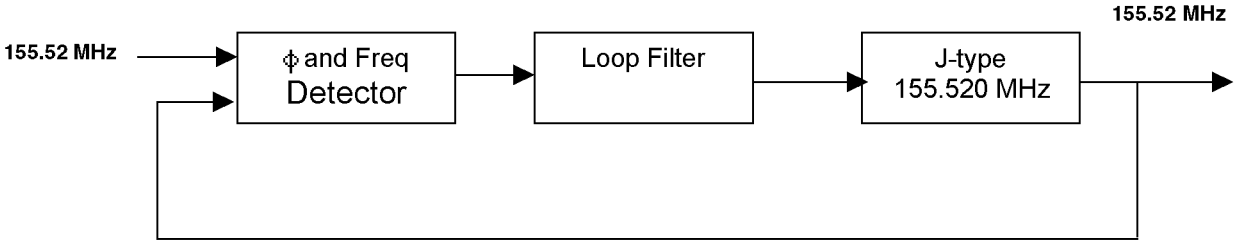
Tape Dimensions						Reel Dimensions							# Per Reel
Product	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**	
J-Type	24	11.5	1.5	4	12	1.78	21	13	100	5	25	330	200

J-Type Voltage Controlled Crystal Oscillator

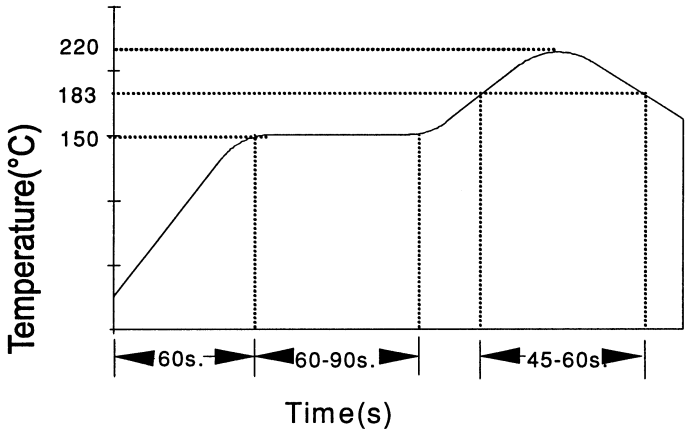
Typical Frequency Translation Diagram



Typical Clock Smoothing Diagram



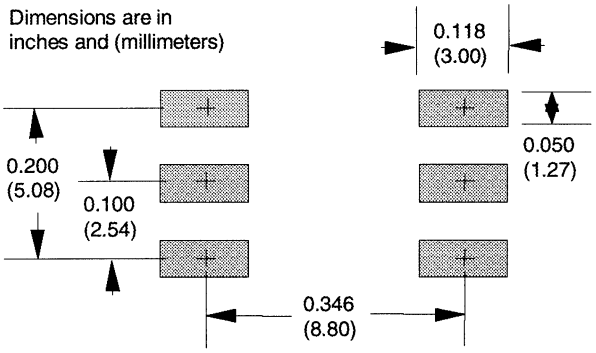
Recommended Solder Reflow Profile



Suggested IR profile

VI qualification includes aging at various extreme temperatures, shock and vibration; temperature cycling and IR reflow simulation. The conditions a device can withstand are well understood and devices can be subjected to the profile in figure above. This profile shows a ramp up condition to prevent thermal shock, a preheat period in which the flux is activated, a ramp up to 183° C which is the eutectic temperature of Sn/Pb and a gradual cool down. The time above 183° C should not exceed 60 seconds and the peak temperature should be no more than 220° C for 10 seconds. The J-types are 100% screened for hermeticity so an aqueous wash is not an issue.

Recommended Solder Pad Layout



Mechanical and Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, 2002
Mechanical Vibration	MIL-STD-883, 2007
Solderability	MIL-STD-883, 2003
Gross and Fine Leak	MIL-STD-883, 1014
Resistance to Solvents	MIL-STD-883, 1016

Handling Precautions

Although ESD protection circuitry has been designed into the the J-type, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

ESD Ratings

Model	Minimum
Human Body Model	1500V
Charged Device Model	1500V

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USA: Vectron International • 166 Glover Avenue, Norwalk, CT 06856 . . . . **Tel: 1-88-VECTRON-1 • Fax: 1-888-FAX-VECTRON**
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