

Very High Speed 2K (6K) Gate CMOS FPGA

Features

- Very high speed
 - Loadable counter frequencies greater than 150 MHz
 - Chip-to-chip operating frequencies up to 85 MHz
 - Input + logic cell + output delays under 9 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
 - 12 x 16 array of 192 logic cells provides 6,000 total available gates
 - 2,000 typically usable "gate array" gates in 68- and 84-pin PLCC, 84-pin CPGA, and 100-pin TQFP packages
- Low power, high output drive
 - Standby current typically 2 mA
 - 16-bit counter operating at 100 MHz consumes 50 mA
 - Minimum I_{OL} of 12 mA and I_{OH} of 8 mA
- Flexible logic cell architecture
 - Wide fan-in (up to 14 input gates)
 - Multiple outputs in each cell
 - Very low cell propagation delay (1.7 ns)
- Powerful design tools—*Warp3*™
 - Designs entered in VHDL, schematics, or both

- Fast, fully automatic place and route
- Waveform simulation with back annotated net delays
- PC and workstation platforms
- Robust routing resources
 - Fully automatic place and route of designs using up to 100 percent of logic resources
 - No hand routing required
- 56 (CY7C383A) to 68 (CY7C384A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
 - Clock skew < 1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
 - Built-in scan path permits 100 percent factory testing of logic and I/O cells
 - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- CMOS process with ViaLink™ programming technology
 - High-speed metal-to-metal link
 - Non-volatile antifuse technology
- 68-pin PLCC is compatible with CY7C382A footprint for easy upgrade
- 84-pin PLCC is compatible with ACT1020 power supply and ground pinouts

Functional Description

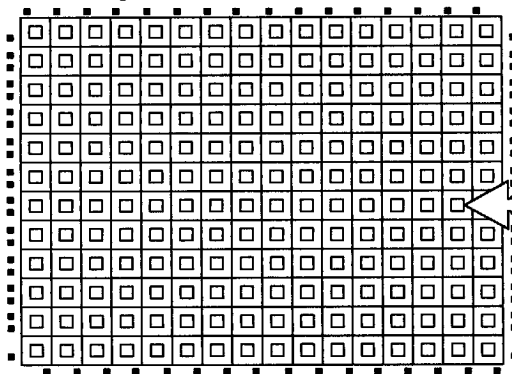
The CY7C383A and CY7C384A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 192 logic cell field-programmable gate array (FPGA) offers 2,000 typically usable "gate array" gates. This is equivalent to 6,000 EPLD or LCA gates. The CY7C383A is available in a 68-pin PLCC. The CY7C384A is available in an 84-pin PLCC and CPGA and 100-pin TQFP.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input delays under 1.5 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

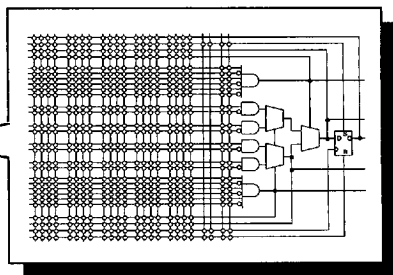
Designs are entered into the CY7C383A and CY7C384A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C383A and CY7C384A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



■ I/O/HIGH-DRIVE INPUT/CLOCK CELLS



68 or 84 PINS, INCLUDING 68 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS

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Warp3 is a trademark of Cypress Semiconductor Corporation.

Pin Configurations (continued)
CPGA
Bottom View

I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	A
I/O	I/O	I/O	I/O	I/(BCLK)	I/(P)	I	I/O	I/O	I/O	I/O	B
I/O	I/O			V _{SS}	I/CLK (SM)	V _{CC}			I/O	I/O	C
I/O	I/O								I/O	I/O	D
I/O	I/O	V _{CC}						V _{SS}	I/O	I/O	E
I/O	I/O	I/O						I/O	I/O	I/O	F
I/O	I/O	V _{SS}						V _{CC}	I/O	I/O	G
I/O	I/O								I/O	I/O	H
I/O	I/O			V _{CC}	I/CLK	V _{SS}			I/O	I/O	J
I/O	I/O	I/O	I/O	I/(SO)	I	I/(SI)	I/O	I/O	I/O	I/O	K
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature

Ceramic -65°C to +150°C
 Plastic -40°C to +125°C

Lead Temperature 300°C

Supply Voltage -0.5V to +7.0V

Input Voltage -0.5V to $V_{CC} + 0.5V$

ESD Pad Protection $\pm 2000 V$

DC Input Voltage $\pm 20 mA$

Latch-Up Current $\pm 200 mA$

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V $\pm$ 5%
Industrial	-40°C to +85°C	5V $\pm$ 10%
Military	-55°C to +125°C	5V $\pm$ 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
-0	0.39	1.82	0.4	1.67	0.46	1.55
-1	0.39	1.56	0.4	1.43	0.46	1.33
-2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0 mA$	3.7		V
		$I_{OH} = -8.0 mA$	2.4		V
		$I_{OH} = -10.0 \mu A$	$V_{CC} - 0.1$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12 mA$ Commercial		0.4	V
		$I_{OL} = 8.0 mA$ Military/Industrial			V
		$I_{OL} = 10.0 \mu A$		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}	-10	+10	μA
I_{OZ}	Output Leakage Current—Three-State	$V_{IN} = V_{CC}$ or V_{SS}	-10	+10	μA
I_{OS}	Output Short Circuit Current	$V_{OUT} = V_{SS}$	-10	-80	mA
		$V_{OUT} = V_{CC}$	30	140	mA
I_{CC}	Standby Supply Current	$V_{IN}, V_{I/O} = V_{CC}$ or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance ⁽¹⁾	$T_A = 25^\circ C, f = 1 MHz,$ $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. $C_{IN} = 40 pF$ max. on I(SI) and I(P).

Switching Characteristics Over the Operating Range

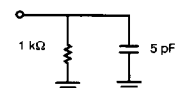
Parameter	Description	Propagation Delays ^[2] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t _{PD}	Combinatorial Delay ^[3]	1.7	2.2	2.6	3.2	5.2	ns
t _{SU}	Set-Up Time ^[3]	2.1	2.1	2.1	2.1	2.1	ns
t _H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t _{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.5	4.6	ns
t _{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t _{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t _{SET}	Set Delay	1.7	2.1	2.6	3.2	5.2	ns
t _{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.3	ns
t _{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t _{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays ^[2]						Unit
		1	2	3	4	6	8	
INPUT CELLS								
t _{IN}	Input Delay (HIGH Drive)	2.4	2.5	2.6	2.7	3.0	3.3	ns
t _{INI}	Input, Inverting Delay (HIGH Drive)	2.5	2.6	2.7	2.8	3.1	3.6	ns
t _{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.8	3.7	4.6	ns
t _{GCK}	Clock Buffer Delay ^[4]	2.7	2.8	2.8	2.9	2.9	3.0	ns
t _{GCKHI}	Clock Buffer Min. HIGH ^[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t _{GCKLO}	Clock Buffer Min. LOW ^[4]	2.0	2.0	2.0	2.0	2.0	2.0	ns

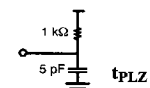
Parameter	Description	Propagation Delays ^[2] with Output Load Capacitance (pF) of					Unit
		30	50	75	100	150	
OUTPUT CELLS							
t _{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t _{OUTH}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t _{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t _{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t _{PHZ}	Output Delay HIGH to Three-State ^[5]	2.9					ns
t _{PLZ}	Output Delay LOW to Three-State ^[5]	3.3					ns

Notes:

- Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
- These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
- Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
- The following loads are used for t_{PHZ}:



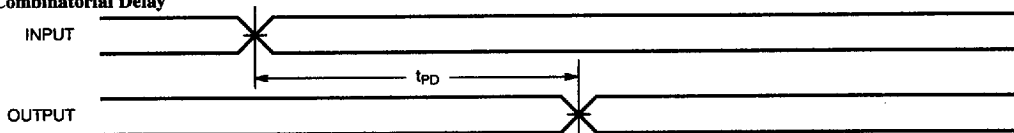
t_{PHZ}



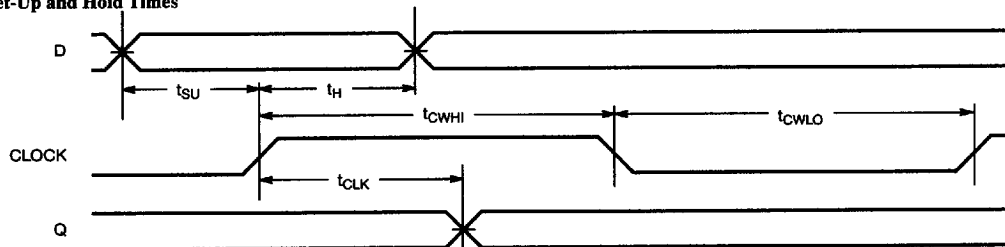
t_{PLZ}

High Drive Buffer

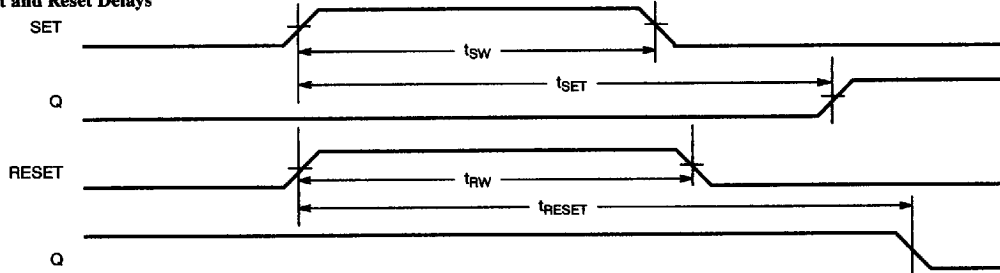
Parameter	Description	# High Drives Wired Together	Propagation Delays ^[2] with Fanout of					Unit
			12	24	48	72	96	
t_{IN}	High Drive Input Delay	1	4.5	5.4				ns
		2		3.9	5.6			ns
		3			4.5	5.3	6.3	ns
		4				4.6	5.3	ns
t_{INI}	High Drive Input, Inverting Delay	1	4.7	5.6				ns
		2		4.0	5.8			ns
		3			4.6	5.5	6.4	ns
		4				4.8	5.5	ns

Switching Waveforms
Combinatorial Delay


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Set-Up and Hold Times


c383A-7

Set and Reset Delays


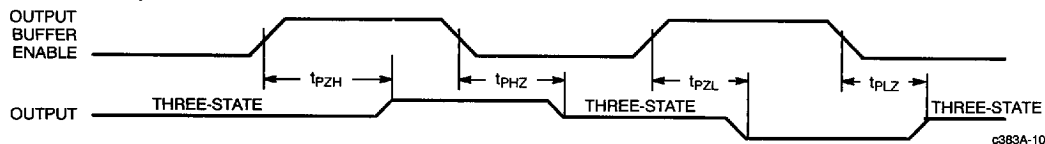
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Output Delay


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Switching Waveforms (continued)

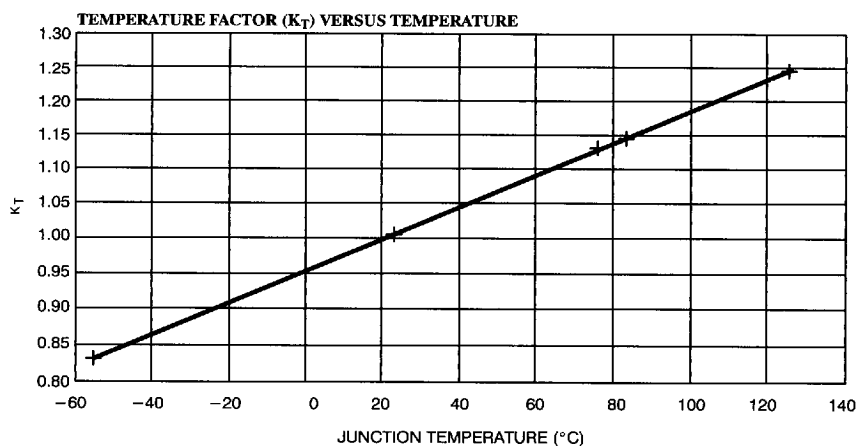
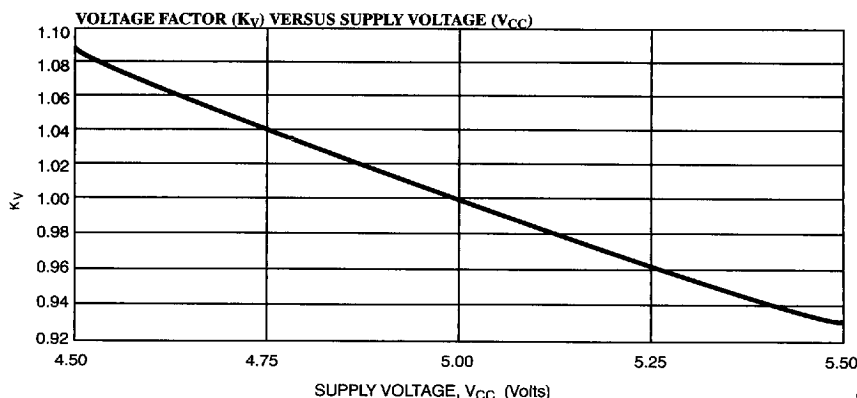
Three-State Delay



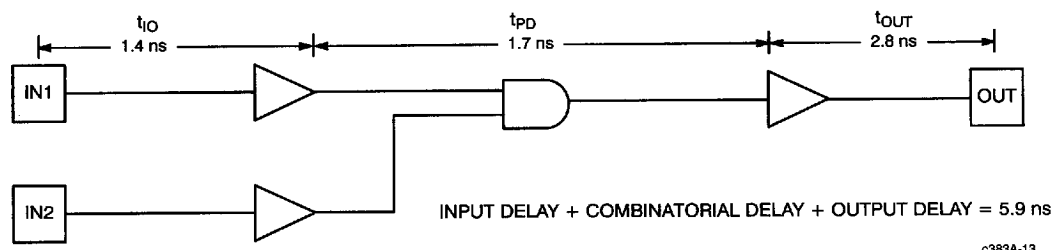
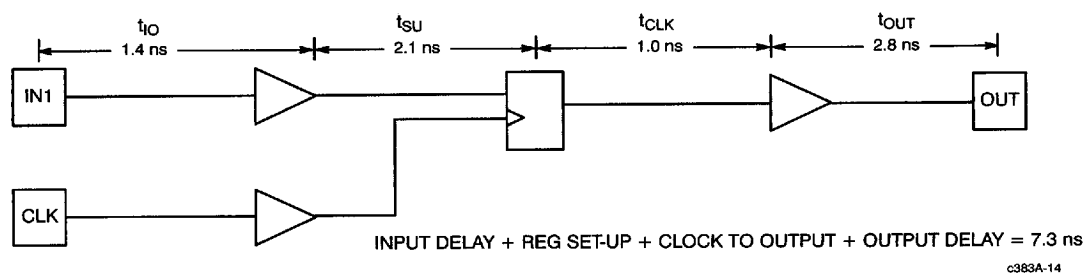
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K , as specified by the speed grade in the Delay

Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



* $\theta_{JA} = 45^\circ\text{C/WATT}$ FOR PLCC

Combinatorial Delay Example (Load = 30 pF)

Sequential Delay Example (Load = 30 pF)


Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C383A-2JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A-2JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
1	CY7C383A-1JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A-1JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C383A-0JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C383A-0JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C384A-2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A-2GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-2JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A-2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A-2GI	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-2JI	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C384A-1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A-1GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A-1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A-1GI	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C384A-1GMB	G84	84-Pin Grid Array (Cavity Up)	Military
	CY7C384A-0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C384A-0GC	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A-0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C384A-0GI	G84	84-Pin Grid Array (Cavity Up)	
	CY7C384A-0JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C384A-0GMB	G84	84-Pin Grid Array (Cavity Up)	Military

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC1}	1, 2, 3

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