ADS-105, ADS-106
12-BIT, 1 MHz
SAMPLING A/D CONVERTERS

FEATURES

- **12-Bit resolution**
- **1 MHz throughput**
- **15 Megohm input impedance**
- **Includes fast Sample/Hold amplifier**
- **3-State output, TTL and CMOS compatible**

GENERAL DESCRIPTION

The ADS-105 and ADS-106 provide high-speed, highly accurate, multiple sample digitization of sinusoidal signals. These devices use a two-pass, digitally correcting subranging architecture. Both models have an analog-to-digital (A/D) converter and a sample-and-hold amplifier (S/H). Combining both the A/D and S/H in one device eliminates critical layout problems assuring stable, high-bandwidth operation.

The ADS-105 accepts unipolar analog inputs (0 to +10V) while the ADS-106 accepts full scale bipolar inputs (±10V).

The ADS-105/-106 offer outstanding high speed analog performance. Maximum differential linearity error is 0.025% FSR ±1/2 LSB of full scale (0 °C to +70 °C).The maximum gain temperature coefficient is ±35 ppm of FSR/°C. Both models guarantee no missing codes over the full -55 °C to +125 °C operating temperature range.

Dynamic specifications include a total sampling rate of 1 MHz for sinusoidal signals which do not exceed the internal bandwidth, settling, and slew rate specifications. The input bandwidth of the S/H accepts sinusoidal signals up to 40 KHz (10V peak to peak) with -70 dB typical harmonic distortion.

Applications for the ADS-105/106 include data acquisition and control systems, array processing, vibration and resonance analysis, medical imaging and scanning, communications signal processing, noise and spectrum analyzers, and video processing.

For high-reliability versions of either the ADS-105 or the ADS-106, contact the factory.

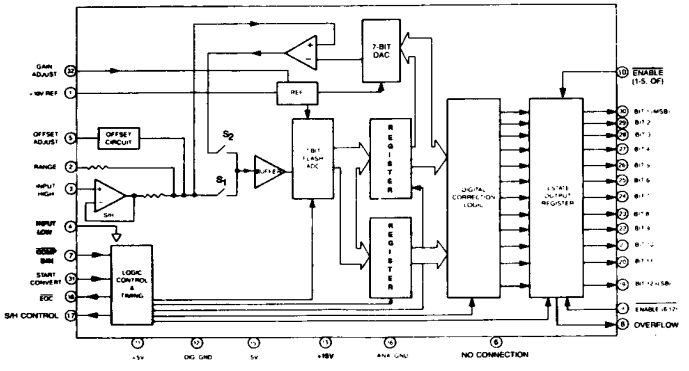
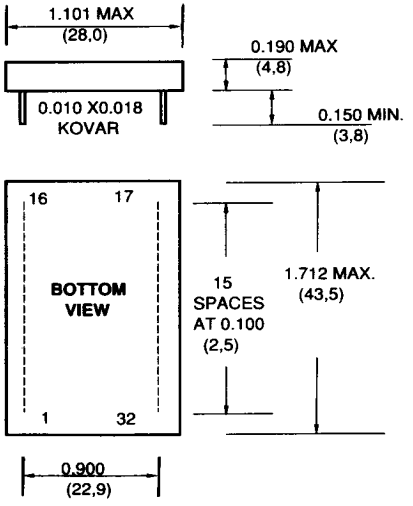


Figure 1. ADS-105, ADS-106 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF OUT
2	RANGE IN
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST IN
6	NO CONNECTION
7	COMP BIN IN
8	OVERFLOW OUT
9	ENABLE (6-12) IN
10	ENABLE (1-5 O.F.) IN
11	+5V POWER IN
12	DIGITAL GROUND
13	+15V POWER IN
14	-15V POWER IN
15	-5V POWER IN
16	ANALOG GROUND
17	S/H CONTROL OUT
18	EOC OUT
19	BIT 12 (LSB) OUT
20	BIT 11 OUT
21	BIT 10 OUT
22	BIT 9 OUT
23	BIT 8 OUT
24	BIT 7 OUT
25	BIT 6 OUT
26	BIT 5 OUT
27	BIT 4 OUT
28	BIT 3 OUT
29	BIT 2 OUT
30	BIT 1 (MSB) OUT
31	START CONVERT IN
32	GAIN ADJUST IN

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 13)	0 to +18	Volts dc
-15V Supply (Pin 14)	0 to -18	Volts dc
+5V Supply(Pin 11)	-0.5 to +7	Volts dc
-5V Supply (Pin 15)	+0.5 to -7	Volts dc
Digital Inputs (Pins 7, 9, 10, and 31)	-0.3 to +5.5	Volts dc
Analog Input	-15 to +15	Volts dc
Lead temp. (10 sec.)	300	°C max.

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range				
ADS-105	–	0 to +10	–	Volts
ADS-106	–	±10	–	Volts
Input Impedance				
Resistance	5	15	–	M Ohms
Capacitance	–	5	7	pF
Input Bias Current	–	±20	±500	nA
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA

SAMPLE/HOLD SPECIFICATIONS	MIN.	TYP.	MAX.	UNITS
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty (Jitter)	–	±100	–	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec.
0 °C to +70 °C	–	–	765	nSec.
-55 °C to +125 °C	–	–	900	nSec.
Sinusoidal Input	–	–	395	nSec.

APPLICATIONS

- **High-speed Data Acquisition and Control Systems**
- **Array Processing, Vibration and Resonance/ transient Analysis**
- **Medical Imaging and Scanning**
- **Communications Signal Processing**
- **Spectrum and Noise Analyzers**
- **Video Processing Systems**

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Integral Nonlinearity				
+25 °C	–	–	±0.0125	%FSR ±1/2LSB
0 °C to +70 °C	–	–	±0.0125	%FSR ±1/2LSB
-55 °C to +125 °C	–	–	±0.0125	%FSR ±3LSB
Integral Nonlinearity Tempco	–	–	±8.5	ppm/°C
Differential Nonlinearity				
+25 °C	–	–	±0.0125	%FSR ±1/2LSB
0 °C to +70 °C	–	–	±0.0125	%FSR ±1/2LSB
-55 °C to +125 °C	–	–	±0.0125	%FSR ±1LSB
Differential Nonlinearity Tempco	–	–	±6.1	ppm/ °C
Full-Scale Absolute Accuracy				
+25 °C	–	±3	±8	LSB
0 °C to +70 °C	–	±4	±14	LSB
-55 °C to +125 °C	–	±8	±29	LSB
ADS-105				
Unipolar Zero Error, +25 °C	–	±1	±3	LSB
Unipolar Zero Error Tempco	–	±13	±25	ppm/ °C
ADS-106				
Bipolar Offset Error, +25 °C	–	±2	±5	LSB
Bipolar Offset Error Tempco	–	±17.5	±35	ppm/ °C
Bipolar Zero Error, +25 °C	–	±1	±3	LSB
Bipolar Zero Error Tempco	–	±13	±25	ppm/ °C
Gain Error	–	±2	±5	LSB
Gain Error Tempco	–	±17.5	±35	ppm/ °C
No missing codes (For 12 binary bits)	Guaranteed over operating temperature range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding: ADS-105 (Pin 7 High)	Straight binary			
(Pin 7 Low)	Complementary binary			
ADS-106 (Pin 7 High)	Offset binary			
(Pin 7 Low)	Complementary offset binary			

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Conversion Rate:				
+25 °C	1	–	–	MHz
0 °C to +70 °C	1	–	–	MHz
-55 °C to +125 °C	1	–	–	MHz
A/D Conversion Time:				
+25 °C	–	–	500	nSec.
0 °C to +70 °C	–	–	540	nSec.
-55 °C to +125 °C	–	–	560	nSec.
Total Harmonic Distortion:				
DC to 100 KHz, (Vin = <5V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB
DC to 40 KHz, (Vin = 10V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB
DC to 25 KHz, (Vin = 20V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
-5V dc Supply	-4.75	-5	-5.25	Volts dc
Supply Current				
+15V Supply	–	+40	+54	mA
-15V Supply	–	-30	-40	mA
+5V Supply *	–	+56	+90	mA
-5V Supply	–	-173	-210	mA
Power Dissipation	–	2.2	2.7	Watts
Supply Rejection	–	–	±0.01	%FSR/%V

PHYSICAL/ ENVIRONMENTAL	MIN.	TYP.	MAX.	UNITS
Operating Temperature Range				
MC Models	0	–	+70	°C
MM Models	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Weight	–	–	0.42(12)	oz.(gram)
Package Type	32-pin hermetically sealed ceramic DIP			
Pin Type	0.010 x 0.018 inch Kovar			

* + 5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce any small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

   Do not connect these grounds together at the power supply terminals when the power supplies are located some distance from the ground plane. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 1) to ground (pin 16) also using a 4.7μF, 25V capacitor. The -5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.

4. Obtain straight binary/offset binary output coding by tying the $\overline{\text{COMP BIN}}$ signal (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 ($\overline{\text{Enable bits 1-5 \& O.F.}}$).

6. The $\overline{\text{S/H}}$ Control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This indicates that the converter can accept a new analog input.

7. Full-scale absolute accuracy refers to the unadjusted performance of the ADS-105/106. These figures may be improved substantially using external trim circuits.

THEORY OF OPERATION

This theory of operation describes the ADS-105/106's function in conjunction with its internal Sample/Hold amplifer for digitizing sinusoidal signals. The ADS-105/106 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step conversion method, this technique uses a single 7-bit flash A/D converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, the block diagram, and the timing diagram as needed.

The ADS-105/106 guarantees a 1 MHz throughput rate when the START CONVERT pulse of 50 nanoseconds is provided at a 1 MHz rate. The 1 MHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or level signals is longer and listed under the acquisition specifications (10V step).

The ADS-105/106 is in the sample mode when the $\overline{\text{S/H}}$ CONTROL pin is high ($\overline{\text{S/H}}$ is in high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to $\overline{\text{S/H}}$ CONTROL low. This as

THEORY OF OPERATION (Cont.)

sures the sample-hold has the minumum required acquisition time for the particular application mode. Sinusoidal inputs being digitized by using a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 75 nanosecond delay before EOC goes high and the A/D conversion begins. This consists of the remaining 40 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to EOC high. The hold mode settling time and input settling time requirements required are met by observing this timing.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. EOC goes low indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed (EOC going low). The S/H Control output goes high shortly before EOC goes low, indicating that the Sample/Hold is back sampling the input. This feature improves the overall throughput of the ADS-105/106.

Data from the previous conversion is valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before the EOC goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput of the ADS-105/106 for sinusoidal inputs consists of 395 nanoseconds for acquisition time, 75 nanoseconds for START CONVERT and min-max propagation delays, 560 nanoseconds for A/D conversion time minus 30 nanoseconds for the S/H CONTROL pin. A throughput time of 1000 nanoseconds is obtained and a 1 Mhz throughput rate is realized.

Combining the A/D and S/H in one device allows the ADS-105/106 to guarantee a total throughput period of 1.0 microsecond maximum over the -55 °C to +125 °C temperature range for the complete system or a throughput rate of 1 MHz. Retriggering the START CONVERT pulse before EOC goes low will not initiate a new conversion.

The practical results of this means that single-channel (non-multiplexed) full-scale inputs with spectral content not exceeding 40 KHz for 10V peak-peak signals may be digitized up to a 1 MHz rate. This will give about 25 data samples per cycle to 12-bit accuracy and linearity. This type of resolution is ideal for capture of signals with a broad spectral content of 40 KHz and below (10V peak-to-peak signals). Because many samples may be taken in a short sampling interval, the ADS-105/106 are ideal for computer-aided spectral analysis of a complex-frequency signal. The 12-bit performance is ideal for larger fast fourier transform sizes of 1024 to 4096 points by reducing frequency binning resolution noise.

For multi-channel multiplexed signals, the very high multiplexing rate allows larger numbers of channels while still retaining moderate bandwidth per channel. Users requiring higher input bandwidth or faster acquisition times should review Datel's ADS-21 or ADS-22 Sampling A/D converter.

Table 1. ADC-105, ADC-106 Timing Specifications

TIMING	MIN.	TYP.	MAX.	UNITS
Start Convert Pulse Width:	50	–	–	nSec.
Start Convert Low to EOC High Delay	20	–	35	nSec.
Start Convert Low to Previous Data Invalid	350	–	–	nSec.
Data Valid Before EOC Goes Low	25	–	–	nSec.
Enable to Output Data Valid Delay	–	–	10	nSec.
EOC Low to Start Convert High (Sinusoidal Inputs)	355	–	–	nSec.

Note: Table 1 applies over the operating temperature range and over the operating power supply range.

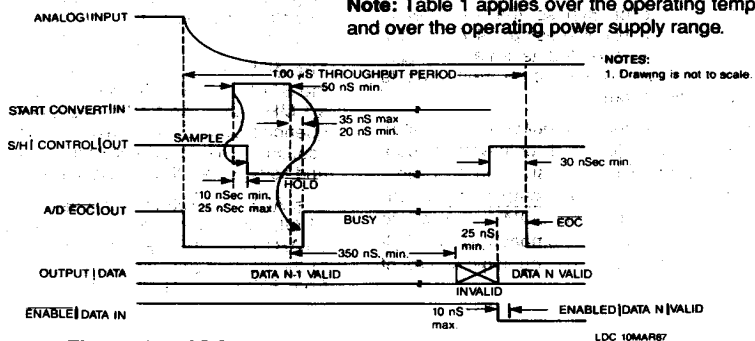


Figure 2. ADC-105, ADC-106 Timing Diagram

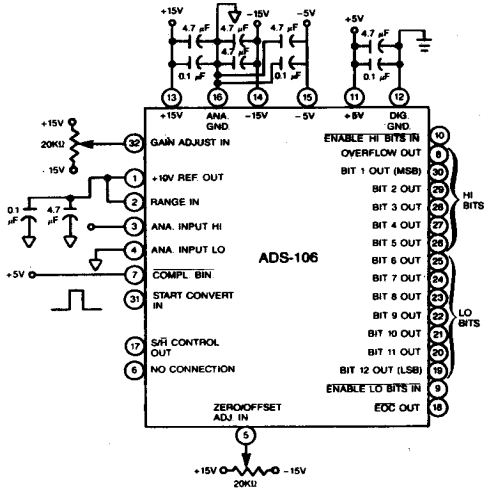


Figure 3. ADS-106 Typical External Connections, ± 10V dc

SYSTEM CALIBRATION PROCEDURE

Remove system errors or the small initial errors as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale input range (FSR). The data outputs should be connected to LED's to observe the resulting data values.

Table 2. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	JUMP PIN 2 TO PIN:
0 to +10V dc	3	No connection
±10V dc	3	1 (+10V Ref.)

Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments:

Apply a precision voltage reference source between the analog input (pin 3) and analog ground (pin 16). Use a very low-noise signal source for accurate calibration.

Adjust the output of the reference source per Tables 3 and 4 for the unipolar zero adjustment (+1/2 LSB) or the bipolar zero adjustment (zero + 1/2 LSB) for the appropriate full scale range. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with COMP BIN tied low.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with the COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low.

3. Full Scale Adjustment:

Set the output of the voltage reference used in step 2 to the value shown in the Tables 3 and 4 for the unipolar or bipolar gain adjustment (+F.S. -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in the Tables 5 and 6.

Table 3. Zero and Gain Adjust for Unipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
UNIPOLAR FSR 0 to +10V	(+1/2 LSB) +1.22mV dc	(+FS -1 1/2 LSB) +9.9963V dc

Table 4. Zero and Gain Adjust for Bipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
BIPOLAR FSR ±10V	(+1/2 LSB) +2.44mV	(+FS -1 1/2 LSB) +9.9927V

Table 5. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	0 to +10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9976V	1111 1111	1111	0000 0000	0000
7/8 FS	+8.750V	1110 0000	0000	0001 1111	1111
3/4 FS	+7.500V	1100 0000	0000	0011 1111	1111
1/2 FS	+5.000V	1000 0000	0000	0111 1111	1111
1/4 FS	+2.500V	0100 0000	0000	1011 1111	1111
1/8 FS	+1.250V	0010 0000	0000	1101 1111	1111
1 LSB	+0.0024V	0000 0000	0001	1111 1111	1110
0	0.0000V	0000 0000	0000	1111 1111	1111

Table 6. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	± 10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9951V	1111 1111	1111	0000 0000	0000
+3/4 FS	+7.5000V	1110 0000	0000	0001 1111	1111
+1/2 FS	+5.0000V	1100 0000	0000	0011 1111	1111
0	0.00000V	1000 0000	0000	0111 1111	1111
-1/2 FS	-5.0000V	0100 0000	0000	1011 1111	1111
-3/4 FS	-7.5000V	0010 0000	0000	1101 1111	1111
-FS + 1 LSB	-9.9951V	0000 0000	0001	1111 1111	1110
-FS	-10.000V	0000 0000	0000	1111 1111	1111

ORDERING INFORMATION

ADS-105 12-Bit, 1 MHz
ADS-106 Sampling A/D Converters

MODEL	TEMPERATURE RANGE	INPUT VOLTAGE RANGE
ADS-105MC	0°C to +70°C	0 to +10V
ADS-106MC	0°C to +70°C	-10 to +10V
ADS-105MM	-55°C to +125°C	0 to +10V
ADS-106MM	-55°C to +125°C	-10 to +10V

Trimming Potentiometer: TP 20K (2 required)
A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high-reliability versions of the ADS-105/-106, contact the factory.