

MOS INTEGRATED CIRCUIT

μ PD46258, 46259L

256K-BIT BiCMOS FAST STATIC RAM 32K-WORD BY 8-BIT/32K-WORD BY 9-BIT

Description

The μ PD46258 is 262,144 bits (32,768 words by 8 bits) and the μ PD46259L is 294,912 bits (32,768 words by 9 bits) BiCMOS static RAMs.

Operating supply voltage is 5 V $\pm$ 10 % for the μ PD46258 or 3.3 V $\pm$ 0.3 V for the μ PD46259L.

The μ PD46258 and 46259L are packed in 32-pin plastic SOJ.

Features

- 32,768 words by 8 or 9 bits organization
- Output Enable input for easy application
- Fast access time

Ordering Information

Part number	Package	Word organization	Access time ns (MAX.)	Supply voltage (TYP.)	Supply current mA (MAX.)	
					Operating	Standby
μ PD46258LA-6	32-Pin plastic SOJ (300 mil)	32K $\times$ 8 bits	6	5 V $\pm$ 10 %	190	50
μ PD46258LA-7			7			
μ PD46258LA-8			8			
μ PD46259LLA-A12		32K $\times$ 9 bits	12	3.3 V $\pm$ 0.3 V	130	20

Quality grade

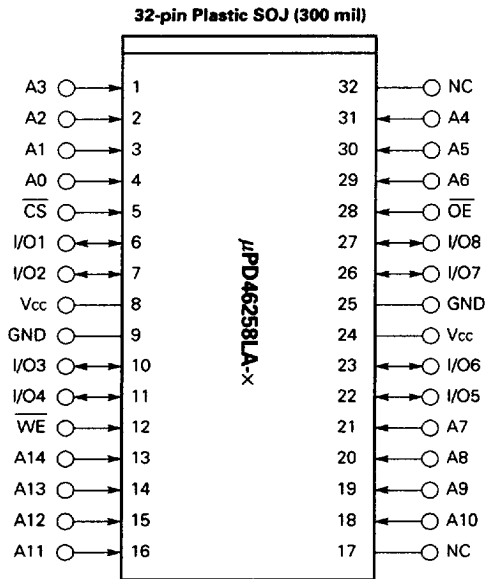
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

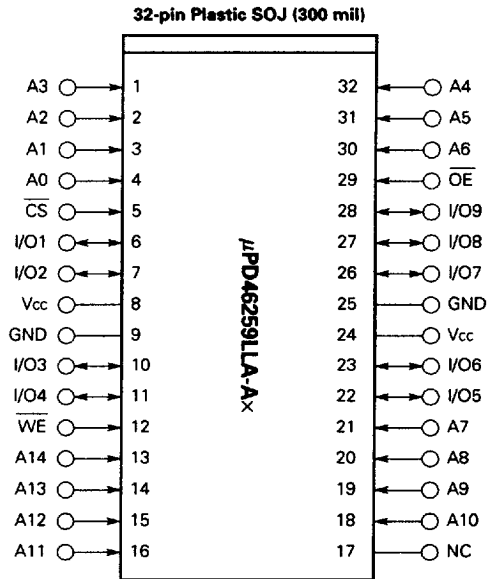
The information in this document is subject to change without notice.

Pin Configuration (Marking Side)

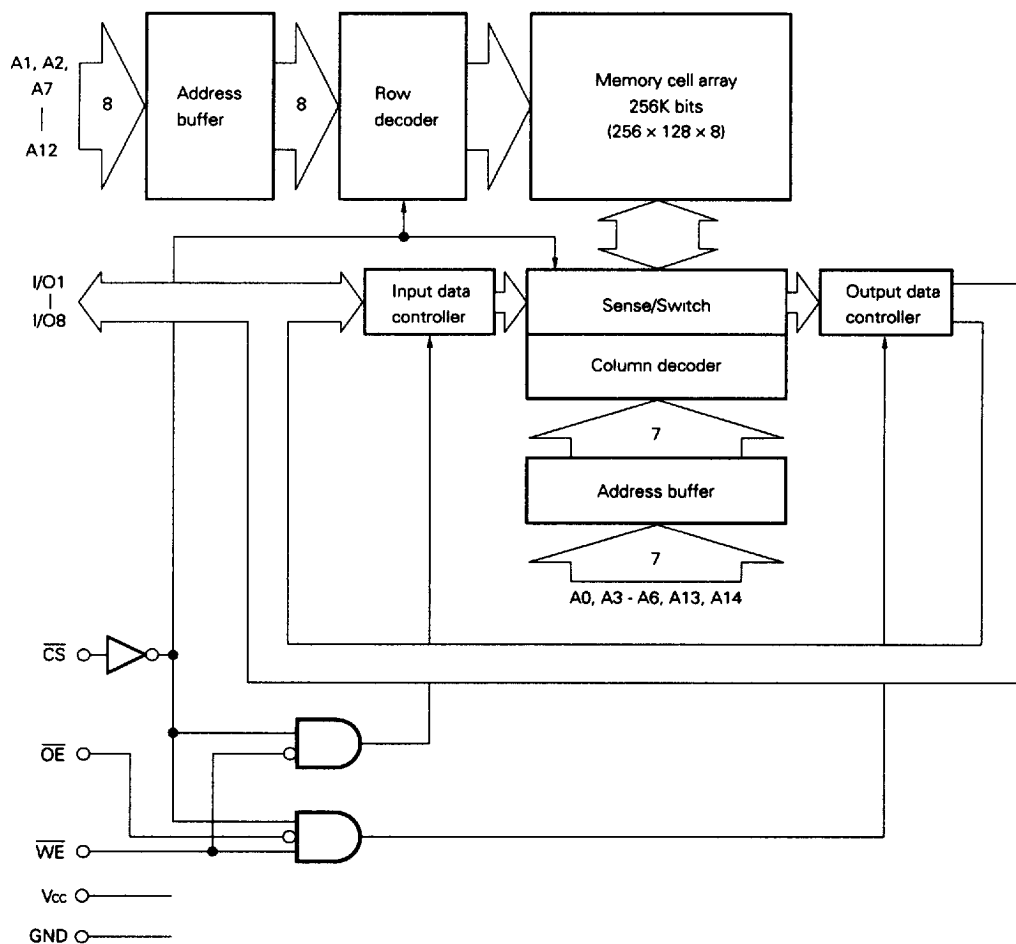
• μPD46258



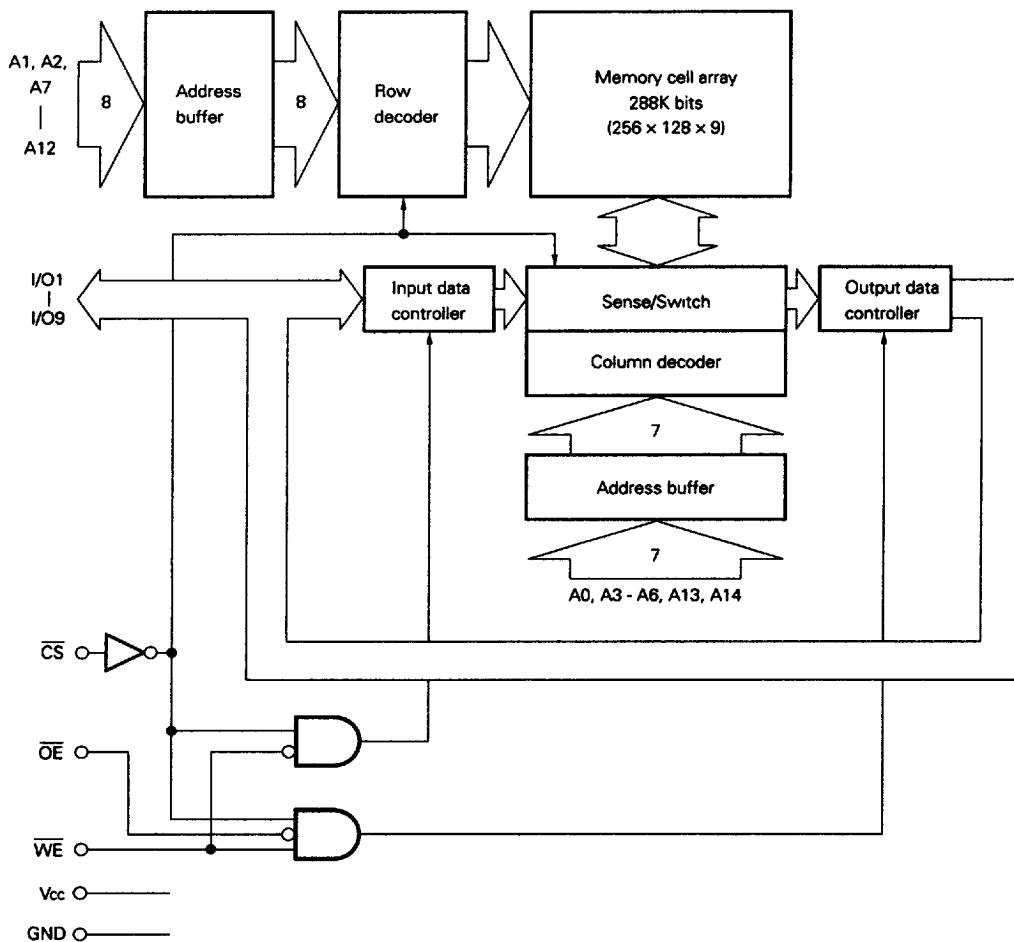
• μPD46259L



A0 - A14 : Address inputs
 I/O1 - I/O9 : Data inputs/outputs
 CS : Chip Select
 WE : Write Enable
 OE : Output Enable
 Vcc : Power Supply
 GND : Ground
 NC : No Connection

Block Diagram (μ PD46258)

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Block Diagram (μ PD46259L)**Truth Table**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	x	x	Not selected	High impedance	I_{ss}
L	L	H	Read	Dout	I_{cc}
L	x	L	Write	Din	
L	H	H	Output disable	High impedance	

Remark x: Don't care

Electrical Characteristics

The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the following tables.

Absolute Maximum Ratings

Parameter	Symbol	μPD46258	μPD46259L	Unit
Supply voltage	V _{CC}	-0.5 Note 1 to +7.0	-0.5 Note 2 to +4.5	V
Input voltage	V _{IN}	-0.5 Note 1 to V _{CC} + 0.5	-0.5 Note 2 to V _{CC} + 0.5	V
Input/Output voltage	V _{IO}	-0.5 Note 1 to +4.5	-0.5 Note 2 to V _{CC}	V
Operating temperature	T _{opt}	0 to 70		°C
Storage temperature	T _{stg}	-55 to +125		°C

Note 1. -1.0 V (MIN.): (Pulse width 3 ns)

2. -2.5 V (MIN.): (Pulse width 3 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD46258			μPD46259L			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V _{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
High level input voltage	V _{IH}	2.2		3.5	2.0		V _{CC} + 0.5	V
Low level input voltage	V _{IL}	-0.5 Note 1		+0.8	-0.5 Note 2		+0.8	°C
Ambient temperature	T _a	0		+70	0		+70	°C

Note 1. -1.0 V (MIN.): (Pulse width 3 ns)

2. -2.5 V (MIN.): (Pulse width 3 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		μPD46258			μPD46259L			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _{II}	V _{IN} = 0 V to V _{CC}		-10		+10	-10		+10	μA
I/O leakage current	I _{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	V _{I/O} = 0 V to 3.5 V	-10		+10	-		-	μA
			V _{I/O} = 0 V to V _{CC}	-		-	-10		+10	
Operating supply current	I _{CC}	$\overline{CS} = V_{IL}$, I _{I/O} = 0 mA	Cycle frequency ≤ 100 MHz			190			130	mA
			Cycle frequency = 0 MHz			130			110	
Standby supply current	I _{SB}	$\overline{CS} = V_{IH}$, V _{IN} = V _{IH} or V _{IL}				70			40	mA
	I _{SB1}	$\overline{CS} \geq V_{CC} - 0.2$ V, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				50			20	
High level output voltage	V _{OH}	I _{OH} = -4.0 mA		2.4			-			V
		I _{OH} = -2.0 mA		-			2.4			
Low level output voltage	V _{OL}	I _{OL} = 8.0 mA				0.4			-	V
		I _{OL} = 4.0 mA				-			0.4	

Remark V_{IN}: Input voltage

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	μPD46258			μPD46259L			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input capacitance	C _{IN}	V _{IN} = 0 V			7			8	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0 V			5			6	pF

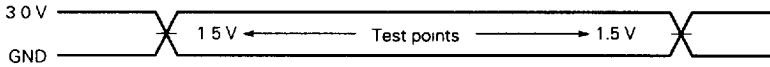
Remark 1. V_{IN}: Input voltage

2. These parameters are sampled and not 100 % tested.

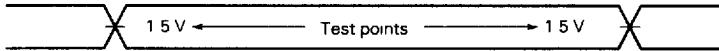
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/Fall Time ≤ 2 ns)



Output waveform



Output load

AC characteristics directed with the **notes** should be measured with the following output load shown in **Fig. 1** to **Fig. 4**.

tAA, tACS, tOE, tOH (for μ PD46258) are measured with the output load shown in **Fig. 1**.

tAA, tACS, tOE, tOH (for μ PD46259L) are measured with the output load shown in **Fig. 2**.

tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW (for μ PD46258) are measured with the output load shown in **Fig. 3**.

tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW (for μ PD46259L) are measured with the output load shown in **Fig. 4**.

Fig. 1 Output load (for μ PD46258)
(tAA, tACS, tOE, tOH)

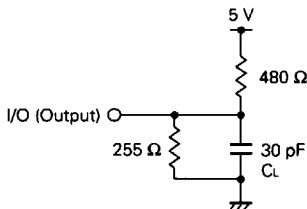


Fig. 2 Output load (for μ PD46259L)
(tAA, tACS, tOE, tOH)

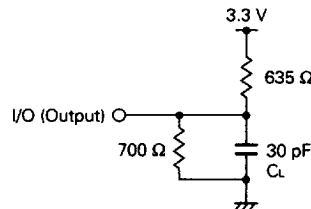


Fig. 3 Output load (for μ PD46258)
(tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW)

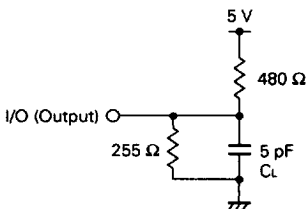
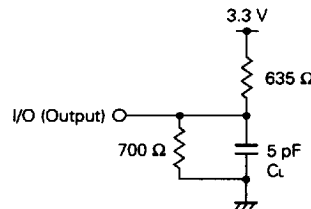


Fig. 4 Output load (for μ PD46259L)
(tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW)



Remark Cl (for **Fig. 1** to **Fig. 4**) includes capacitances of the probe and jig, stray capacitances.

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Read Cycle (μ PD46258: $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	μ PD46258-6		μ PD46258-7		μ PD46258-8		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	6		7		8		ns	
Address access time	t_{AA}		6		7		8	ns	Note 1.
CS access time	t_{ACS}		6		7		8	ns	
OE access time	t_{OE}		4		5		5	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
CS to output in low impedance	t_{CLZ}	2		2		2		ns	Note 2.
$\overline{OE}$ to output in low impedance	t_{OLZ}	1		1		1		ns	
CS to output in high impedance	t_{CHZ}		3		4		4	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		3		4		4	ns	

Note 1. See the output load shown in Fig. 1.

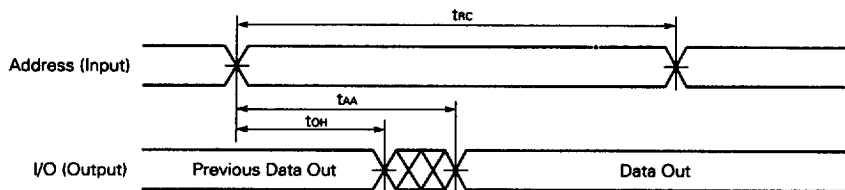
2. See the output load shown in Fig. 3.

Read Cycle (μ PD46259L: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	μ PD46259L-A12		Unit	Condition
		MIN.	MAX.		
Read cycle time	t_{RC}	12		ns	
Address access time	t_{AA}		12	ns	Note 1.
CS access time	t_{ACS}		12	ns	
$\overline{OE}$ access time	t_{OE}		6	ns	
Output hold from address change	t_{OH}	2		ns	
CS to output in low impedance	t_{CLZ}	2		ns	Note 2.
$\overline{OE}$ to output in low impedance	t_{OLZ}	1		ns	
CS to output in high impedance	t_{CHZ}		5	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		5	ns	

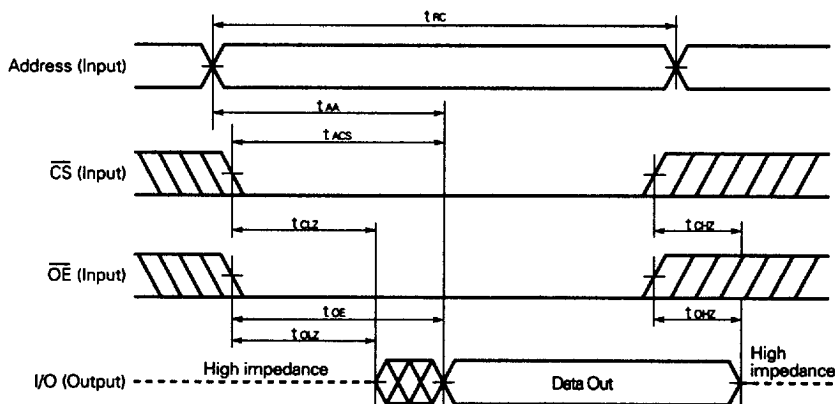
Note 1. See the output load shown in Fig. 2.

2. See the output load shown in Fig. 4.

Read Cycle Timing Chart 1 (Address Access)

Remark 1. In read cycle, $\overline{WE}$ should be fixed to high level.

2. $\overline{CS} = \overline{OE} = V_{IL}$

Read Cycle Timing Chart 2 ($\overline{CS}$ Access)

Caution Address valid prior to or coincident with $\overline{CS}$ low level input.

Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle (μPD46258: Vcc = 5 V ±10 %)

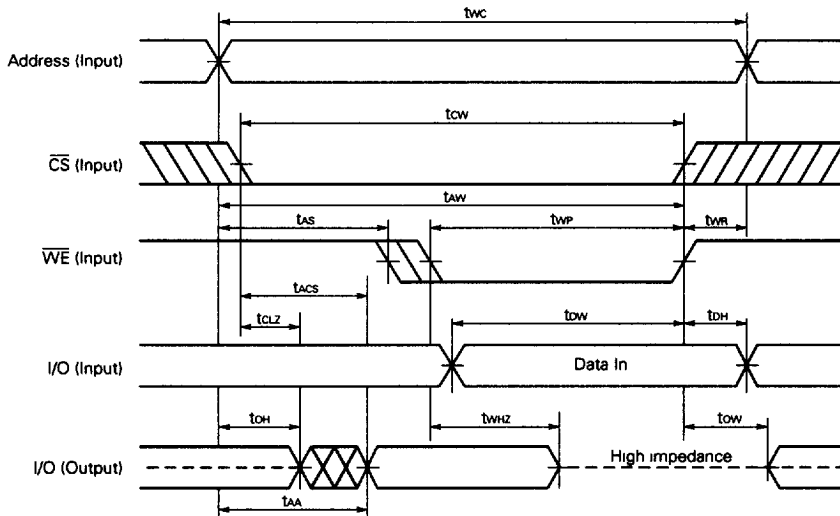
Parameter	Symbol	μPD46258-6		μPD46258-7		μPD46258-8		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	6		7		8		ns	
CS to end of write	t _{CS}	4		5		6		ns	
Address valid to end of write	t _{AV}	4		5		6		ns	
Write pulse width	t _{WP}	4		5		6		ns	
Data valid to end of write	t _{DV}	3		4		5		ns	
Data hold time	t _{DH}	0		0		0		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write recovery time	t _{WR}	0		0		0		ns	
WE to output in high impedance	t _{WHZ}		3		4		4	ns	Note
Output active from end of write	t _{OW}	1		1		1		ns	

Note See the output load shown in Fig. 3.

Write Cycle (μPD46259L: Vcc = 3.3 V ±0.3 V)

Parameter	Symbol	μPD46259L-A12		Unit	Condition
		MIN.	MAX.		
Write cycle time	t _{WC}	10		ns	
CS to end of write	t _{CS}	7		ns	
Address valid to end of write	t _{AV}	7		ns	
Write pulse width	t _{WP}	7		ns	
Data valid to end of write	t _{DV}	6		ns	
Data hold time	t _{DH}	0		ns	
Address setup time	t _{AS}	0		ns	
Write recovery time	t _{WR}	0		ns	
WE to output in high impedance	t _{WHZ}		5	ns	Note
Output active from end of write	t _{OW}	1		ns	

Note See the output load shown in Fig. 4.

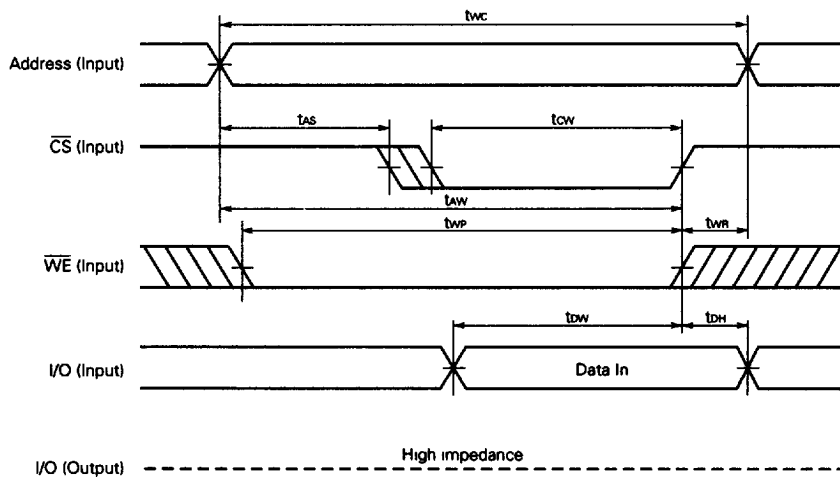
Write Cycle Timing Chart 1 ($\overline{\text{WE}}$ Controlled)

Caution $\overline{\text{CS}}$ or $\overline{\text{WE}}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of a low level $\overline{\text{CS}}$ and a low level $\overline{\text{WE}}$.

2. During t_{whz} , I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When $\overline{\text{WE}}$ is at low level, the I/O pins are always High impedance. When $\overline{\text{WE}}$ is at high level, read operation is executed. Therefore $\overline{\text{OE}}$ should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 ($\overline{\text{CS}}$ Controlled)

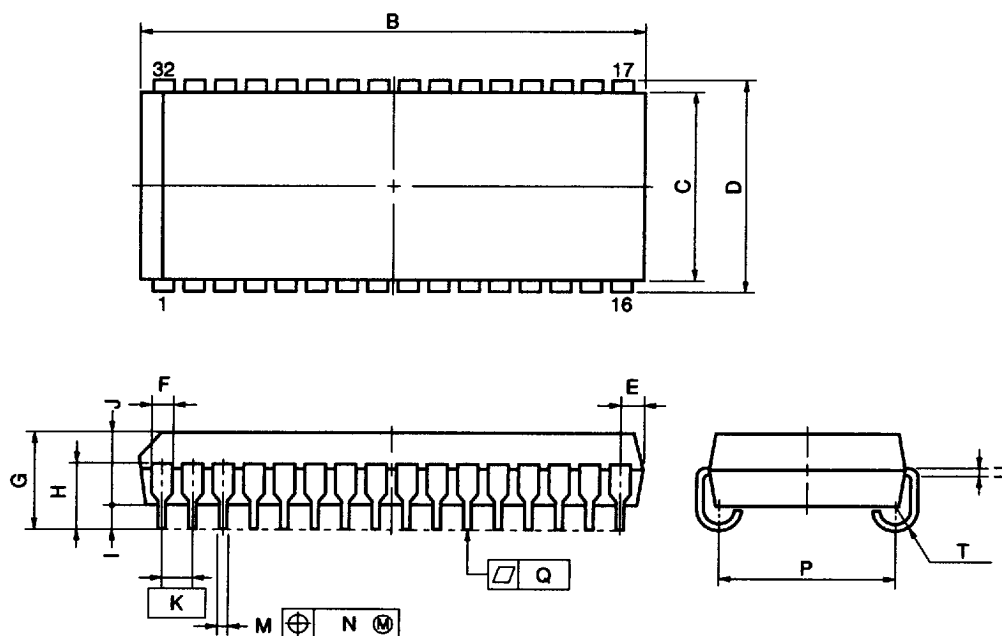
Caution $\overline{\text{CS}}$ or $\overline{\text{WE}}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{\text{CS}}$ and a low level $\overline{\text{WE}}$.

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Package Drawing

32 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	21.21 ^{+0.2} _{-0.35}	0.835 ^{+0.008} _{-0.014}
C	7.57	0.298
D	8.47±0.2	0.333 ^{+0.008} _{-0.008}
E	1.08±0.15	0.043 ^{+0.008} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.4±0.2	0.094 ^{+0.008} _{-0.008}
I	0.8 MIN.	0.031 MIN.
J	2.55	0.1
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

P32LA-300A-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD46258 and 46259L.

Types of Surface Mount Device

μ PD46258LA : 32-pin plastic SOJ (300 mil)

μ PD46259LLA: 32-pin plastic SOJ (300 mil)