

MOS INTEGRATED CIRCUIT

μ PD42S65165, 4265165

64 M-BIT DYNAMIC RAM
4 M-WORD BY 16-BIT, EDO,
BYTE READ/WRITE MODE

Description

The μ PD42S65165, 4265165 are 4,194,304 words by 16 bits CMOS dynamic RAMs with optional EDO.

EDO is a kind of the page mode and is useful for the read operation.

Besides, the μ PD42S65165 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 50-pin plastic TSOP (II).

Features

- EDO (Hyper page mode)
- 4,194,304 words by 16 bits organization
- Single +3.3 V $\pm$ 0.3 V power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)
μ PD42S65165-A50, 4265165-A50	540 mW	50 ns	84 ns	20 ns
μ PD42S65165-A60, 4265165-A60	468 mW	60 ns	104 ns	25 ns

- The μ PD42S65165 can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S65165	4,096 cycles/128 ms	$\overline{\text{RAS}}$ only refresh, Normal read/write, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	0.72 mW (CMOS level input)
μ PD4265165	4,096 cycles/64 ms	$\overline{\text{RAS}}$ only refresh, Normal read/write, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh	1.8 mW (CMOS level input)

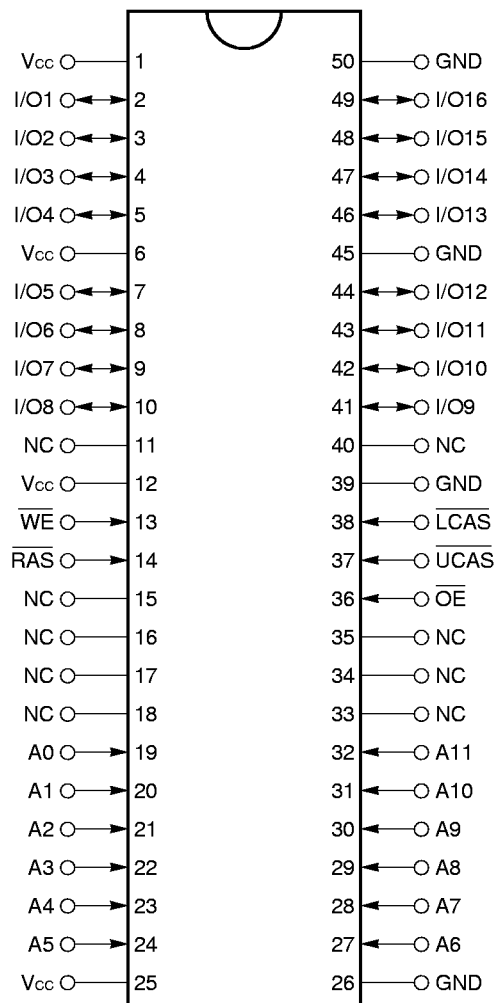
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Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μ PD42S65165G5-A50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh
μ PD42S65165G5-A60-7JF	60 ns		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD4265165G5-A50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
μ PD4265165G5-A60-7JF	60 ns		$\overline{\text{RAS}}$ only refresh Hidden refresh

Pin Configuration (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

 μ PD42S65165G5-7JF μ PD4265165G5-7JF

A0 to A11 : Address Inputs

I/O1 to I/O16 : Data Inputs/Outputs

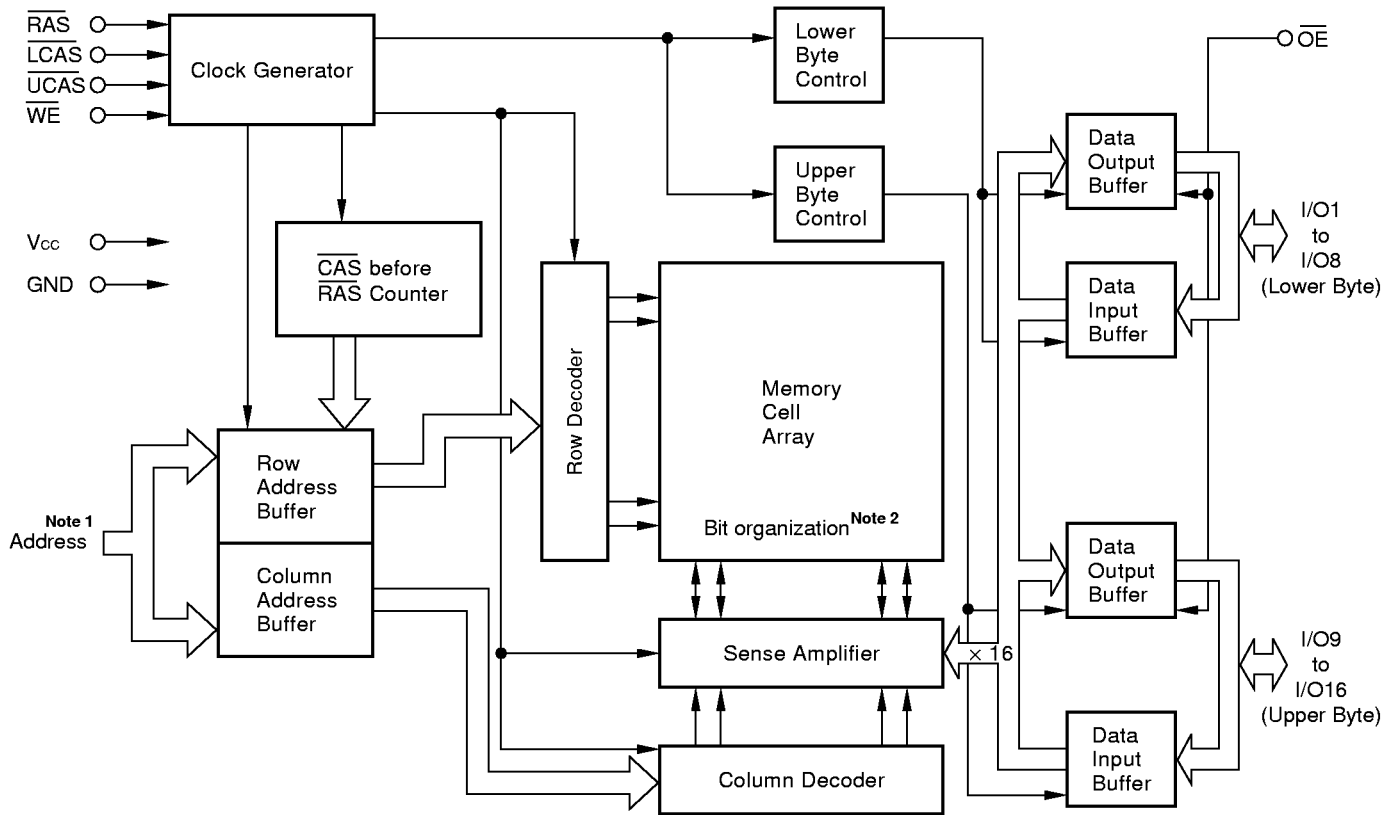
 $\overline{\text{RAS}}$: Row Address Strobe $\overline{\text{UCAS}}$: Upper Byte Column Address Strobe $\overline{\text{LCAS}}$: Lower Byte Column Address Strobe $\overline{\text{WE}}$: Write Enable $\overline{\text{OE}}$: Output Enable

Vcc : Power Supply

GND : Ground

NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S65165, 4265165	A0 - A11	A0 - A9

2. $4,096 \times 1,024 \times 16$

Input/Output Pin Functions

The μ PD42S65165, 4265165 have input pins $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A11 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ (Upper, Lower column address strobe)	Input	$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 12-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

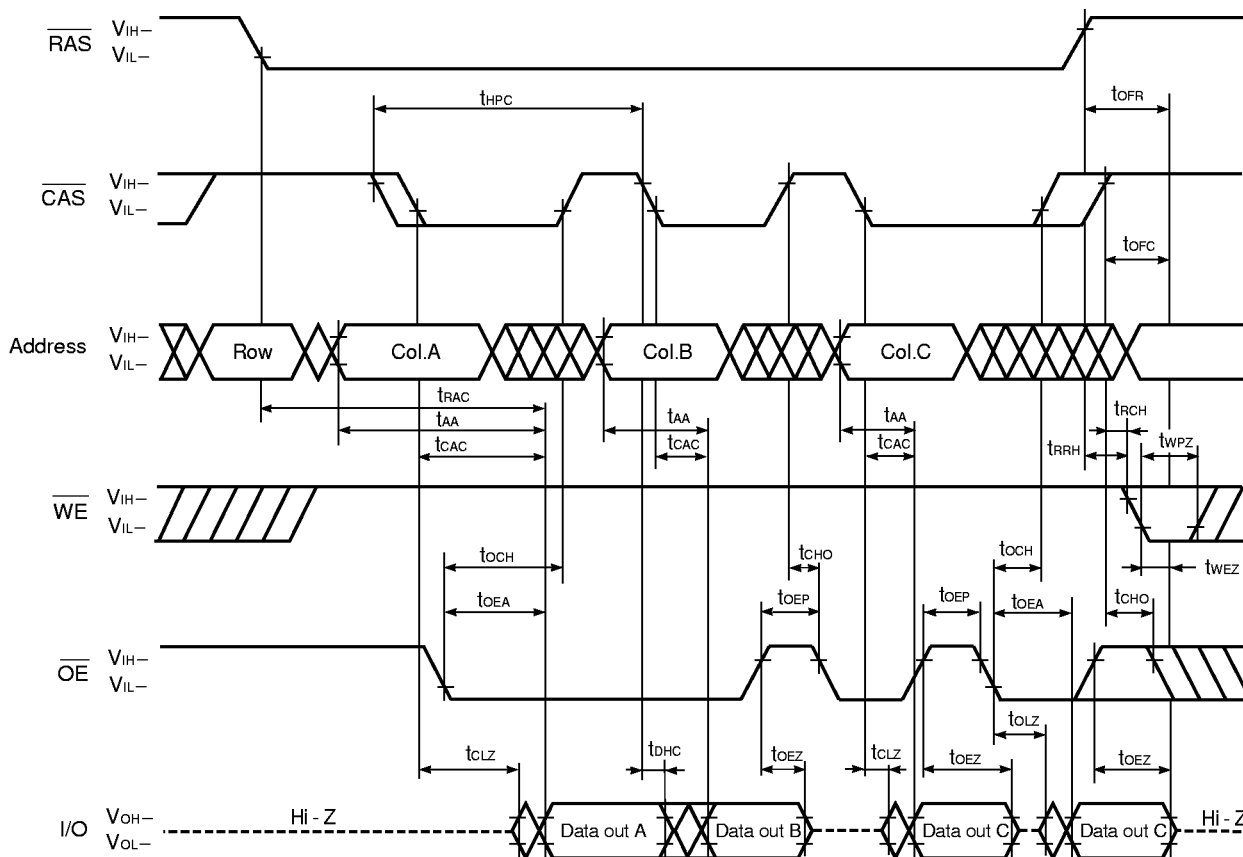
In the hyper page mode (EDO), due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{\text{CAS}}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.

Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

The faster of t_{OEZ} and t_{WEZ} becomes effective.

The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of $\overline{\text{CAS}}$ signal when controlling data output with the $\overline{\text{OE}}$ signal.
 - (1) $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 - (2) $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ inactive) and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μ PD42S65165, 4265165]

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	$t_{RAC} = 50 \text{ ns}$	150	mA	1, 2, 3
			$t_{RC} = t_{RC(MIN.)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	130		
Standby current	μ PD42S65165	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, $I_O = 0 \text{ mA}$		1.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, $I_O = 0 \text{ mA}$		0.2		
	μ PD4265165		$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, $I_O = 0 \text{ mA}$		1.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, $I_O = 0 \text{ mA}$		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	$t_{RAC} = 50 \text{ ns}$	150	mA	1, 2, 3, 4
			$t_{RC} = t_{RC(MIN.)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	130		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ cycling	$t_{RAC} = 50 \text{ ns}$	120	mA	1, 2, 5
			$t_{HPC} = t_{HPC(MIN.)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	$t_{RAC} = 50 \text{ ns}$	150	mA	1, 2
			$t_{RC} = t_{RC(MIN.)}$, $I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	130		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles/128 ms, only for the μ PD42S65165)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: $t_{RC} = 31.3 \mu\text{s}$ $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$	$t_{RAS} \leq 300 \text{ ns}$	500	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} $I_O = 0 \text{ mA}$	$t_{RAS} \leq 1 \mu\text{s}$	600	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μ PD42S65165)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: $t_{RAS} = 5 \text{ ms}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_O = 0 \text{ mA}$		400	μA	2
Input leakage current		$I_{I(L)}$	$V_I = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current		$I_{O(L)}$	$V_O = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage		V_{OH}	$I_O = -2.0 \text{ mA}$	2.4		V	
Low level output voltage		V_{OL}	$I_O = +2.0 \text{ mA}$		0.4	V	

Notes 1. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

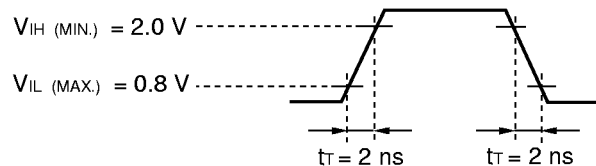
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.5. I_{CC4} is measured assuming that all column address inputs are switched only once during each Hyper page (EDO) cycle.

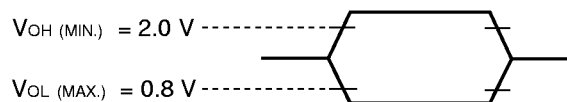
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

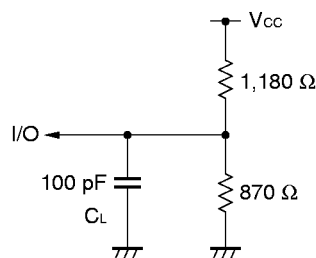
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t _{RC}	84	—	104	—	ns	
$\overline{\text{RAS}}$ precharge time		t _{RP}	30	—	40	—	ns	
$\overline{\text{CAS}}$ precharge time		t _{CPN}	7	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width		t _{RAS}	50	10,000	60	10,000	ns	1
$\overline{\text{CAS}}$ pulse width		t _{CAS}	8	10,000	10	10,000	ns	
$\overline{\text{RAS}}$ hold time		t _{RSH}	13	—	15	—	ns	
$\overline{\text{CAS}}$ hold time		t _{CSH}	38	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time		t _{RCD}	11	37	14	45	ns	2
$\overline{\text{RAS}}$ to column address delay time		t _{RAD}	9	25	12	30	ns	2
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time		t _{CRP}	5	—	5	—	ns	3
Row address setup time		t _{ASR}	0	—	0	—	ns	
Row address hold time		t _{RAH}	7	—	10	—	ns	
Column address setup time		t _{ASC}	0	—	0	—	ns	
Column address hold time		t _{CAH}	7	—	10	—	ns	
$\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$		t _{OES}	0	—	0	—	ns	
$\overline{\text{CAS}}$ to data setup time		t _{CLZ}	0	—	0	—	ns	
$\overline{\text{OE}}$ to data setup time		t _{OLZ}	0	—	0	—	ns	
$\overline{\text{OE}}$ to data delay time		t _{OED}	10	—	13	—	ns	
Masked byte write hold time referenced to $\overline{\text{RAS}}$		t _{MRH}	0	—	0	—	ns	
Transition time (rise and fall)		t _r	1	50	1	50	ns	
Refresh time	$\mu\text{PD42S65165}$	t _{REF}	—	128	—	128	ms	4
	$\mu\text{PD4265165}$		—	64	—	64	ms	

- Notes 1.** In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{\text{RAS}}(\text{MAX.})$ is 100 μs . If $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
- 2.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- 3.** $t_{\text{CRP}}(\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- 4.** This specification is applied only to the μ PD42S65165.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	ns	1
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	15	ns	1
Access time from column address	t_{AA}	—	25	—	30	ns	1
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	t_{RAL}	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	10	0	13	ns	3
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	t_{CHO}	5	—	5	—	ns	4

- Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- 2.** Either $t_{\text{RCH}}(\text{MIN.})$ or $t_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
- 3.** $t_{\text{OEZ}}(\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .
- 4.** $\overline{\text{WE}}$: inactive (in read cycle)
 $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active..... t_{CHO} is effective.
 $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active..... t_{OCH} is effective.

Write Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	7	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	7	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	13	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	7	–	10	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEh}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	7	–	10	–	ns	3

- Notes**
1. $t_{WP} \text{ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH} \text{ (MIN.)}$ should be met.
 2. If $t_{WCS} \geq t_{WCS} \text{ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. $t_{DS} \text{ (MIN.)}$ and $t_{DH} \text{ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	107	–	133	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	64	–	77	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	ns	1

- Note**
1. If $t_{WCS} \geq t_{WCS} \text{ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD} \text{ (MIN.)}$, $t_{CWD} \geq t_{CWD} \text{ (MIN.)}$, $t_{AWD} \geq t_{AWD} \text{ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD} \text{ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	20	—	25	—	ns	1
$\overline{\text{RAS}}$ pulse width	t_{RASP}	50	125,000	60	125,000	ns	
$\overline{\text{CAS}}$ pulse width	t_{HCAS}	8	10,000	10	10,000	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	7	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{ACP}	—	30	—	35	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t_{CPWD}	41	—	52	—	ns	2
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	30	—	35	—	ns	
Read modify write cycle time	t_{HPRWC}	52	—	66	—	ns	
Data output hold time	t_{DHC}	5	—	5	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t_{OCH}	5	—	5	—	ns	3
$\overline{\text{OE}}$ precharge time	t_{OEP}	5	—	5	—	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t_{WEZ}	0	10	0	13	ns	4, 5
$\overline{\text{WE}}$ pulse width	t_{WPZ}	7	—	10	—	ns	5
Output buffer turn-off delay from $\overline{\text{RAS}}$	t_{OFR}	0	10	0	13	ns	4, 5
Output buffer turn-off delay from $\overline{\text{CAS}}$	t_{OFC}	0	10	0	13	ns	4, 5

Notes 1. t_{HPC} (MIN.) is applied to $\overline{\text{CAS}}$ access.

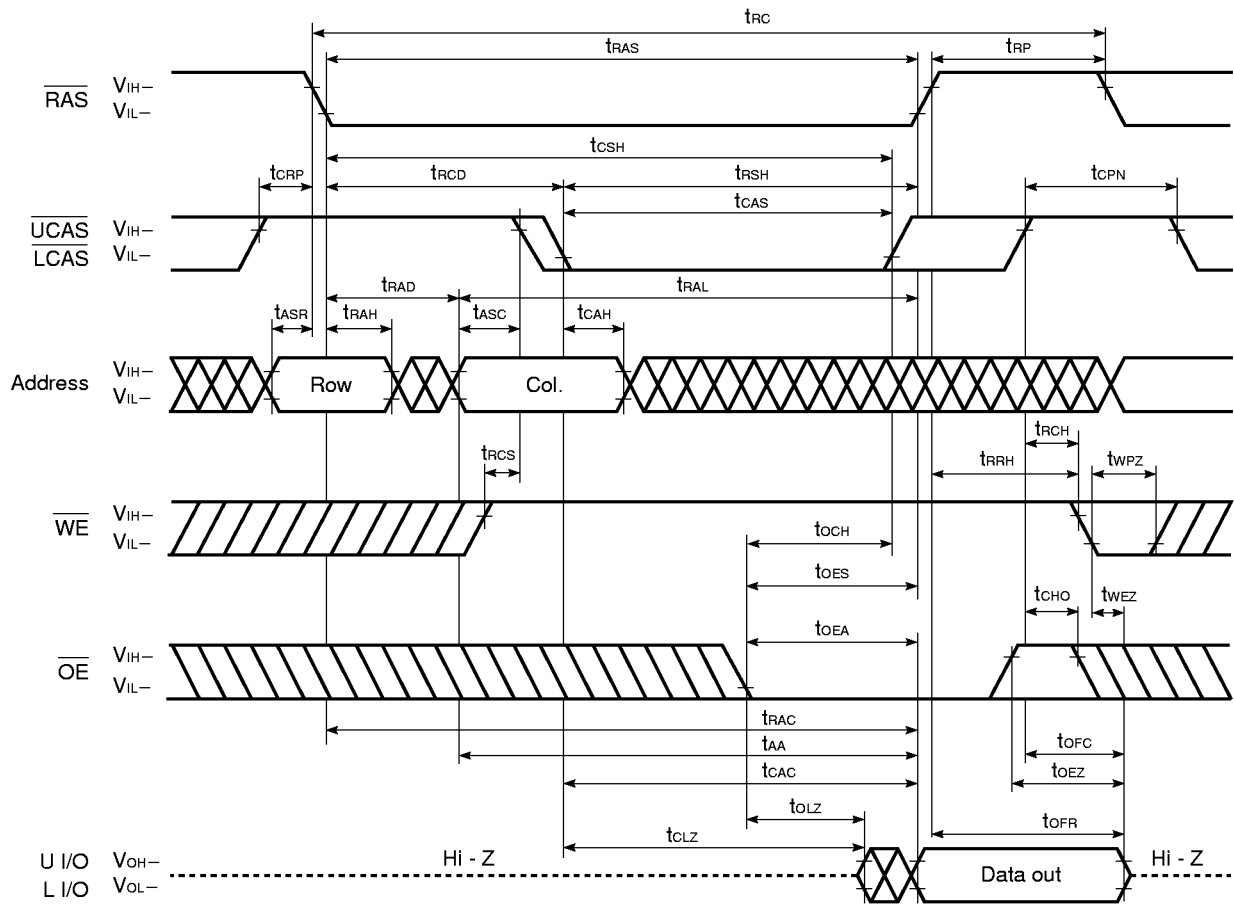
2. If $t_{WCS} \geq t_{WCS}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{MIN.})$, $t_{CWD} \geq t_{CWD}(\text{MIN.})$, $t_{AWD} \geq t_{AWD}(\text{MIN.})$ and $t_{CPWD} \geq t_{CPWD}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
 3. $\overline{\text{WE}}$: inactive (in read cycle)
 $\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.
 $\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.
 4. $t_{OFC}(\text{MAX.})$, $t_{OFR}(\text{MAX.})$ and $t_{WEZ}(\text{MAX.})$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL} .
 5. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.
 - (1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of the read cycle)
 $\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active
 t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.
 t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.
 The slower of t_{OFC} and t_{OFR} becomes effective.
 - (2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{OEZ} is effective.
 Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)
 $\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.
 The faster of t_{OEZ} and t_{WEZ} becomes effective.
- The faster of (1) and (2) becomes effective.

Refresh Cycle

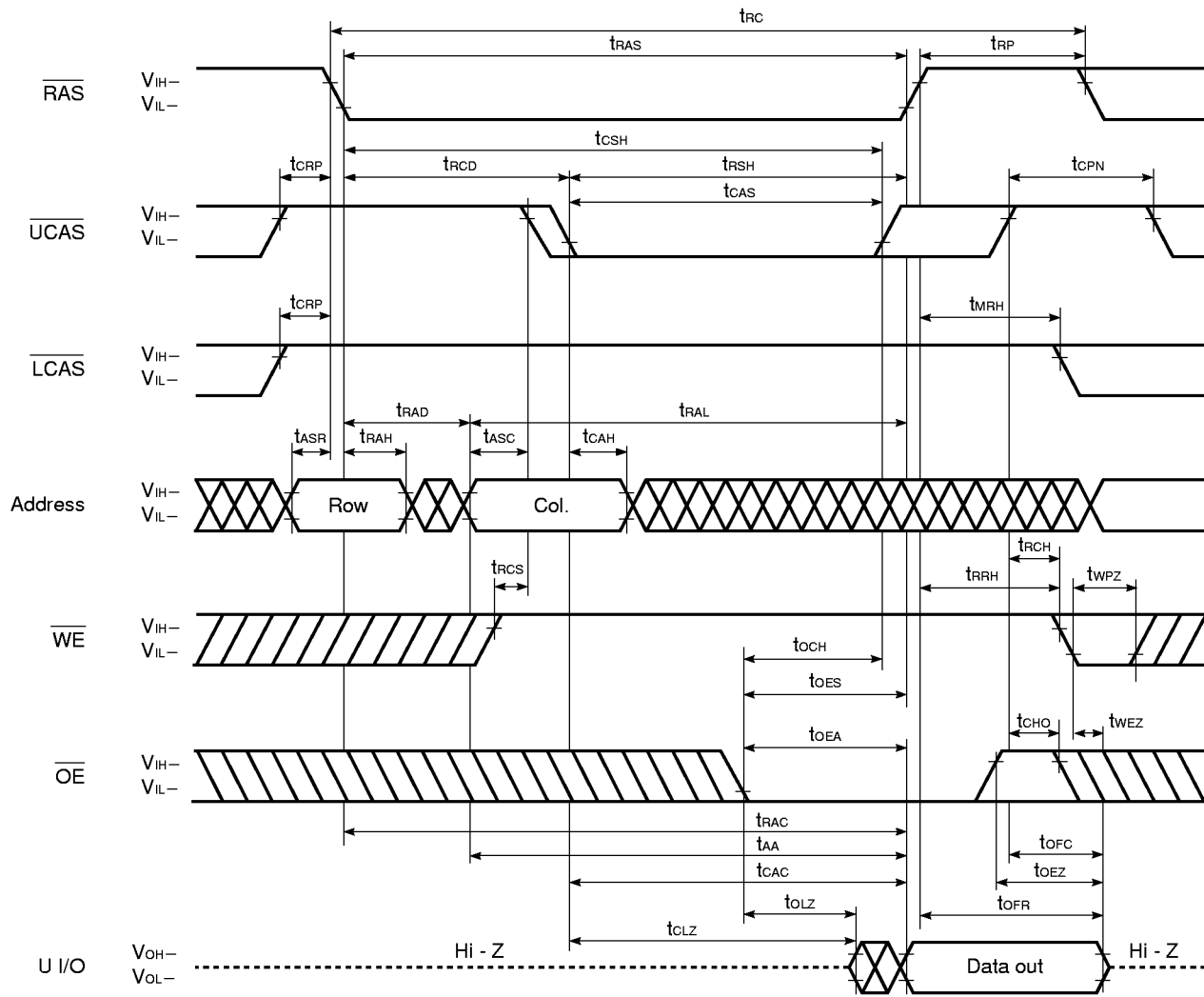
Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	—	100	—	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	90	—	110	—	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	−50	—	−50	—	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	—	10	—	ns	
$\overline{WE}$ hold time	t_{WHR}	15	—	15	—	ns	

Note 1. This specification is applied only to the μ PD42S65165.

Read Cycle

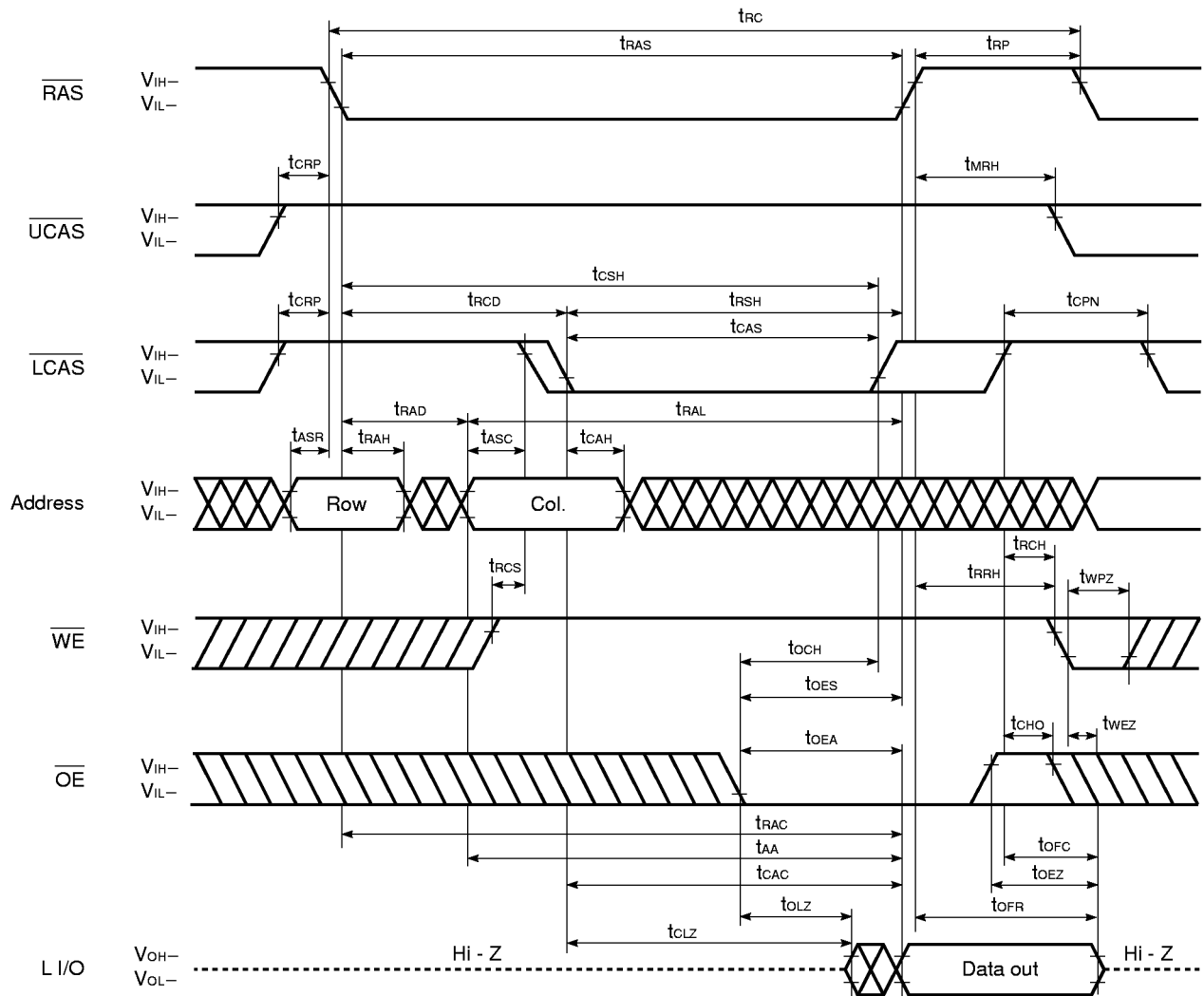


Upper Byte Read Cycle



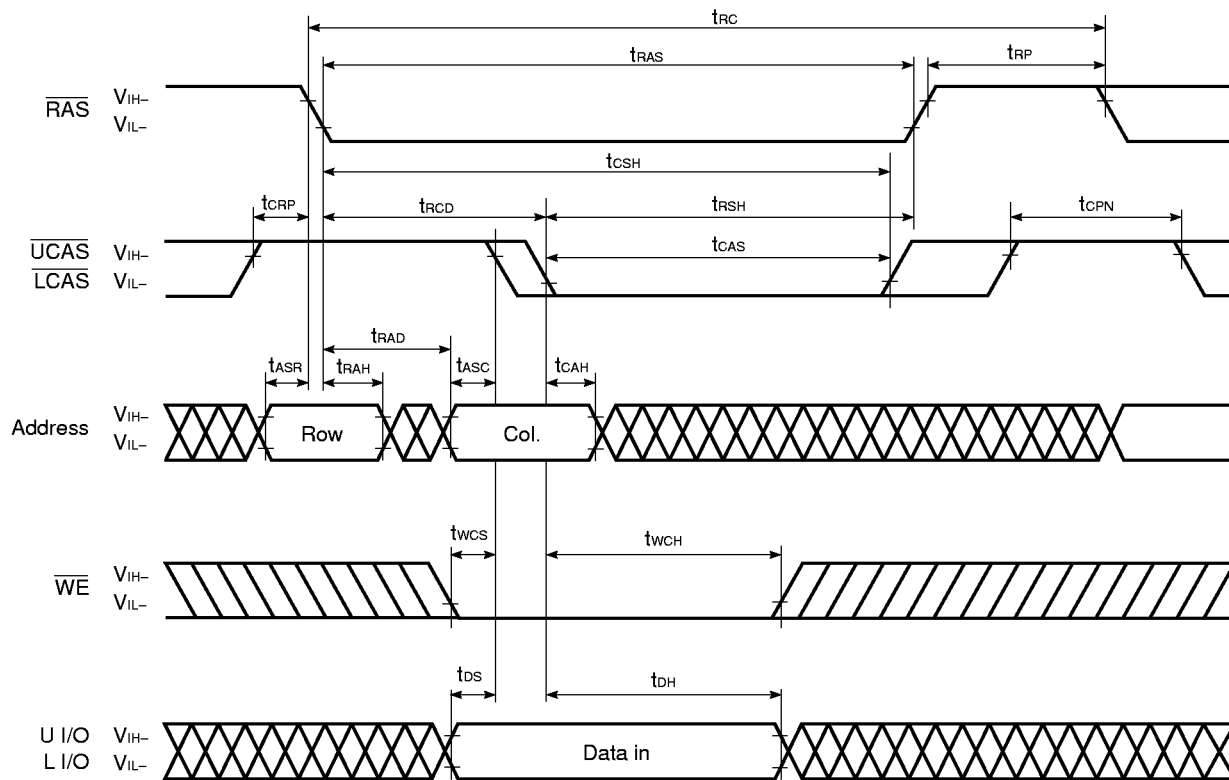
Remark L I/O: Hi-Z

Lower Byte Read Cycle



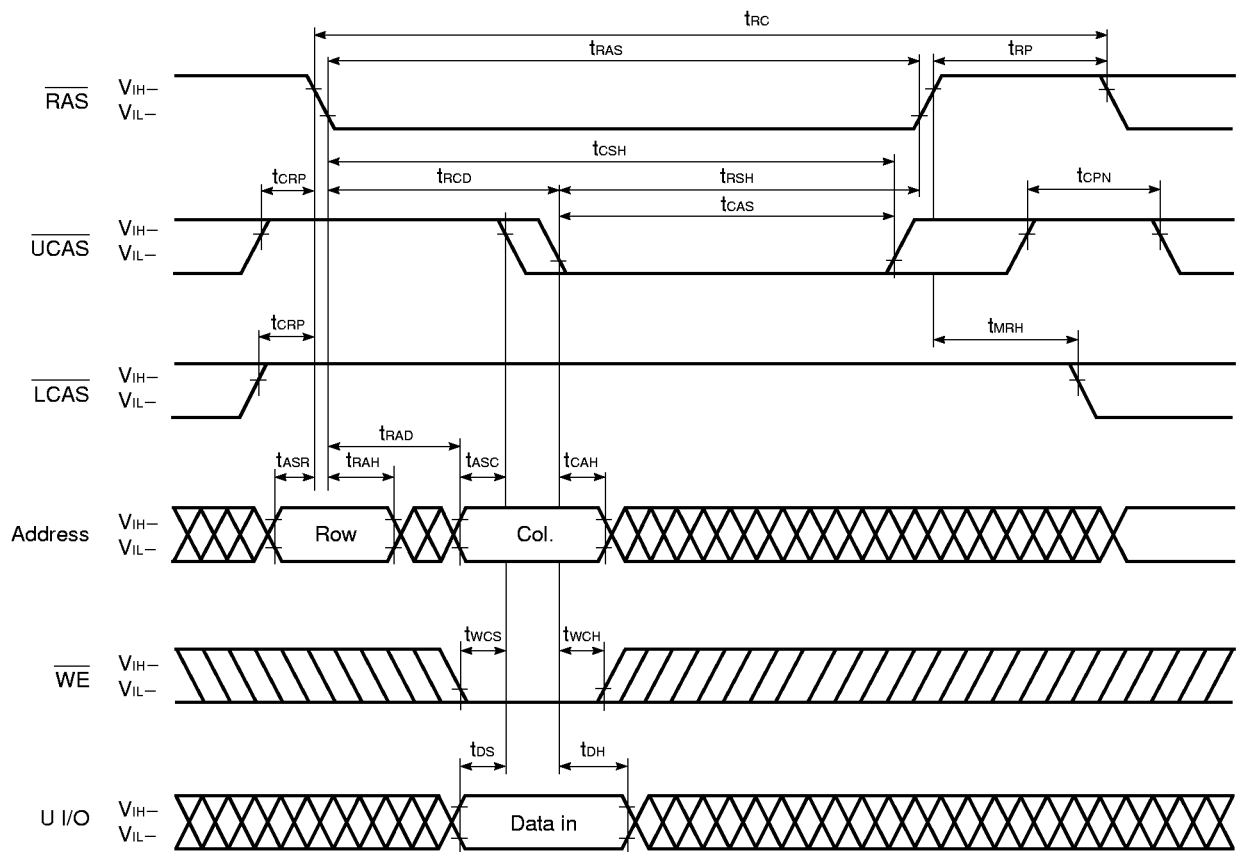
Remark U I/O: Hi-Z

Early Write Cycle



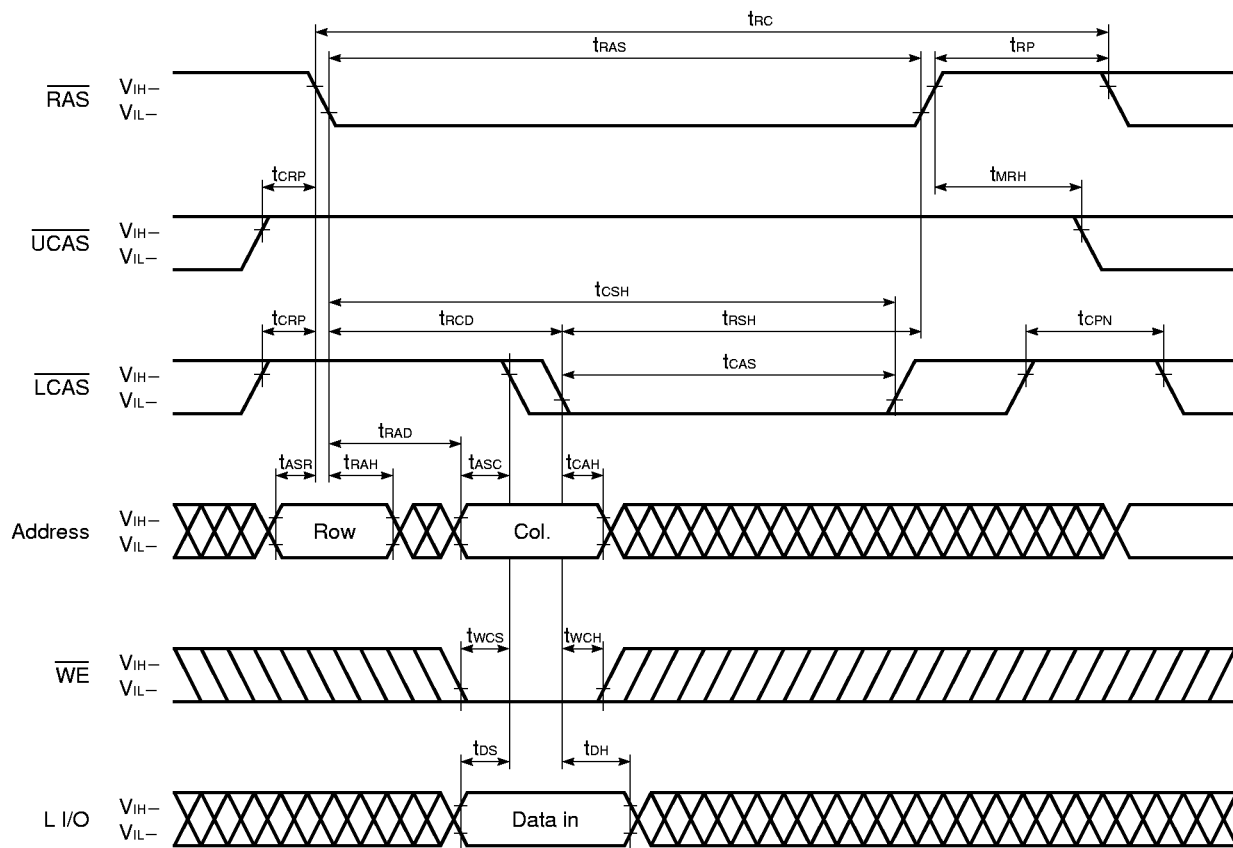
Remark $\overline{\text{OE}}$: Don't care

Upper Byte Early Write Cycle



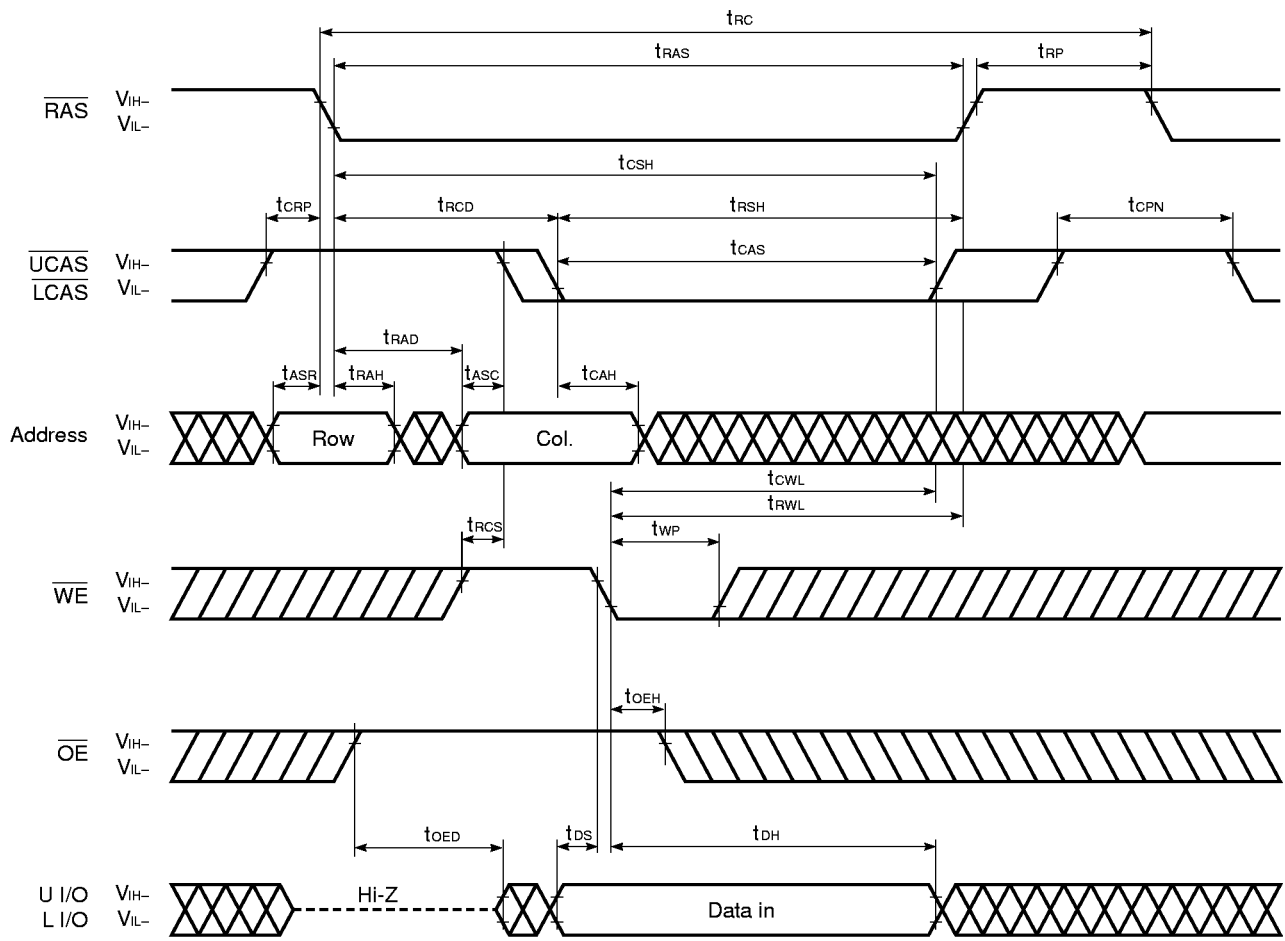
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

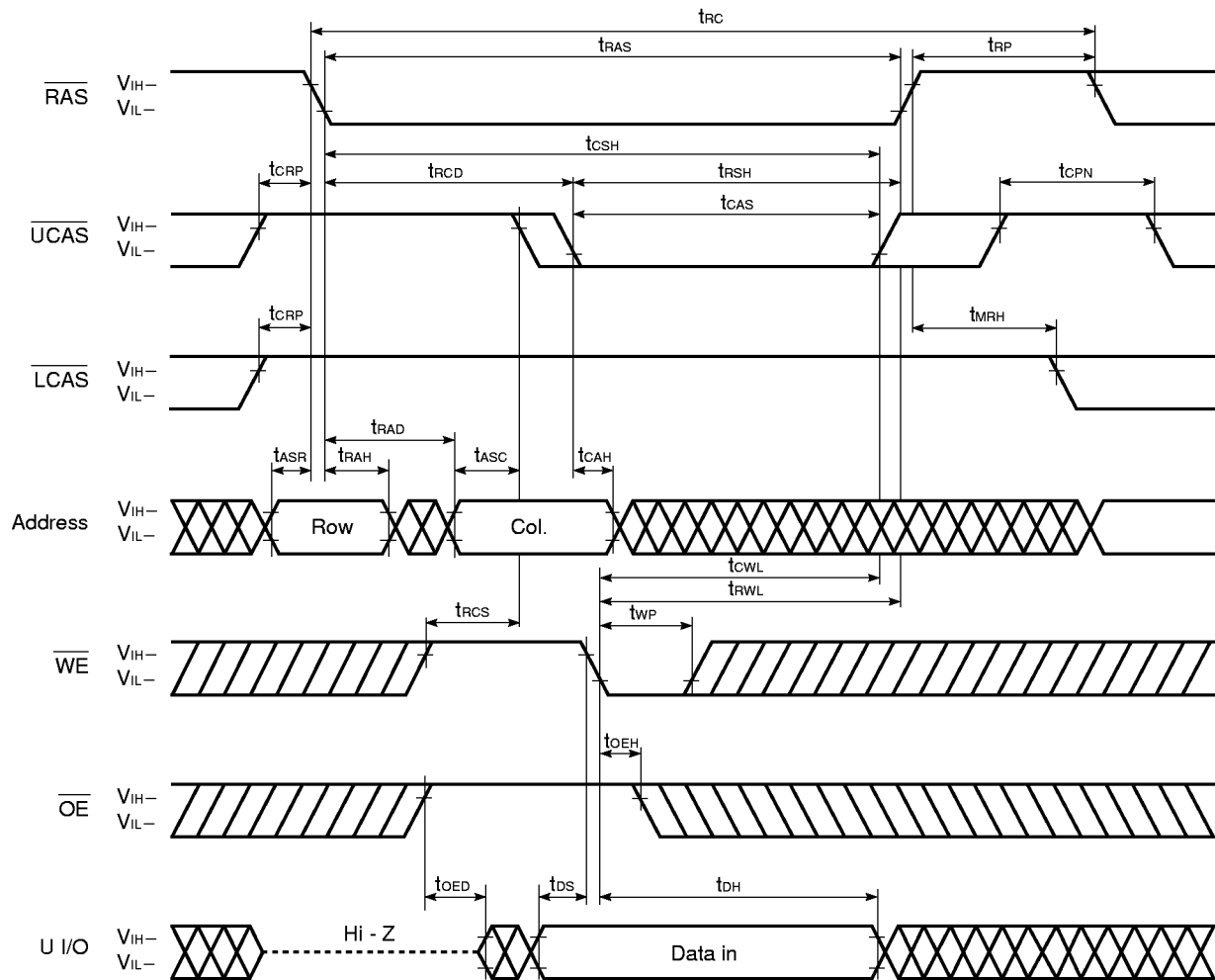


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

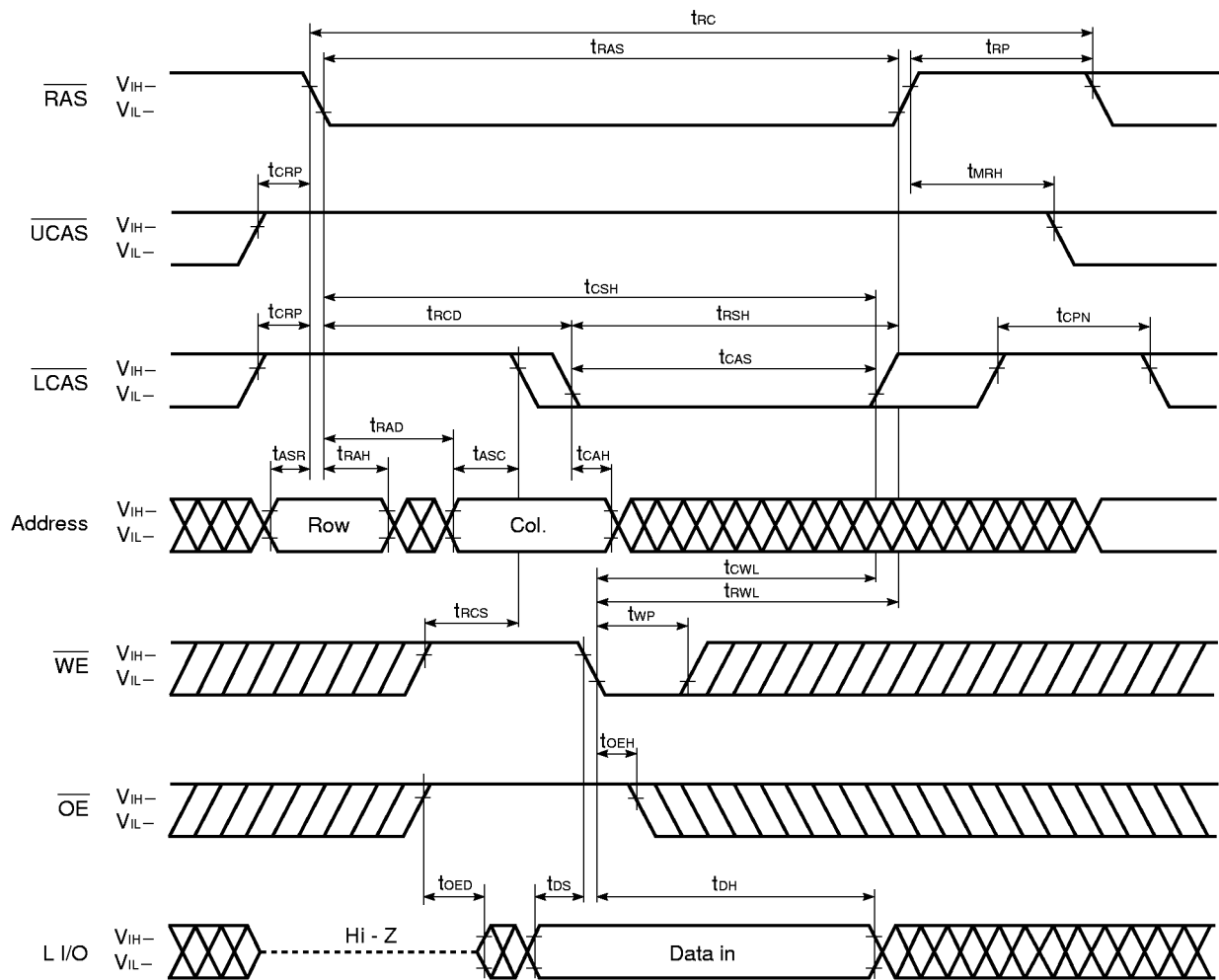


Upper Byte Late Write Cycle



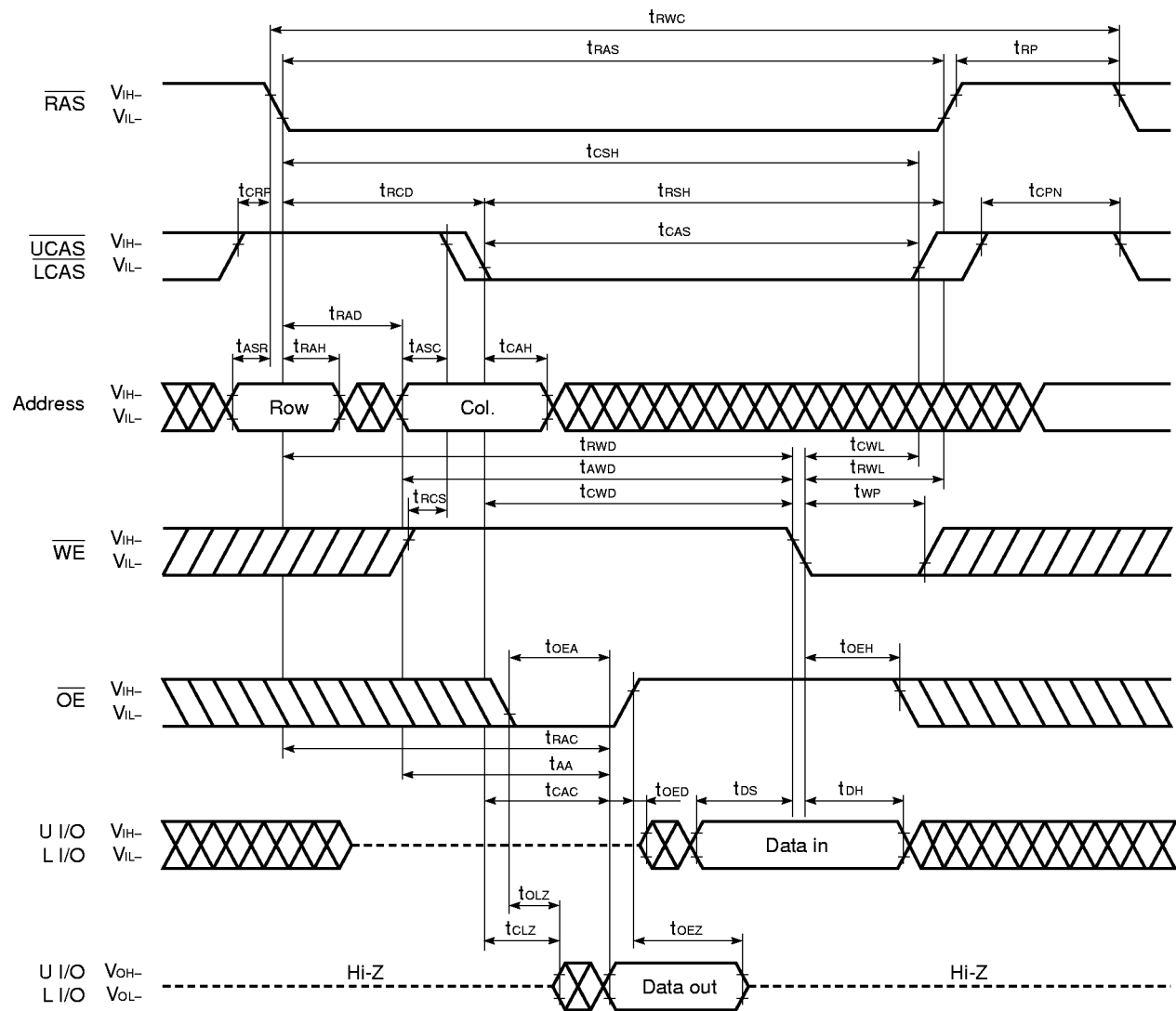
Remark L I/O: Don't care

Lower Byte Late Write Cycle

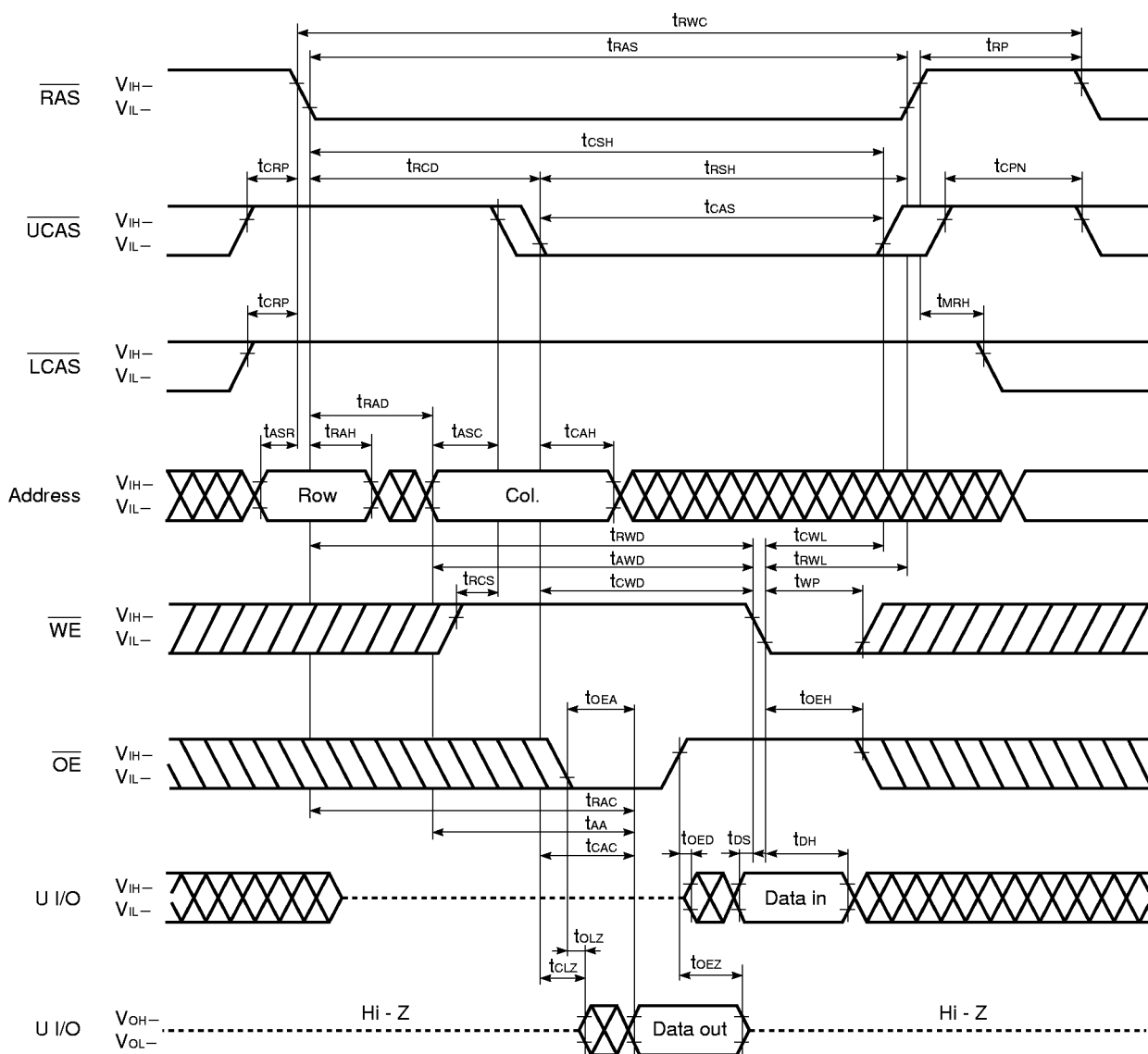


Remark U I/O: Don't care

Read Modify Write Cycle



Upper Byte Read Modify Write Cycle



Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

[illegible]

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The timing diagram illustrates the relationship between several control and data signals over time. The signals shown are:

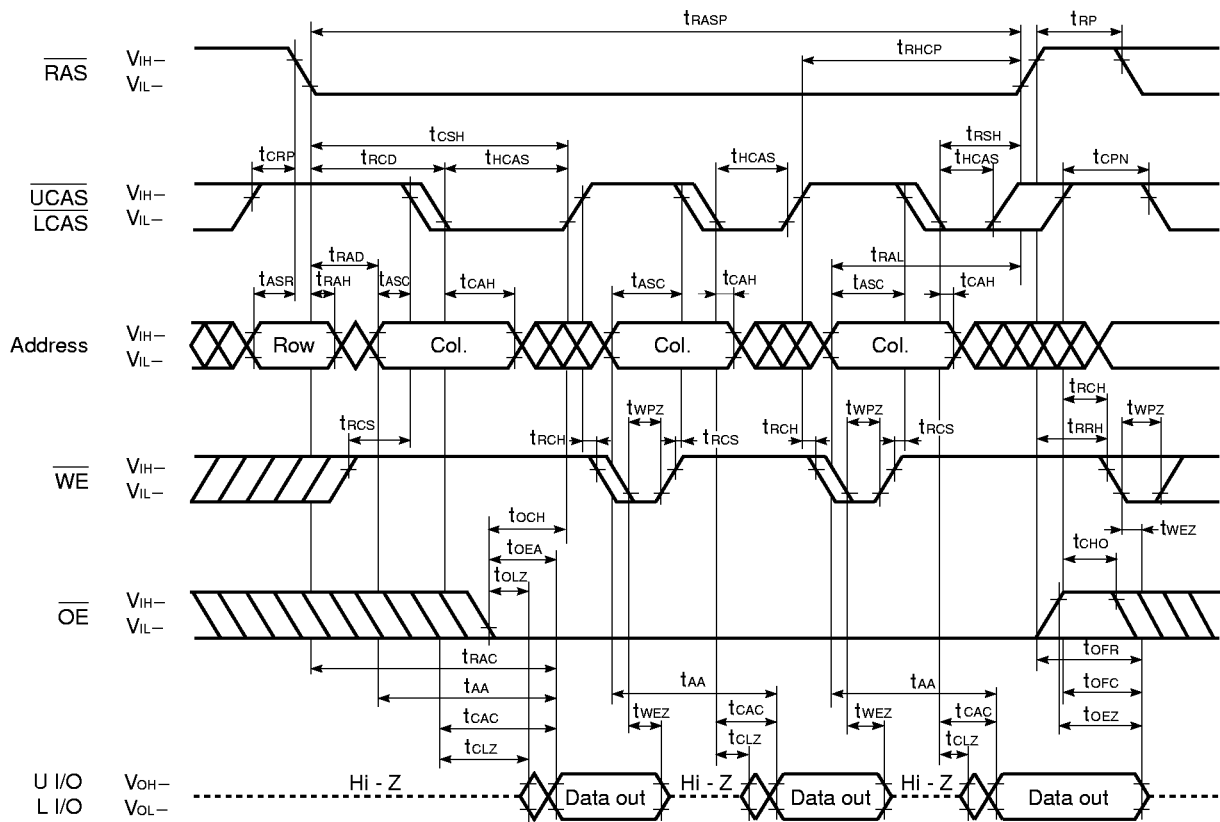
- RAS**: Active-low chip select signal.
- UCAS**: Active-low user chip select signal.
- LCAS**: Active-low local chip select signal.
- Address**: Multiplexer address signal, with fields for Row and Column (Col.).
- WE**: Active-low write enable signal.
- OE**: Active-low output enable signal.
- U I/O**: User input/output bus, shown as Hi-Z (high impedance) during certain periods.
- L I/O**: Local input/output bus, also shown as Hi-Z during certain periods.

Key timing parameters labeled include:

- t_{RASP} , t_{RHCP} , t_{RP}
- t_{CRP} , t_{CSH} , t_{RCD} , t_{HCAS} , t_{HPC} , t_{RSH} , t_{HCAS} , t_{CPN}
- t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{TSC} , t_{AL} , t_{OFR} , t_{OFC}
- t_{CH} , t_{RRH} , t_{WPZ} , t_{CHO} , t_{WEZ}
- t_{TOEA} , t_{ACP} , t_{AAC} , t_{CAC} , t_{DHC} , t_{TOEZ}
- t_{TRAC} , t_{TAA} , t_{TCAC} , t_{TCLZ}

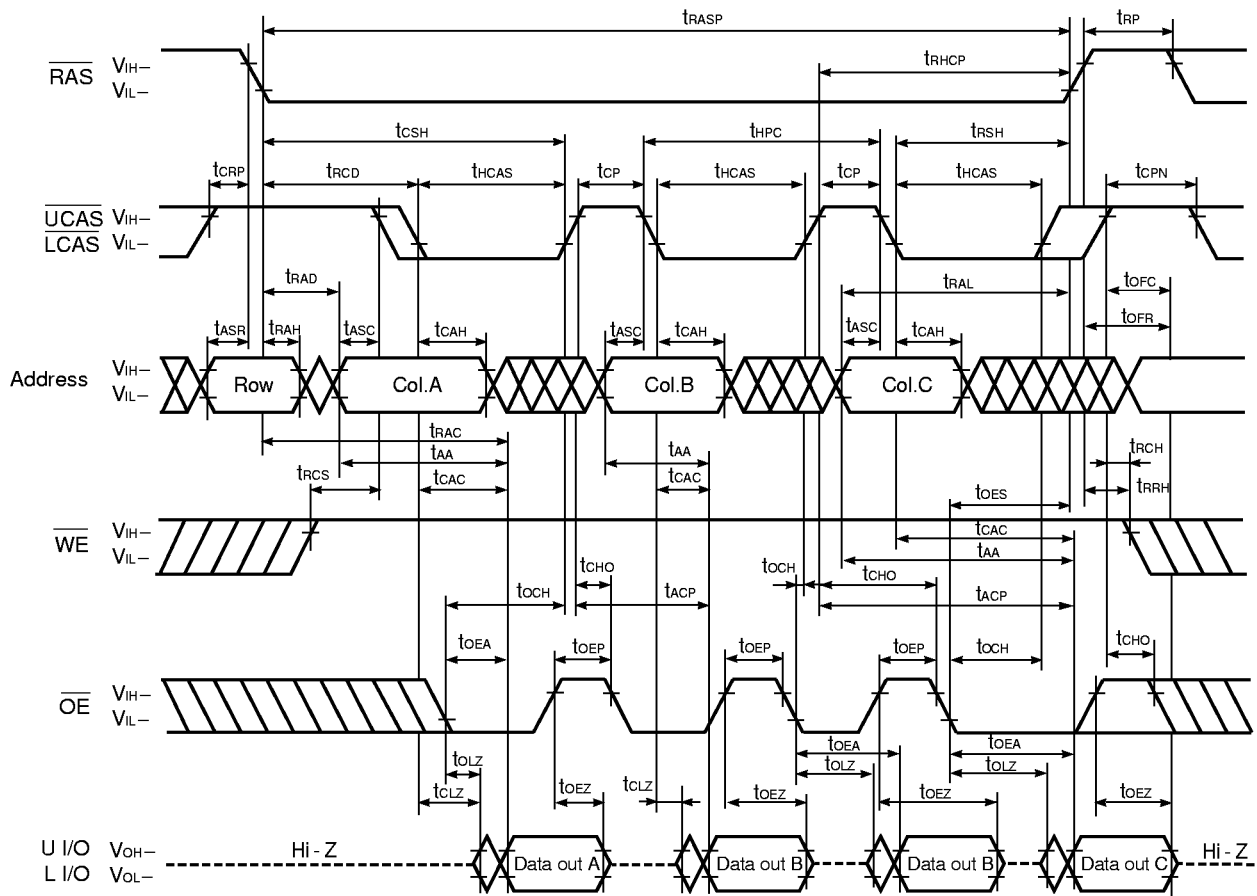
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Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)



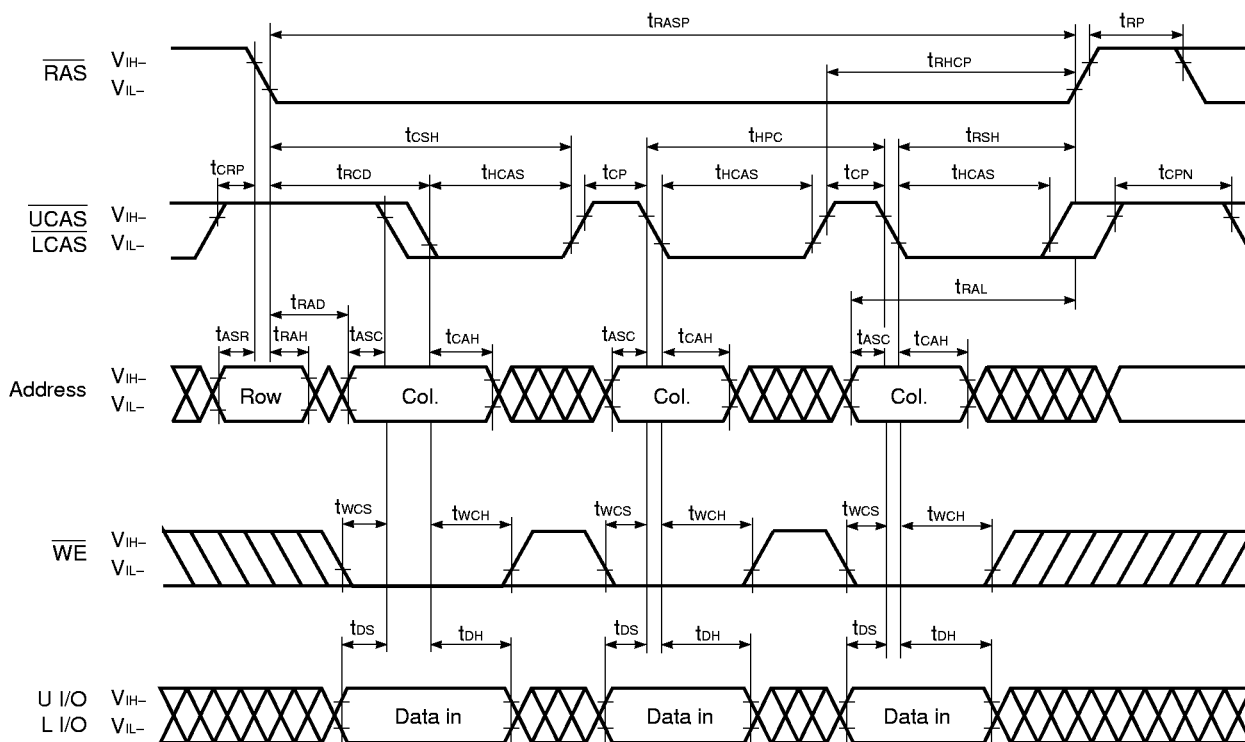
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

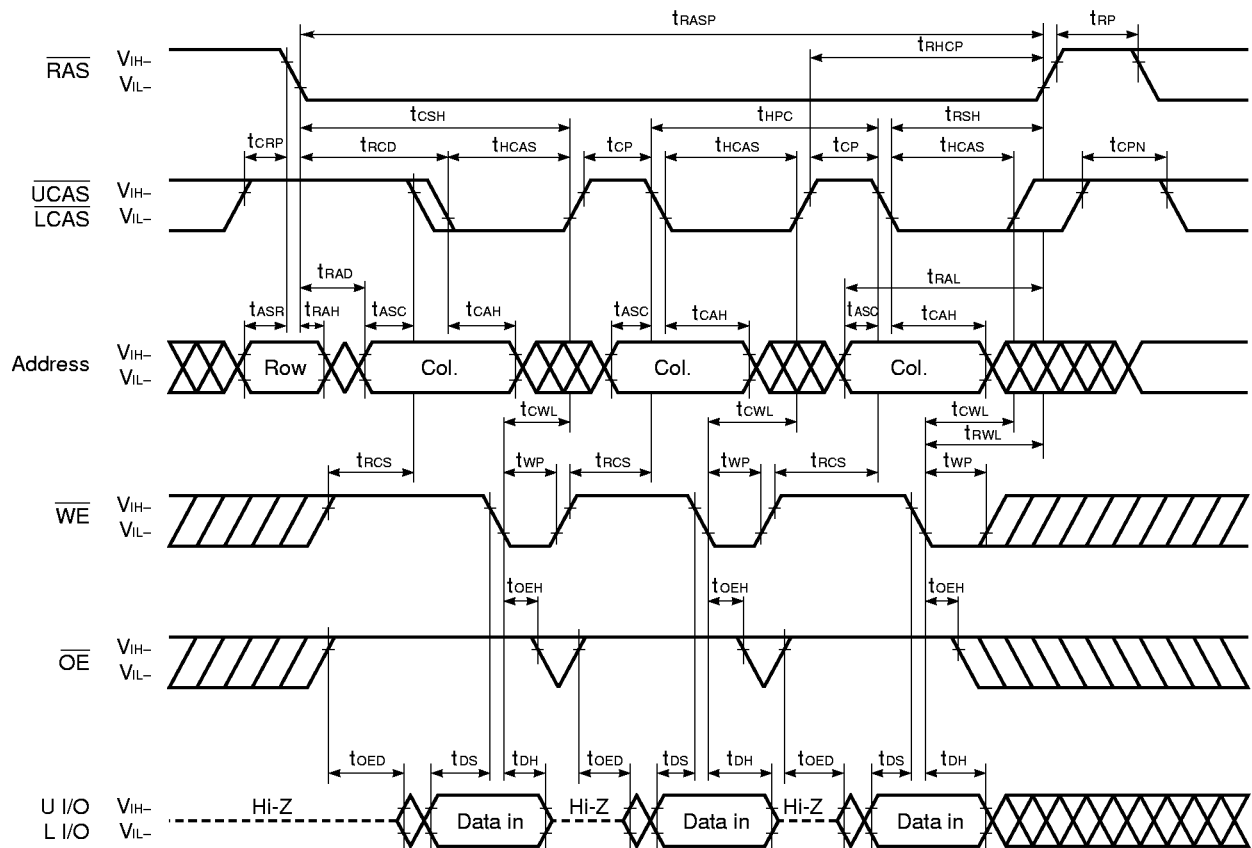
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

The diagram illustrates the timing relationships for a memory device. The signals and their timing parameters are as follows:

- RAS**: $\overline{V_{IH}}$, V_{IL} . Timing parameters: t_{RAS} (total pulse width), t_{RHP} (pulse height), t_{RP} (pulse period), t_{CRP} (setup time before RAS), t_{RCD} (column address delay), t_{CSH} (row address setup), t_{HPC} (row address hold), t_{RSH} (row address setup), t_{HCAS} (column address setup), t_{CPN} (column address period), t_{CP} (column address period), t_{MRH} (memory refresh hold).
- UCAS**: V_{IH} , V_{IL} . Timing parameters: t_{CRP} (setup time before UCAS), t_{CP} (column address period), t_{HCAS} (column address setup), t_{CP} (column address period).
- LCAS**: V_{IH} , V_{IL} . Timing parameters: t_{CRP} (setup time before LCAS), t_{CP} (column address period), t_{HCAS} (column address setup), t_{CP} (column address period).
- Address**: V_{IH} , V_{IL} . Timing parameters: t_{ASR} (address setup), t_{RAH} (row address hold), t_{ASC} (address setup), t_{CAH} (column address hold), t_{RAD} (row address delay), t_{RAL} (row address delay).
- WE**: V_{IH} , V_{IL} . Timing parameters: t_{wCS} (write enable setup), t_{wCH} (write enable hold), t_{wCS} (write enable setup), t_{wCH} (write enable hold), t_{wCS} (write enable setup), t_{wCH} (write enable hold).
- U I/O**: V_{IH} , V_{IL} . Timing parameters: t_{ds} (data setup), t_{dH} (data hold), t_{ds} (data setup), t_{dH} (data hold).
- L I/O**: V_{IH} , V_{IL} . Timing parameters: t_{ds} (data setup), t_{dH} (data hold).

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
3. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

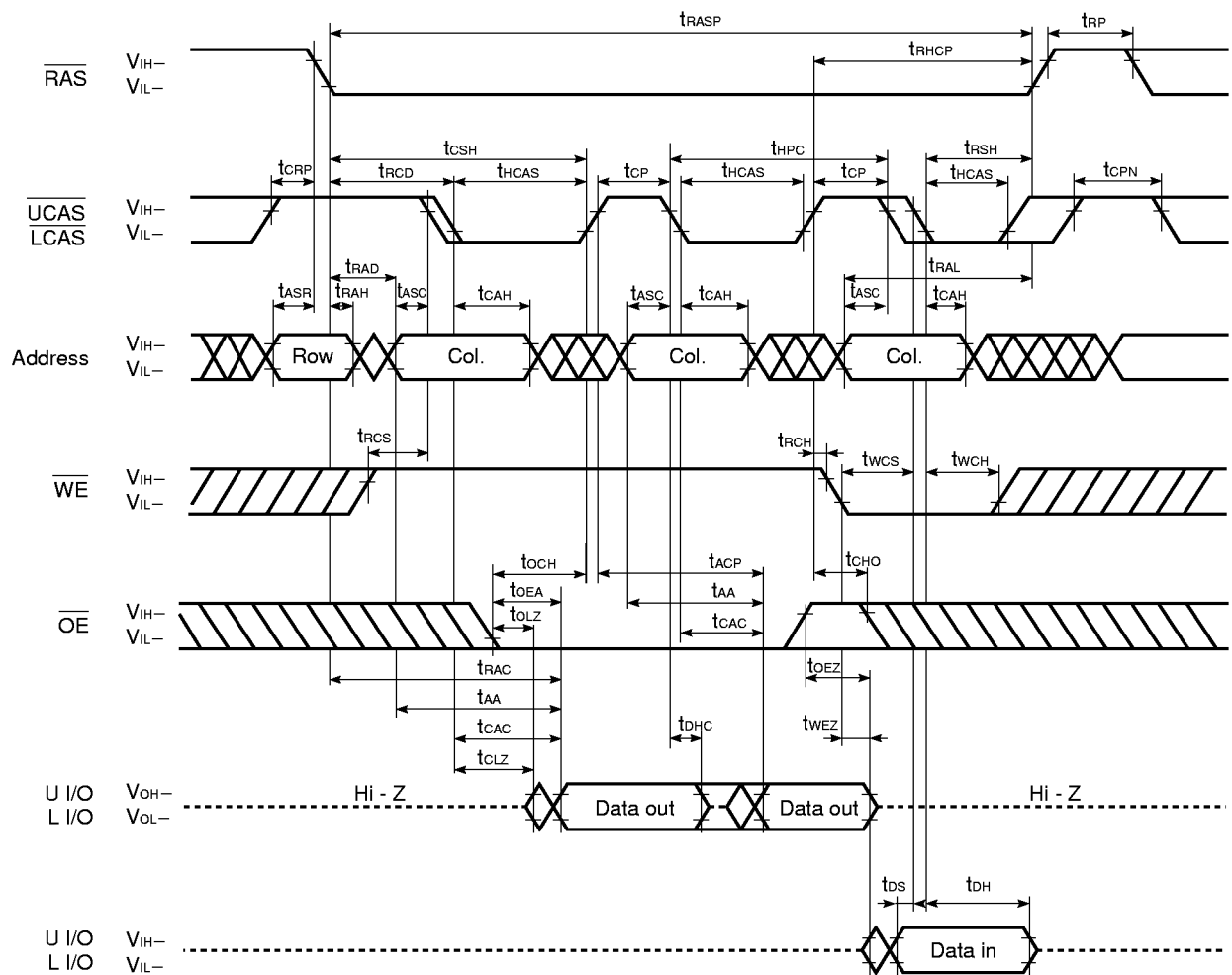
[illegible]

- Remarks 1.** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

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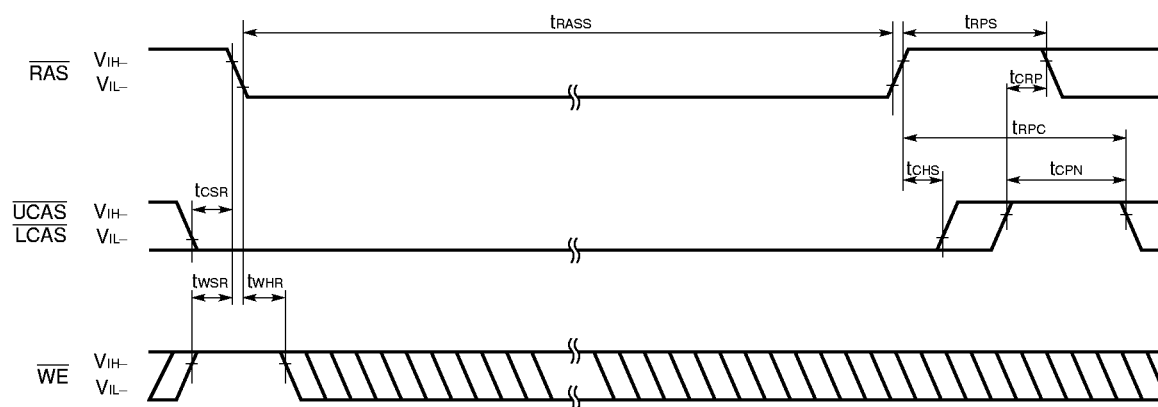
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Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S65165)



Remark Address, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 4,096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh 4,096 times within a 64 ms interval just before and after setting CAS before RAS self refresh.

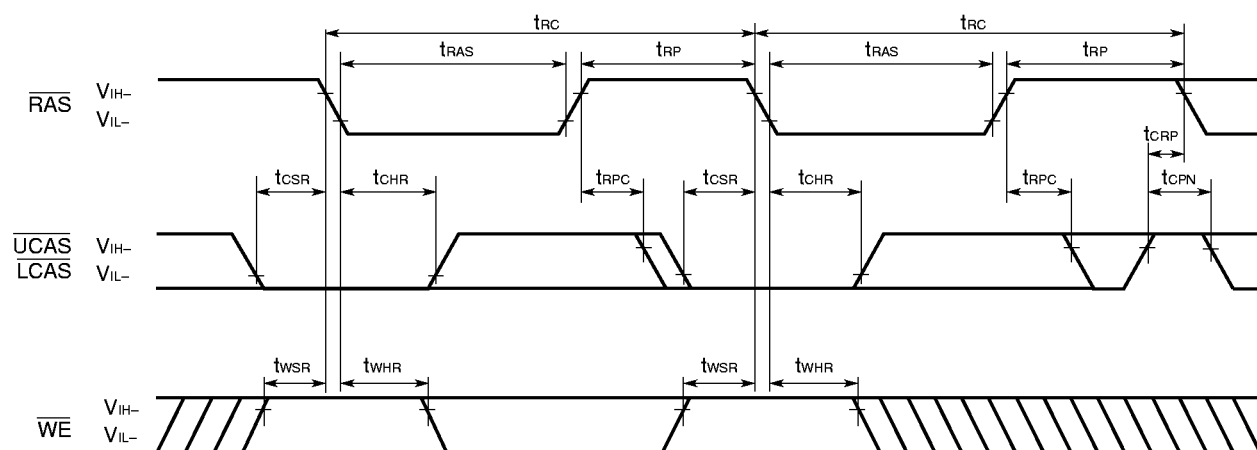
(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied.

And refresh cycles (4,096/128 ms) should be met.

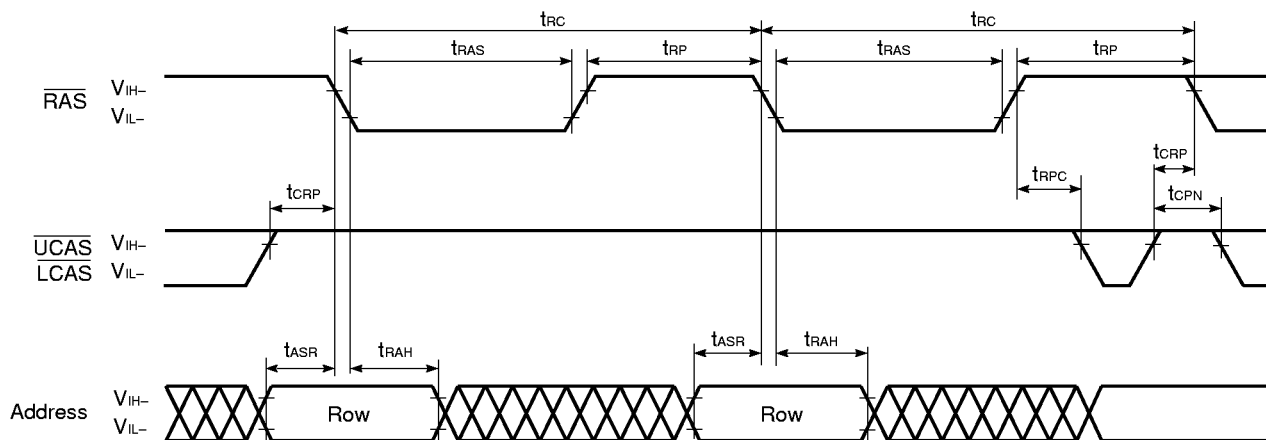
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



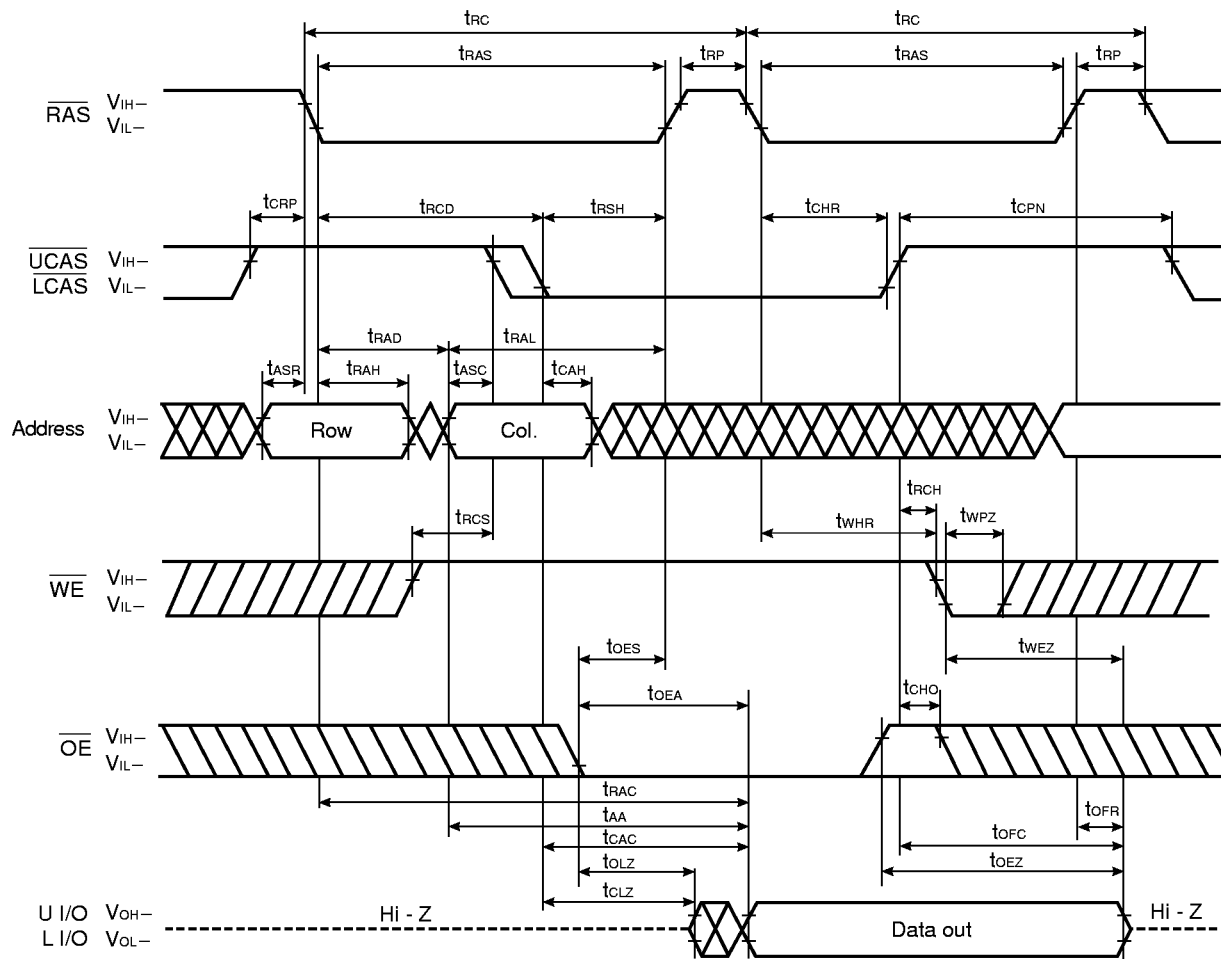
Remark Address, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

$\overline{\text{RAS}}$ Only Refresh Cycle

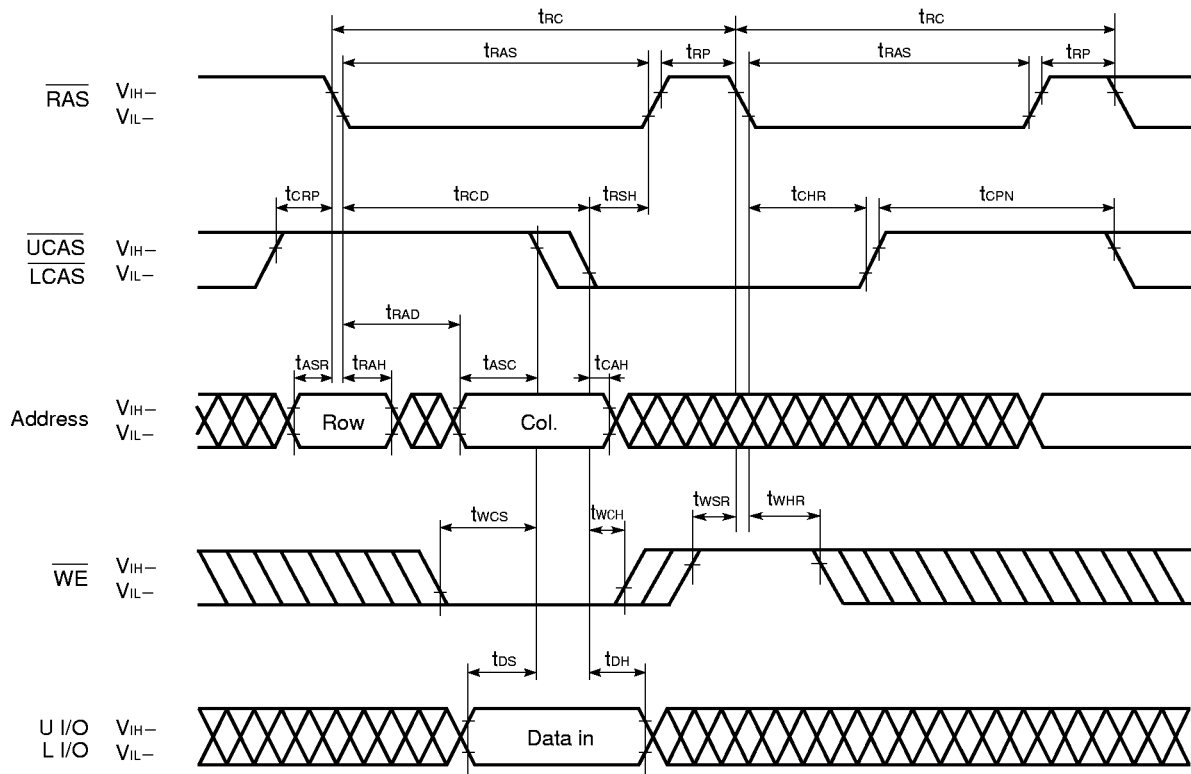


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



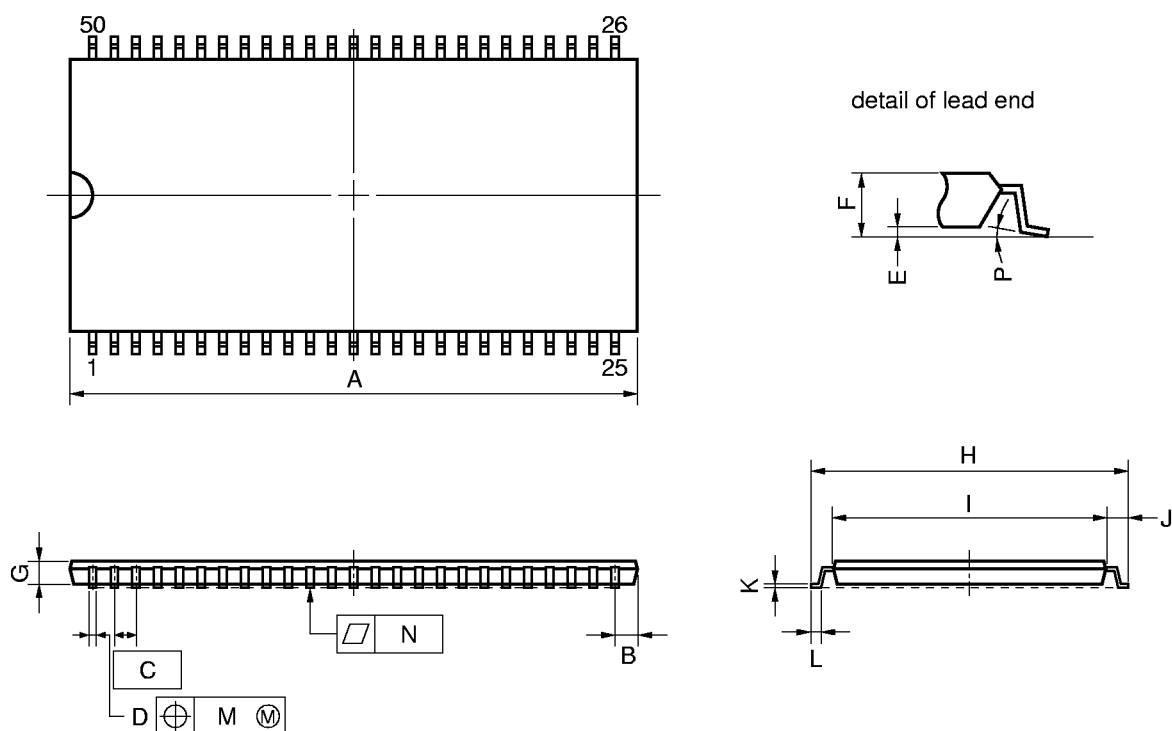
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawing

50PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD42S65165, 4265165.

Type of Surface Mount Device

μ PD42S65165G5-7JF, 4265165G5-7JF: 50-pin plastic TSOP (II) (400 mil)