μPD424412
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424412 is a static-column 1,048,576 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

Features

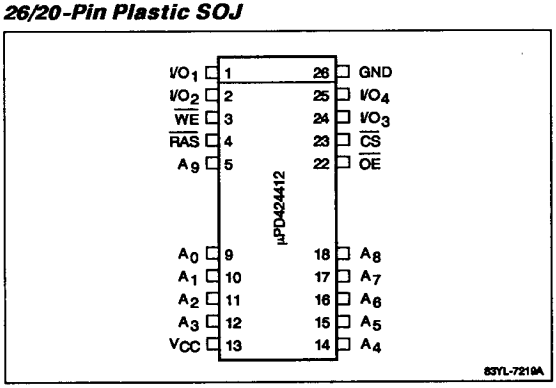
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- High-density 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

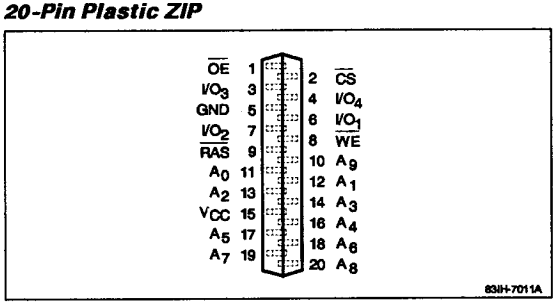
Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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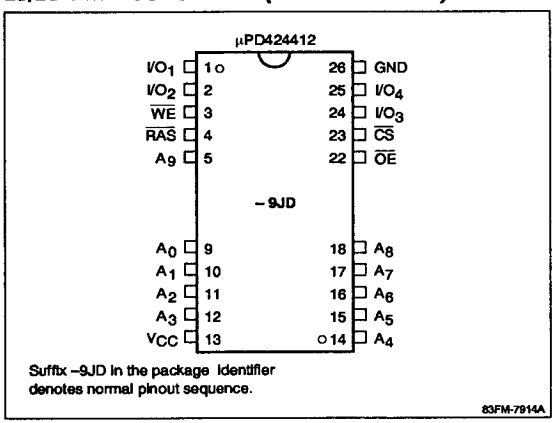
Pin Configurations (cont)

26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

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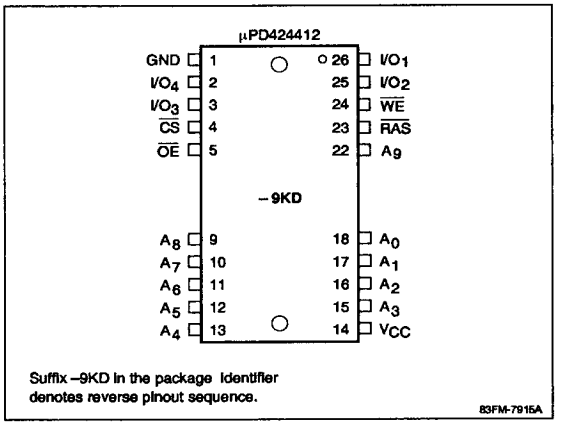
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

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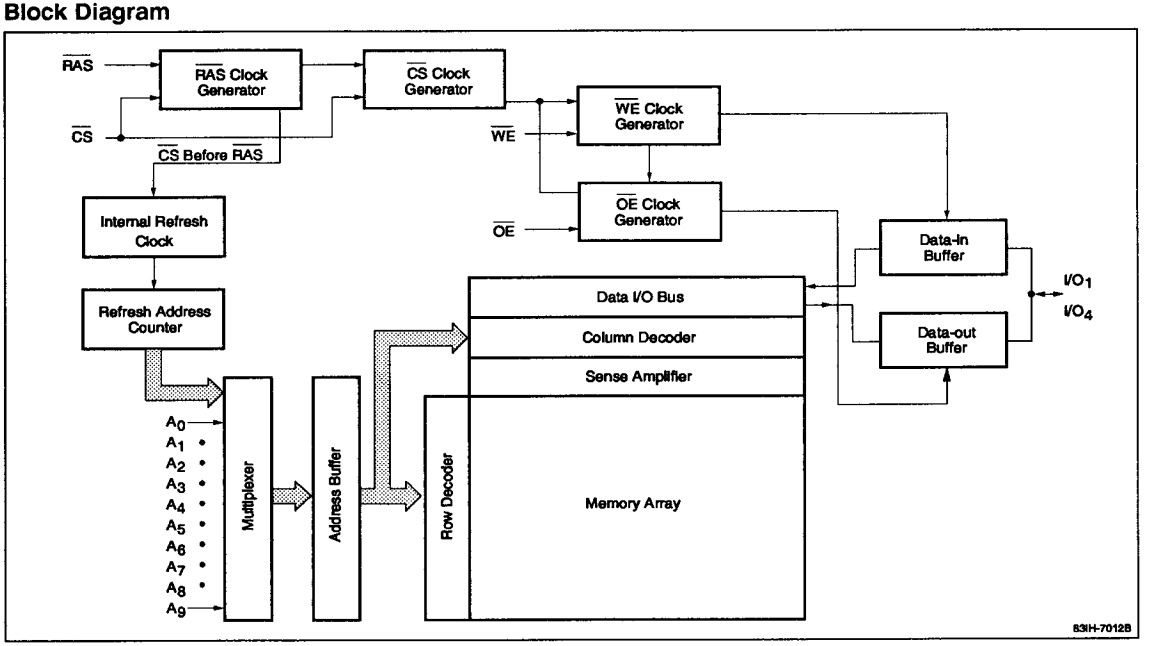
Block Diagram



Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Power Option	Package
μPD424412LA-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424412LA-60L	60 ns	120 ns	35 ns	Low power	
LA-70L	70 ns	140 ns	40 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424412V-60	60 ns	120 ns	35 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424412V-60L	60 ns	120 ns	35 ns	Low power	
V-70L	70 ns	140 ns	40 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424412GS-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns		
GS-80	80 ns	160 ns	50 ns		
μPD424412GS-60L	60 ns	120 ns	35 ns	Low power	
GS-70L	70 ns	140 ns	40 ns		
GS-80L	80 ns	160 ns	50 ns		
μPD424412GSM-60	60 ns	120 ns	35 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns		
GSM-80	80 ns	160 ns	50 ns		
μPD424412GSM-60L	60 ns	120 ns	35 ns	Low power	
GSM-70L	70 ns	140 ns	40 ns		
GSM-80L	80 ns	160 ns	50 ns		

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 – I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Low Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; $\overline{WE}$, $\overline{OE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; I/O open
	300	μA	≤ 200 ns		

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		90		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Colum address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		55		65		80		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		40		45		55		ns	(Note 15)
Write command referenced to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output hold time for address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		30	ns	
Access time from $\overline{WE}$	t_{PWA}		60		70		90		110	ns	(Notes 7, 16)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 12)
Read cycle time	t_{RSC}	35		40		50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-modify-write cycle time	t_{RWC}	145		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		90		105		130		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Read/write cycle time	t_{RWSC}	65		95		120		145		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 16)
Write-per-bit hold time	t_{WBH}	15		15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write-per-bit setup time	t_{WBS}	10		10		10		10		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 13)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 15)
Write-per-bit mask data hold time	t_{WH}	15		15		15		20		ns	
$\overline{WE}$ command hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		15		15		20		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 13)
Write-per-bit mask data setup time	t_{WS}	10		10		10		10		ns	
Write cycle time	t_{WSC}	35		40		50		60		ns	
$\overline{WE}$ command setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq$ exceeds t_{RAD} max, then t_{RAC} will increase by the amount t_{RCD} exceeds t_{RCD} (max).

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes $t_{WAD} \leq t_{WAD}$ (max).

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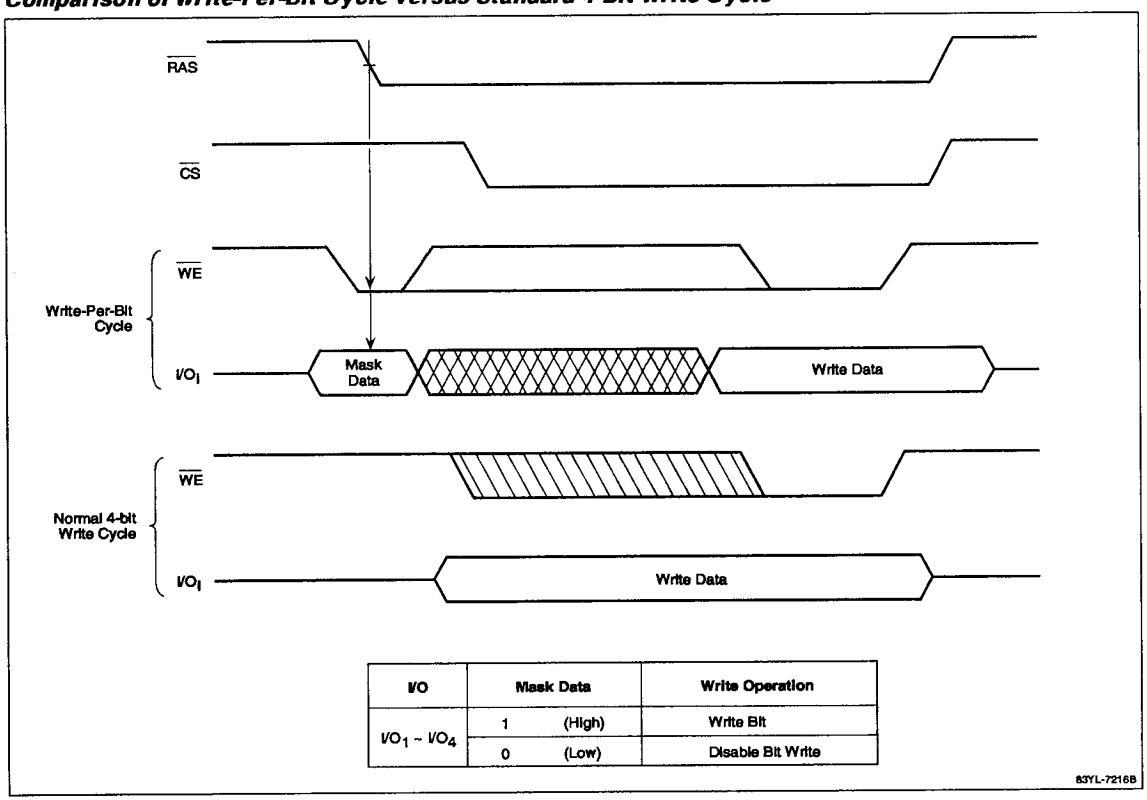
Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE}$ = V_{IL}. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



I/O	Mask Data		Write Operation
I/O_1 ~ I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

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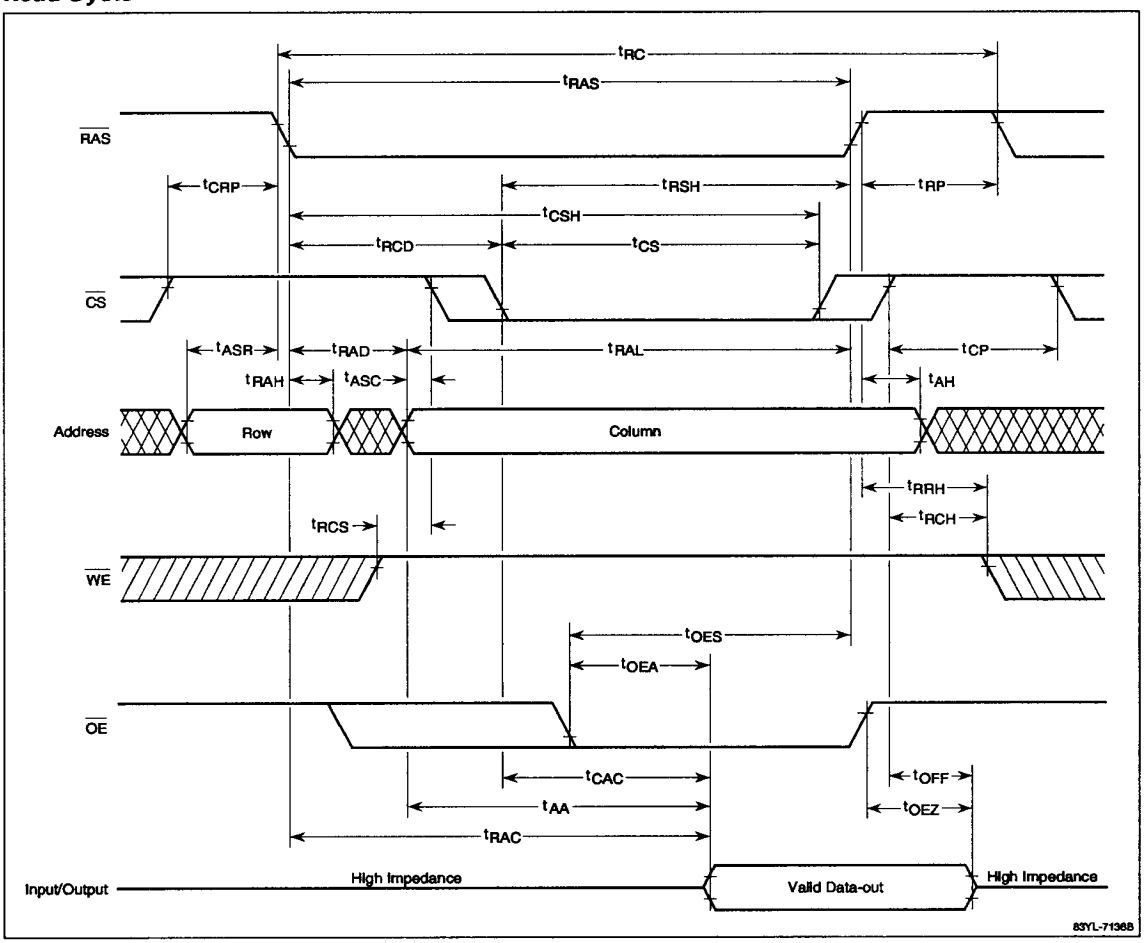
Timing Waveforms

Read Cycle



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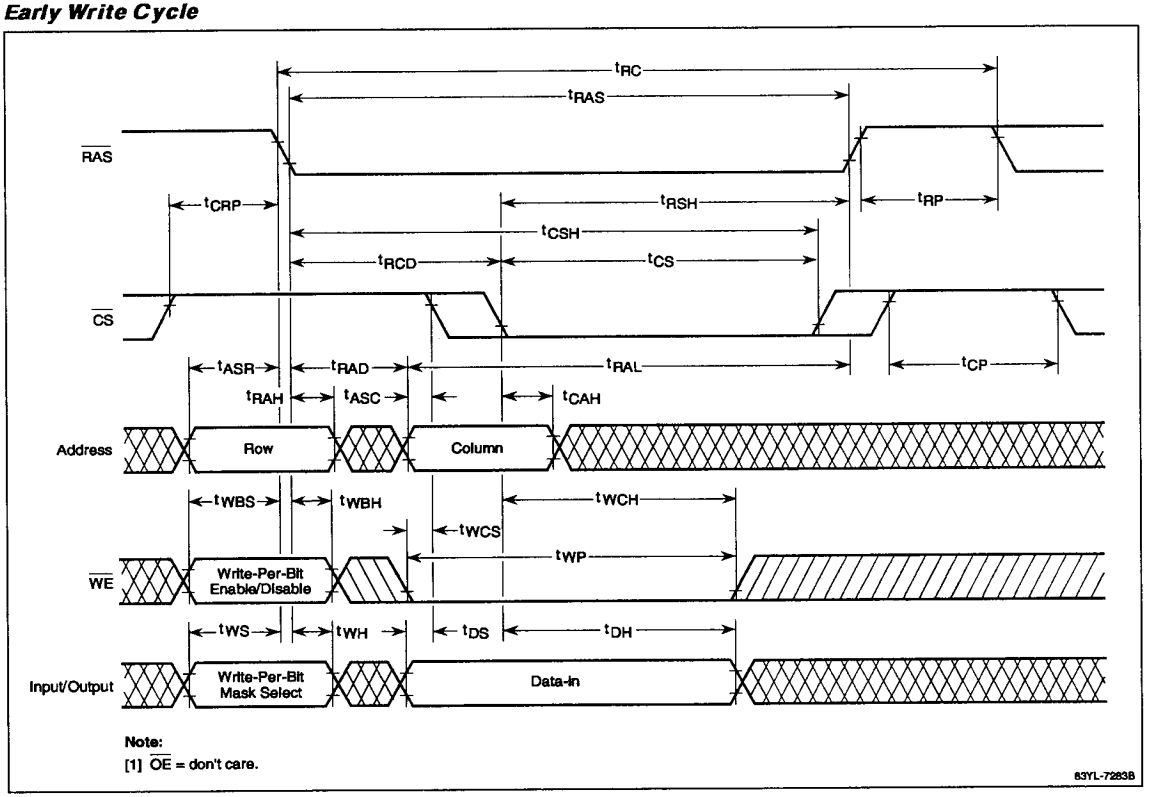
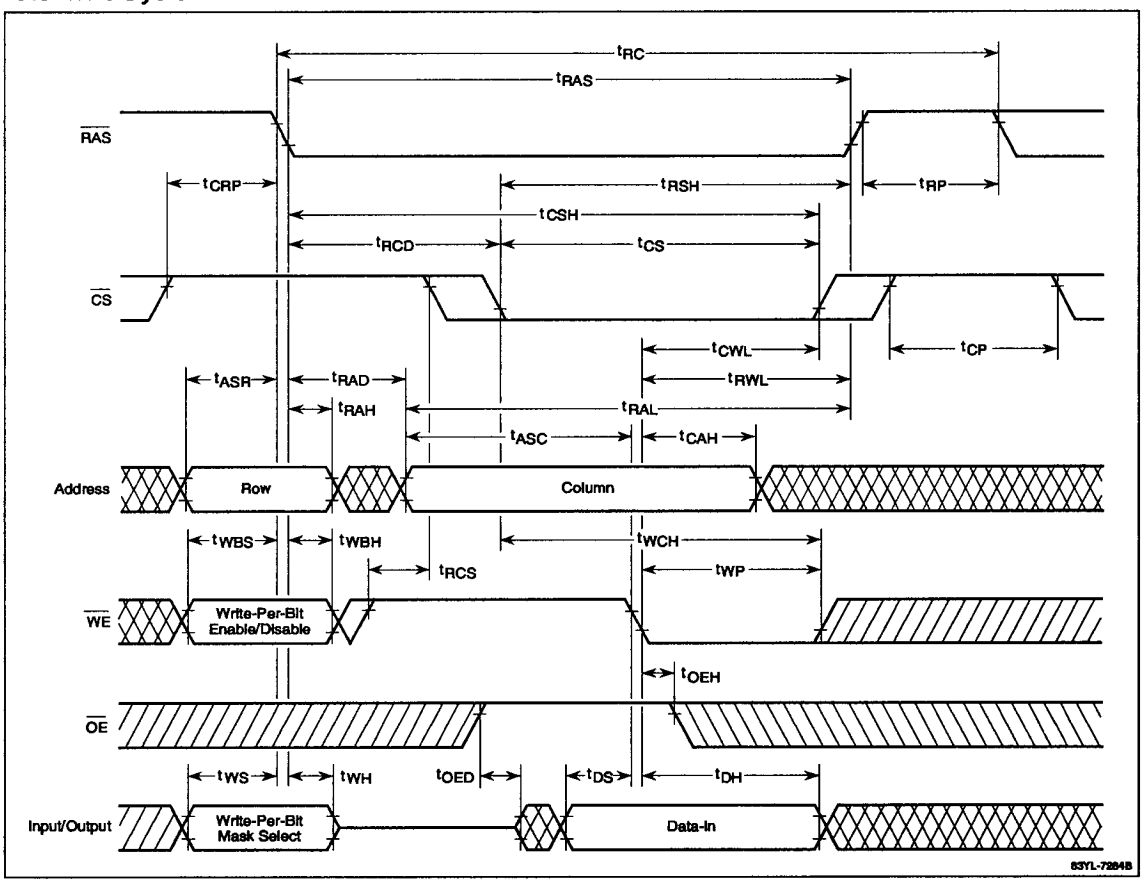
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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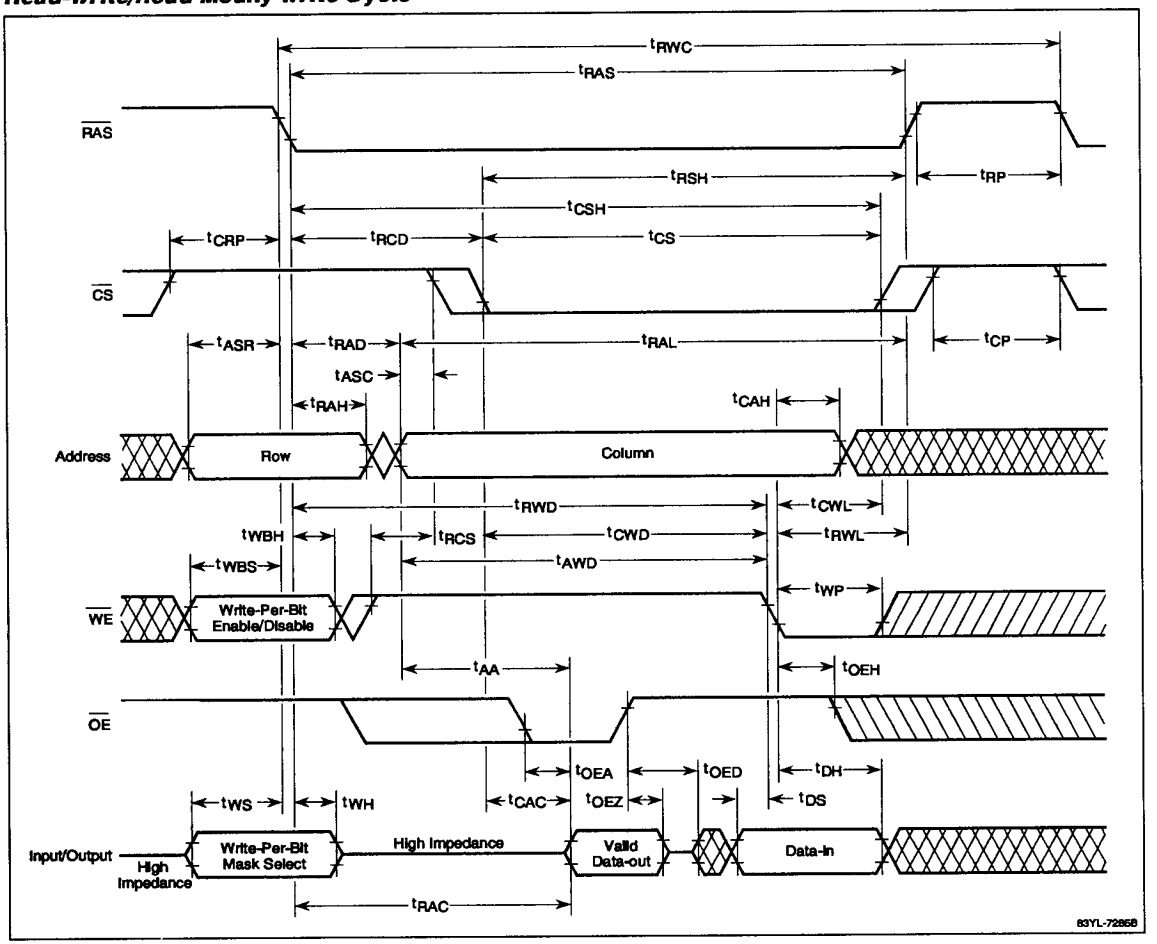
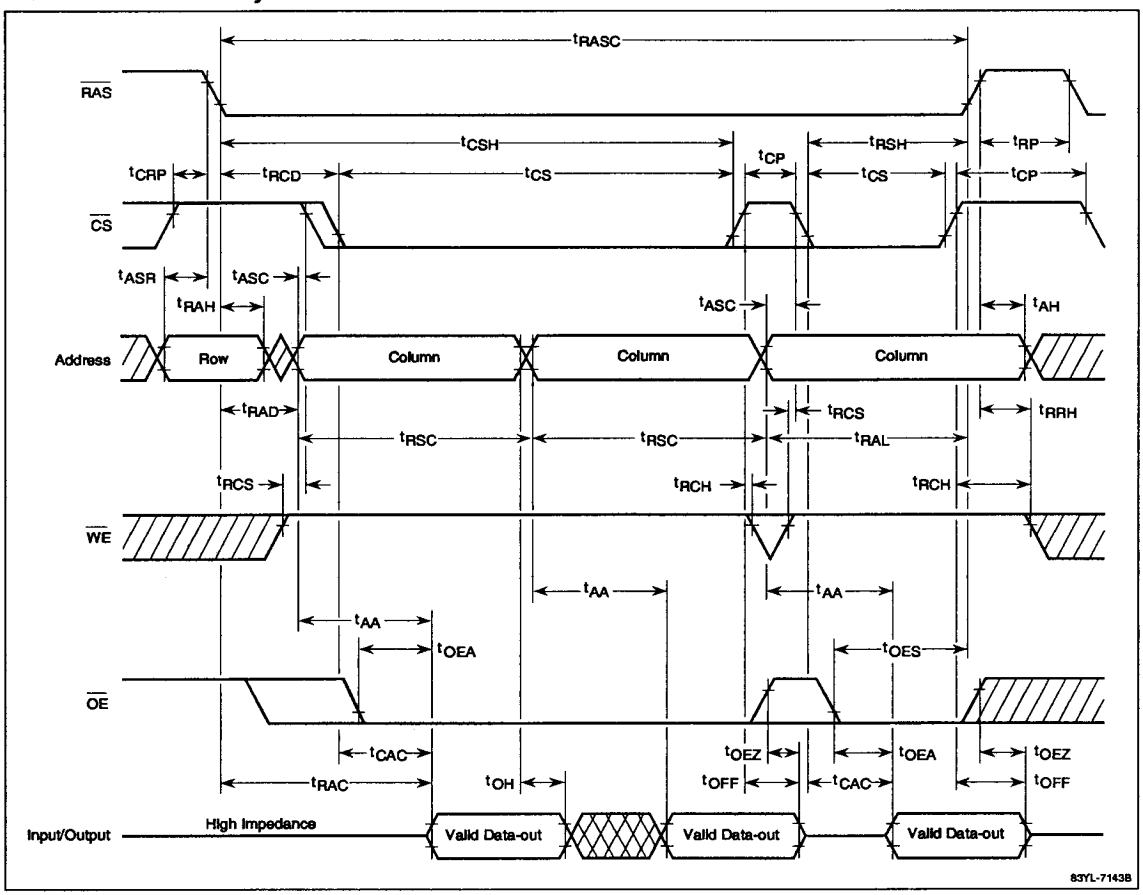
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Static-Column Read Cycle



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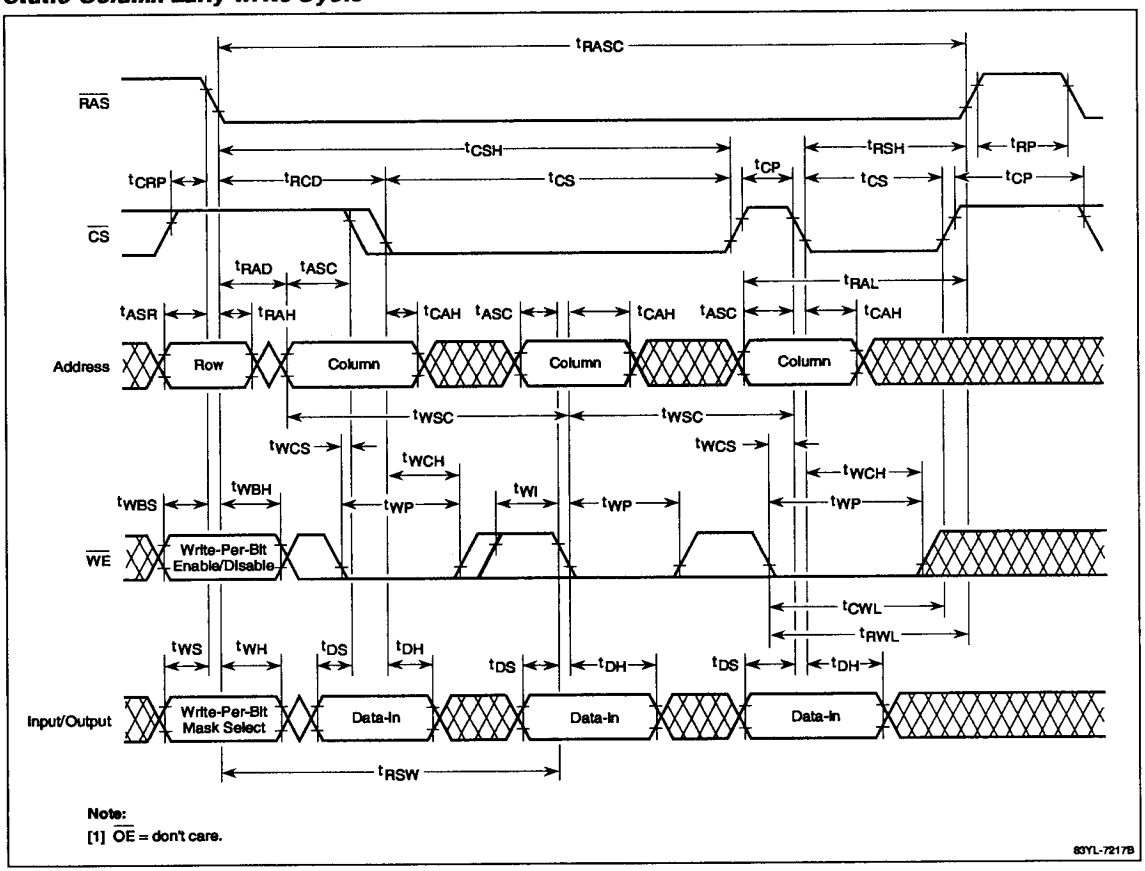
Timing Waveforms (cont)

Static-Column Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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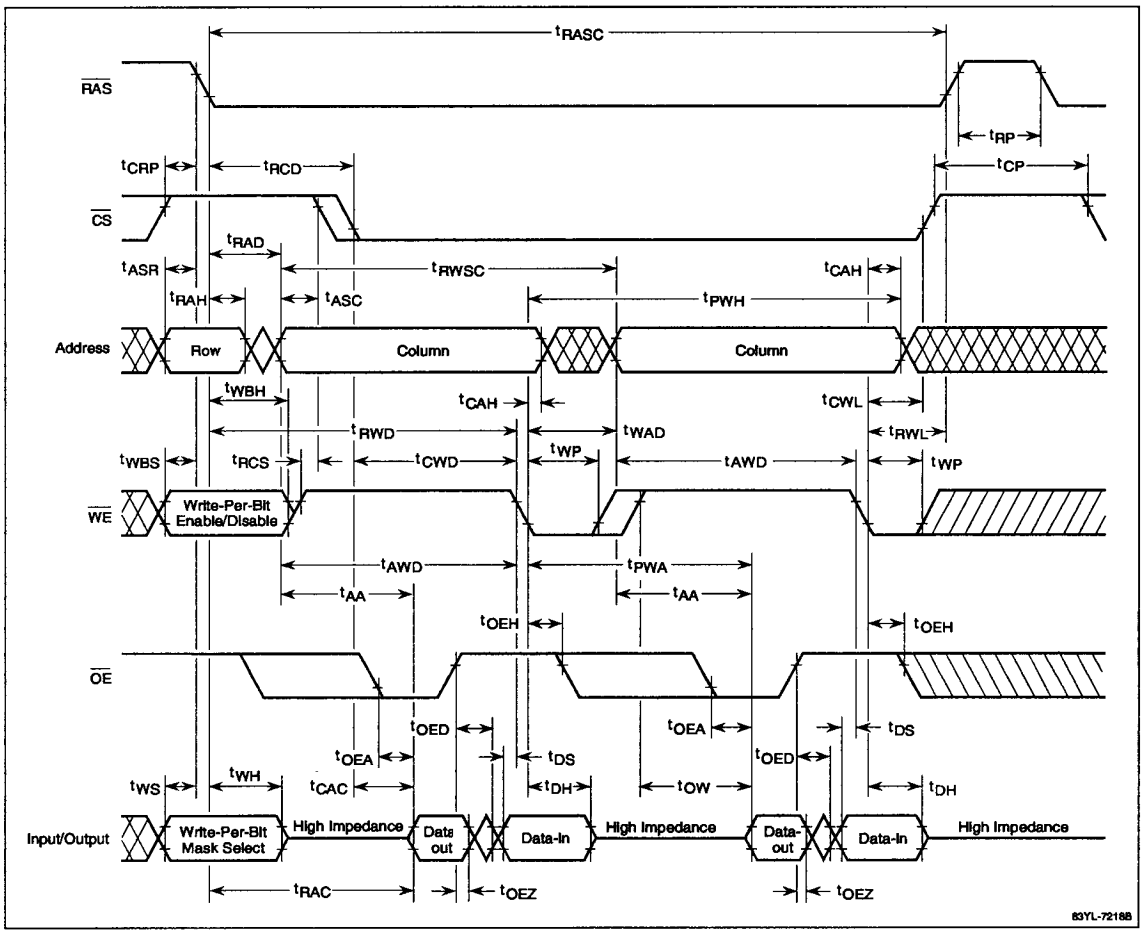
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



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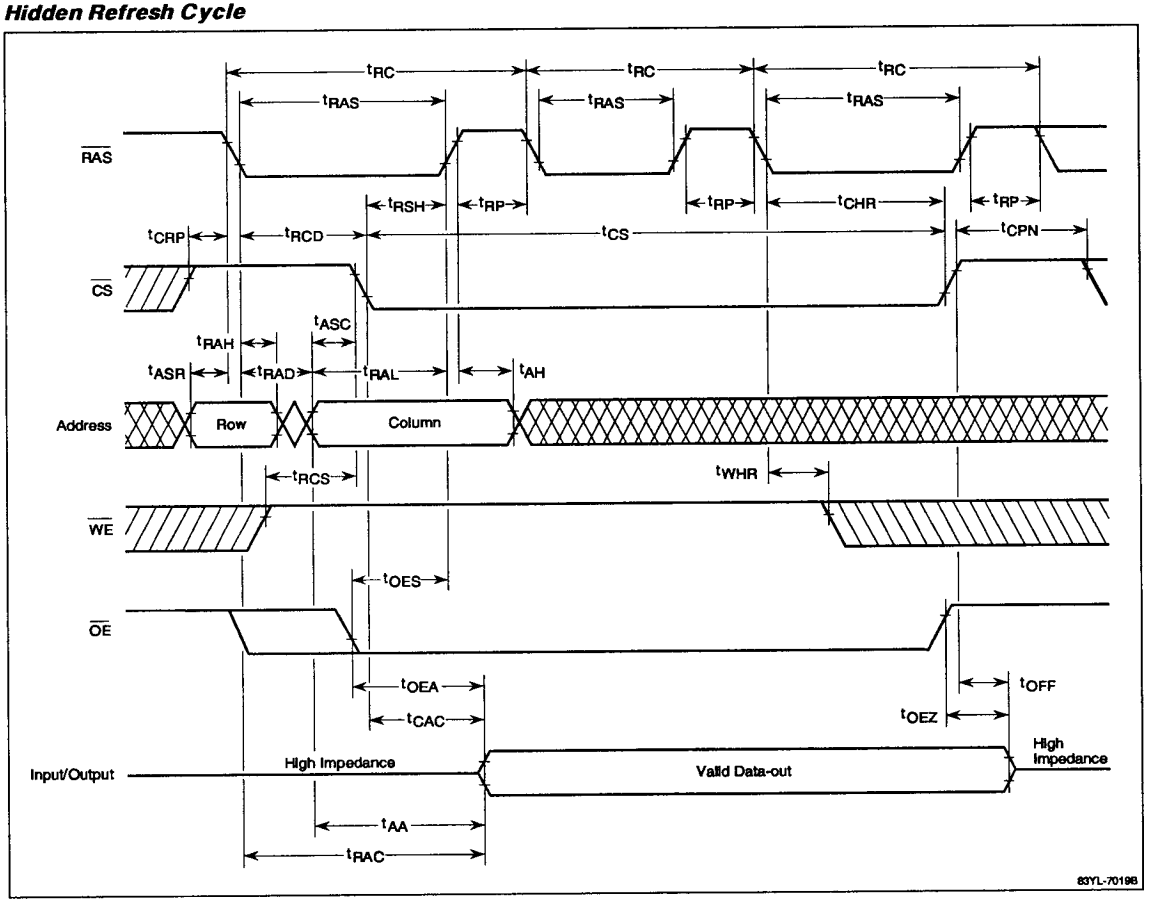
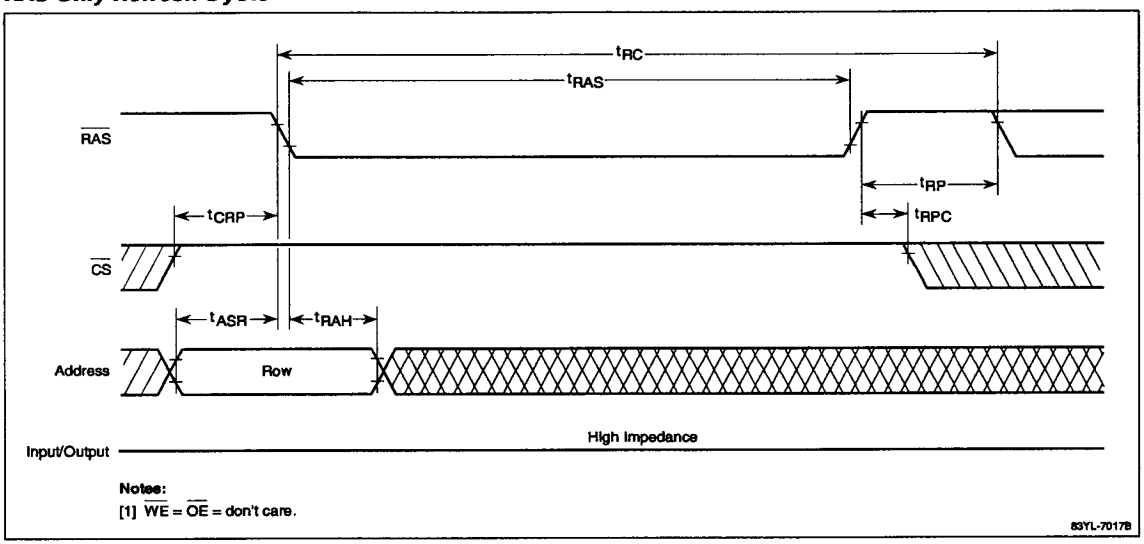
Timing Waveforms (cont)

Hidden Refresh Cycle

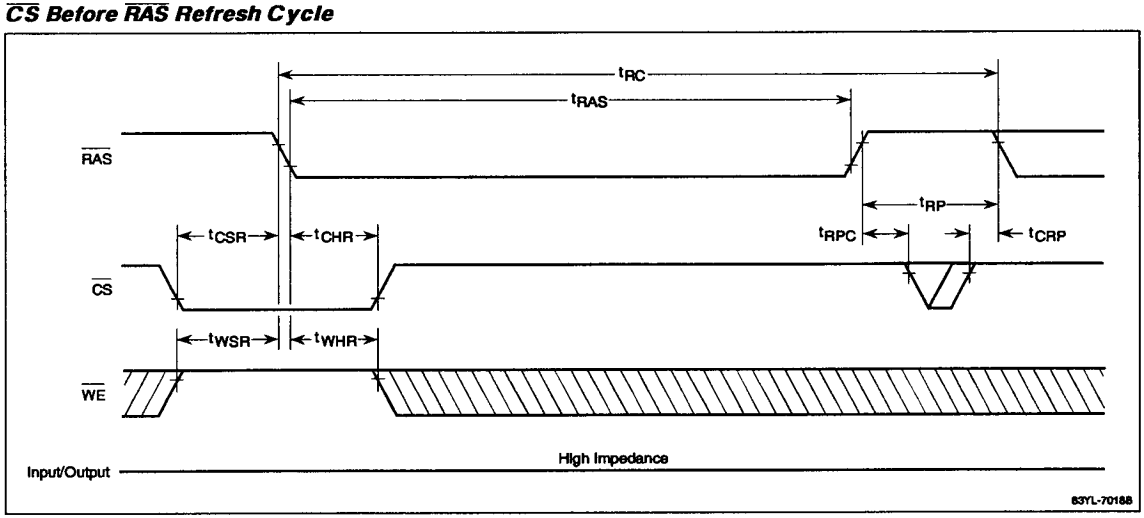


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



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