NEC Electronics Inc.

T-46-23-17

μPD424400
1,048,576 x 4-Bit Dynamic CMOS RAM

February 1991

Description

The μPD424400 is a fast-page dynamic RAM organized as 1,048,576 words by 4 bits and designed to operate from a single + 5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

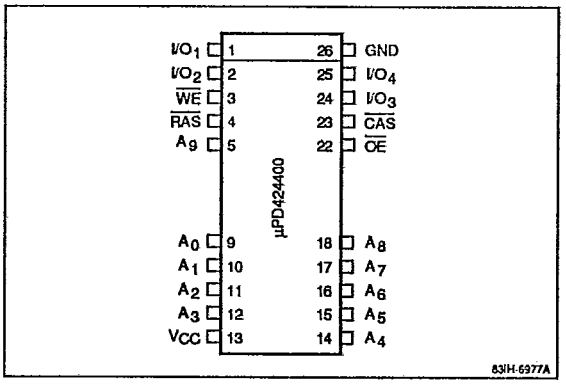
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

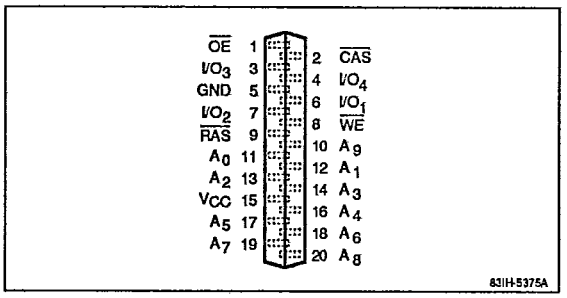
- 1,048,576 by 4-bit organization
- Single + 5-volt power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ (300 and 350 mil), 20-pin plastic ZIP, and 26/20-pin plastic TSOP packaging

Pin Configurations

26/20-Pin Plastic SOJ

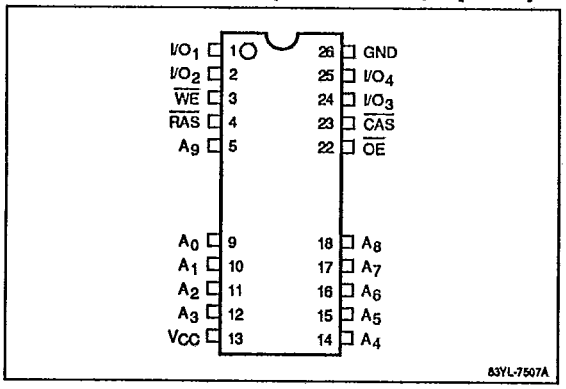


20-Pin Plastic ZIP

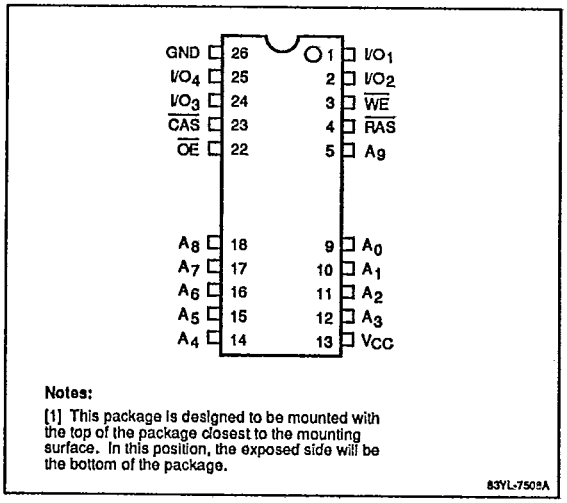


Pin Configurations

26/20-Pin Plastic TSOP (normal leads, top view)



26/20-Pin Plastic TSOP (reverse leads, bottom view)



Notes:

[1] This package is designed to be mounted with the top of the package closest to the mounting surface. In this position, the exposed side will be the bottom of the package.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

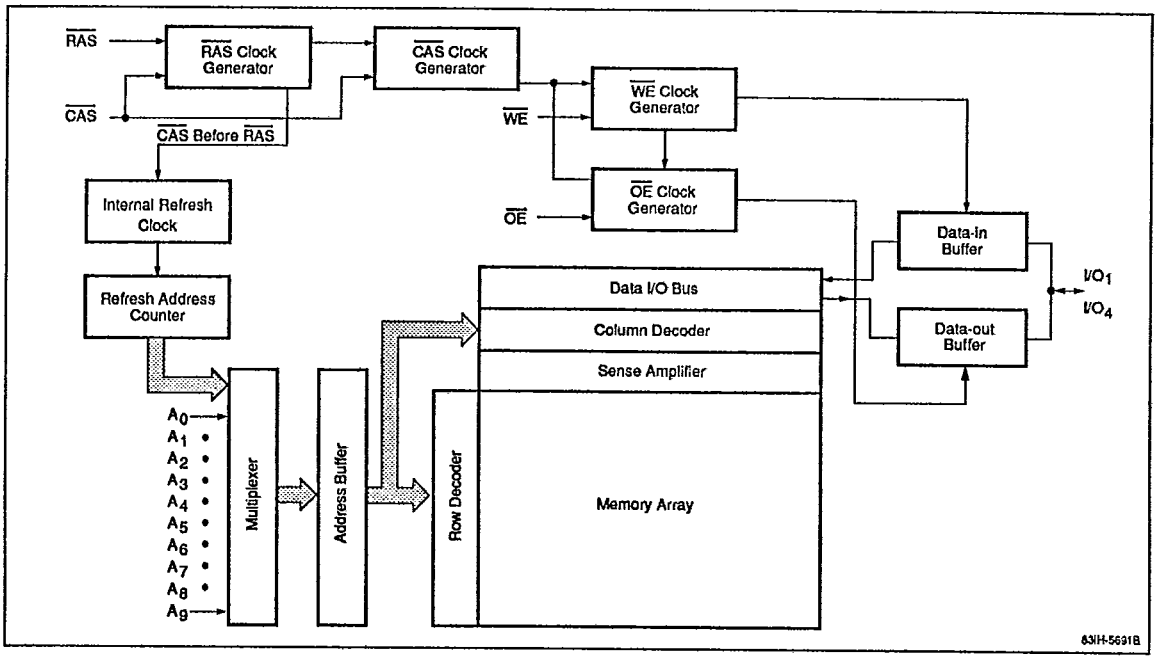
Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD424400LA-60	60 ns	120 ns	40 ns	Standard	26/20-pin plastic SOJ (300 mil)
LA-70	70 ns	140 ns	45 ns		
LA-80	80 ns	160 ns	50 ns		
LA-10	100 ns	190 ns	60 ns		
μPD424400LA-60L	60 ns	120 ns	40 ns	Low power	
LA-70L	70 ns	140 ns	45 ns		
LA-80L	80 ns	160 ns	50 ns		
LA-10L	100 ns	190 ns	60 ns		
μPD424400LB-70	70 ns	140 ns	45 ns	Standard	26/20-pin plastic SOJ (350 mil)
LB-80	80 ns	160 ns	50 ns		
LB-10	100 ns	190 ns	60 ns		
μPD424400LB-70L	70 ns	140 ns	45 ns	Low Power	
LB-80L	80 ns	160 ns	50 ns		
LB-10L	100 ns	190 ns	60 ns		
μPD424400V-60	60 ns	120 ns	40 ns	Standard	20-pin plastic ZIP
V-70	70 ns	140 ns	45 ns		
V-80	80 ns	160 ns	50 ns		
V-10	100 ns	190 ns	60 ns		
μPD424400V-60L	60 ns	120 ns	40 ns	Low power	
V-70L	70 ns	140 ns	45 ns		
V-80L	80 ns	160 ns	50 ns		
V-10L	100 ns	190 ns	60 ns		
μPD424400GS-60-9JD	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (normal leads)
GS-70-9JD	70 ns	140 ns	45 ns		
GS-80-9JD	80 ns	160 ns	50 ns		
μPD424400GS-60L-9JD	60 ns	120 ns	40 ns	Low power	
GS-70L-9JD	70 ns	140 ns	45 ns		
GS-80L-9JD	80 ns	160 ns	50 ns		
μPD424400GS-60-9KD	60 ns	120 ns	40 ns	Standard	26/20-pin plastic TSOP (reverse leads)
GS-70-9KD	70 ns	140 ns	45 ns		
GS-80-9KD	80 ns	160 ns	50 ns		
μPD424400GS-60L-9KD	60 ns	120 ns	40 ns	Low power	
GS-70L-9KD	70 ns	140 ns	45 ns		
GS-80L-9KD	80 ns	160 ns	50 ns		

Low Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V or ≤ 0.2 V, as appropriate; I/O open; all other inputs ≥ $V_{CC} - 0.2$ V or ≤ 0.2 V	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; D_{IN}, $\overline{WE}$, $\overline{OE}$, Addresses ≥ $V_{CC} - 0.2$ V or ≤ 0.2 V; I/O open
	300	μA	≤ 200 ns		

Block Diagram



AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		100		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		90		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		120		100		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 3, 4, 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		15		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 14)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	85		90		100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	70	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		55		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

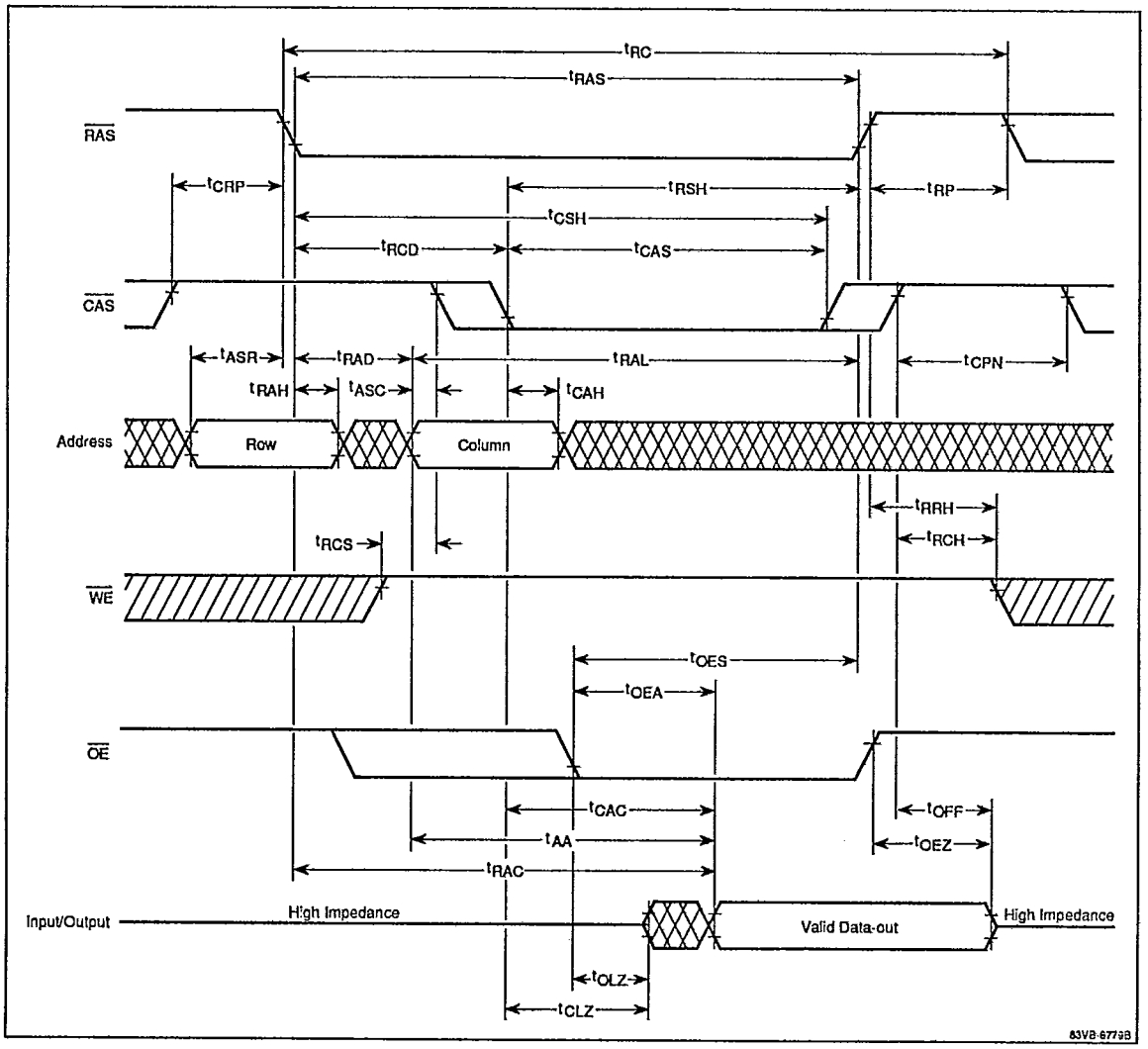
(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

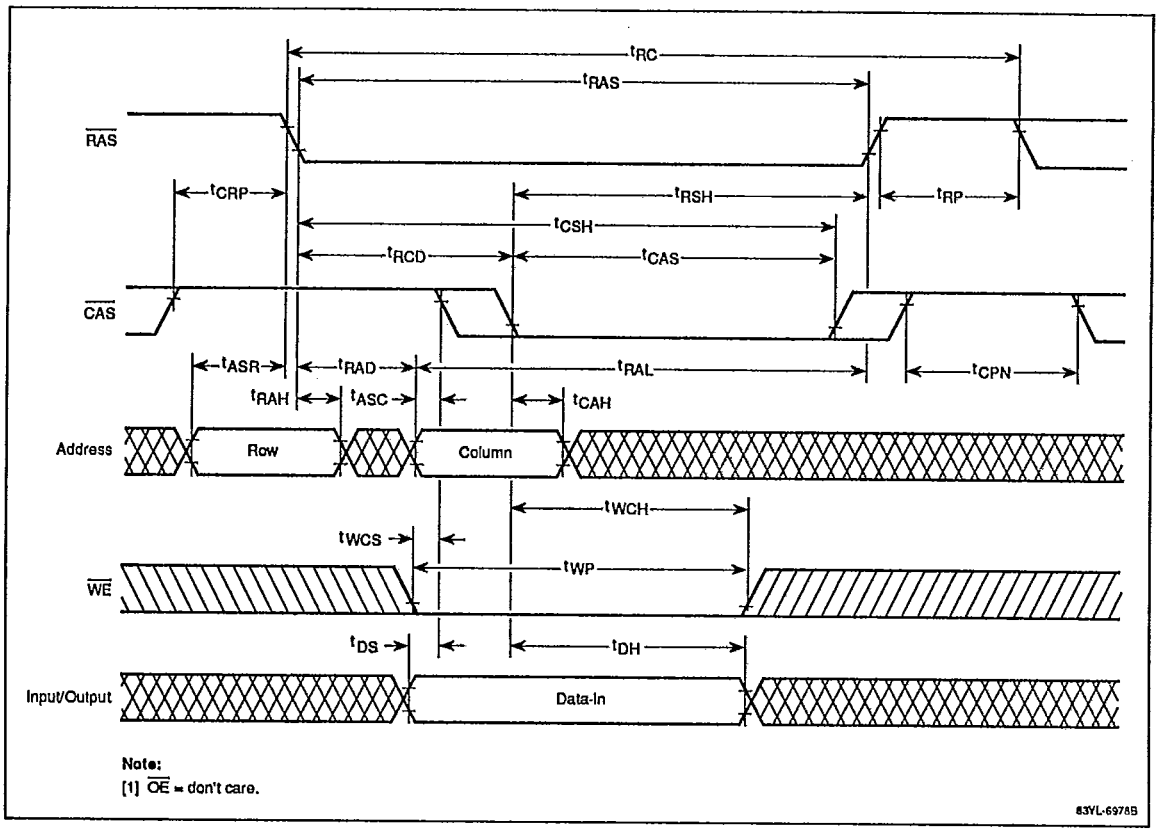
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle

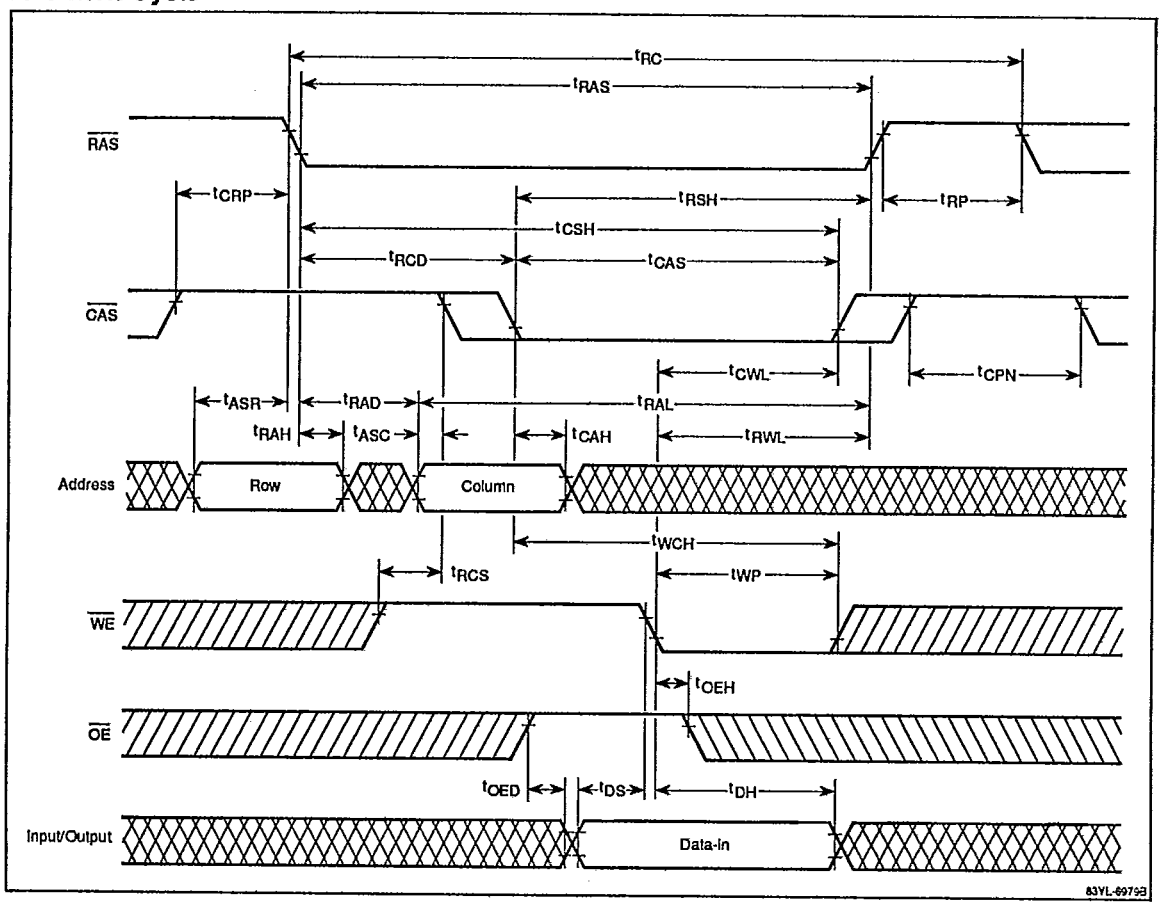


Note:
[1] $\overline{OE}$ = don't care.

83YL-69788

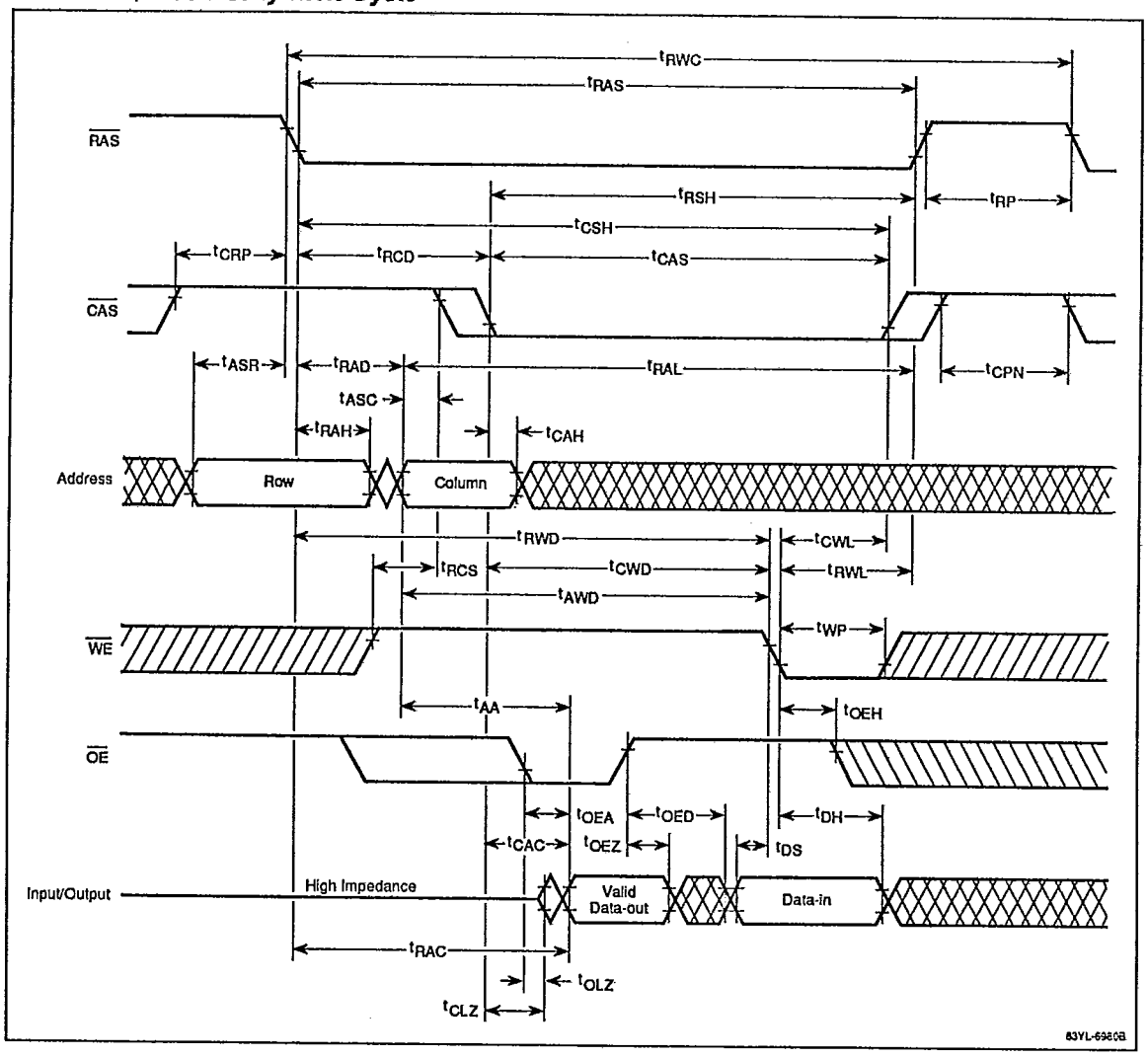
Timing Waveforms (cont)

Late Write Cycle



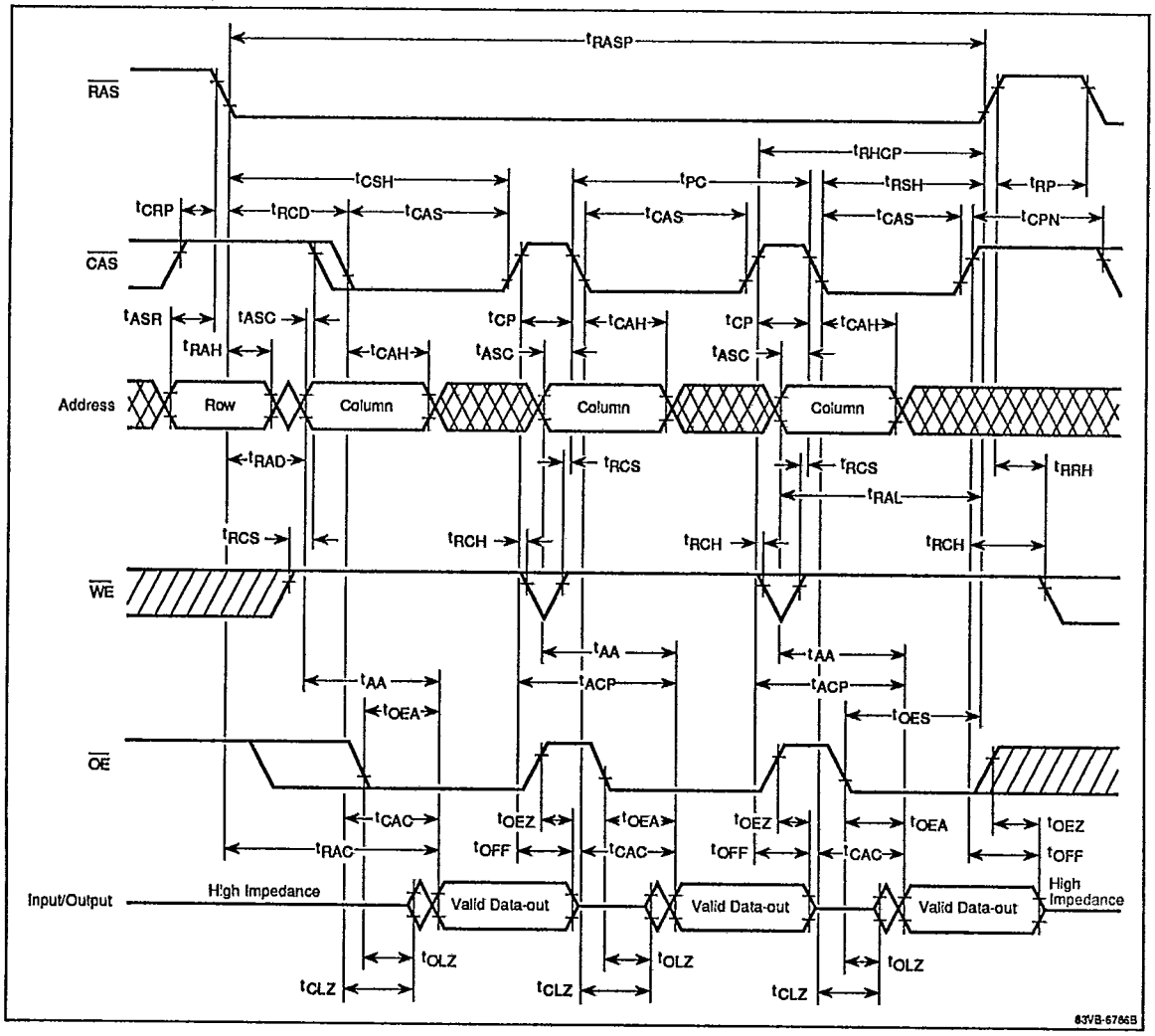
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



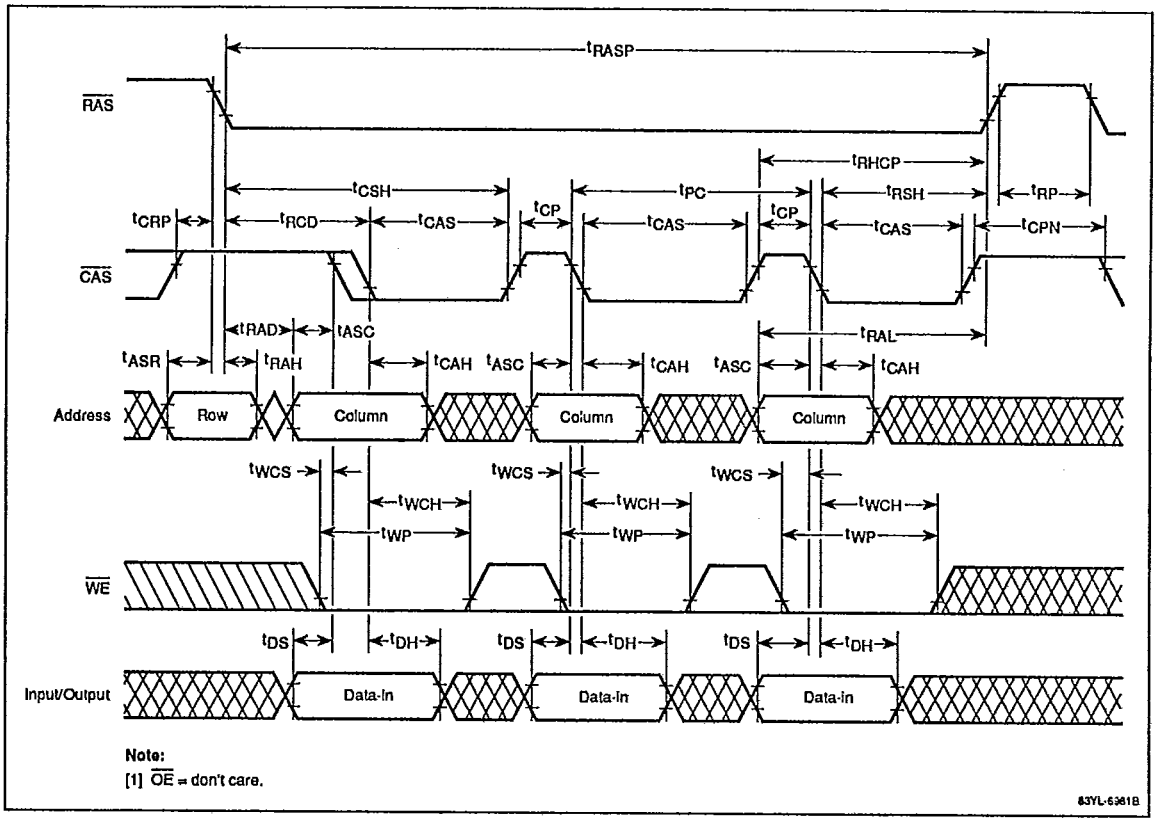
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle

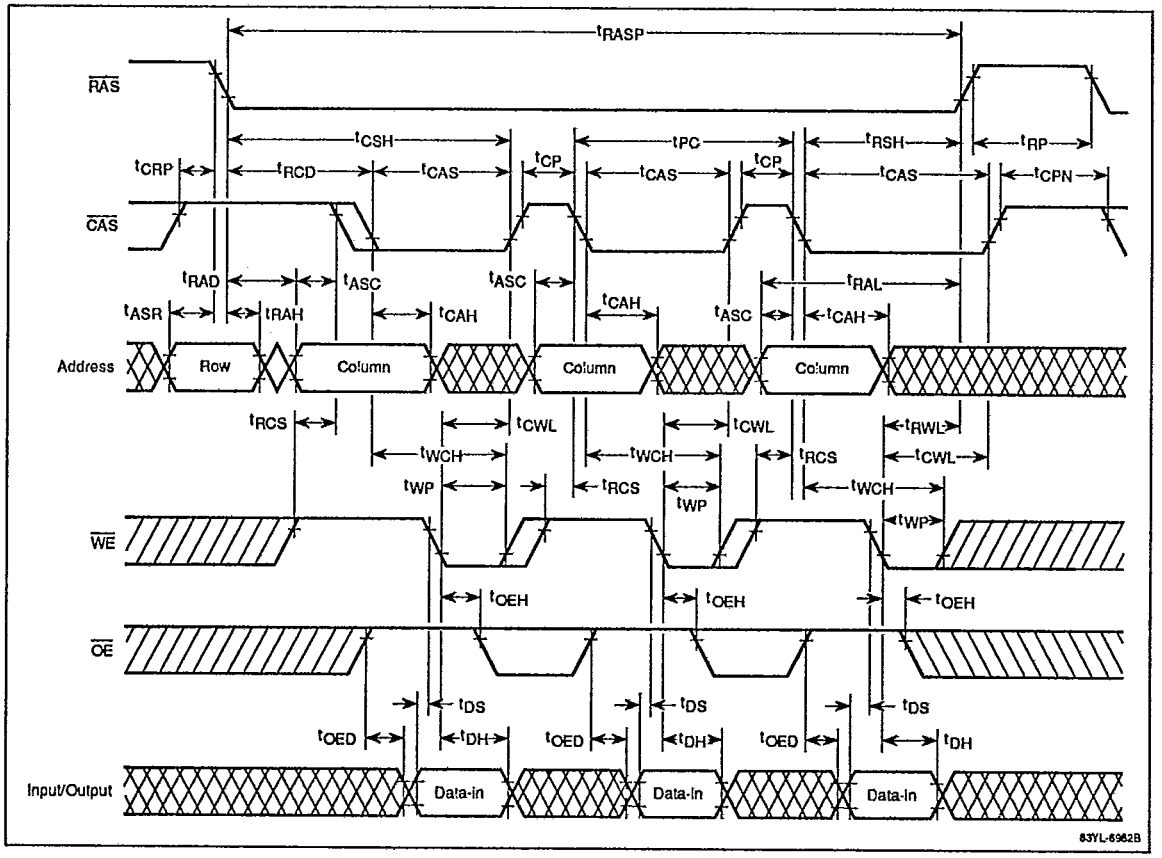


Note:
[1] $\overline{OE}$ = don't care.

83YL-6361B

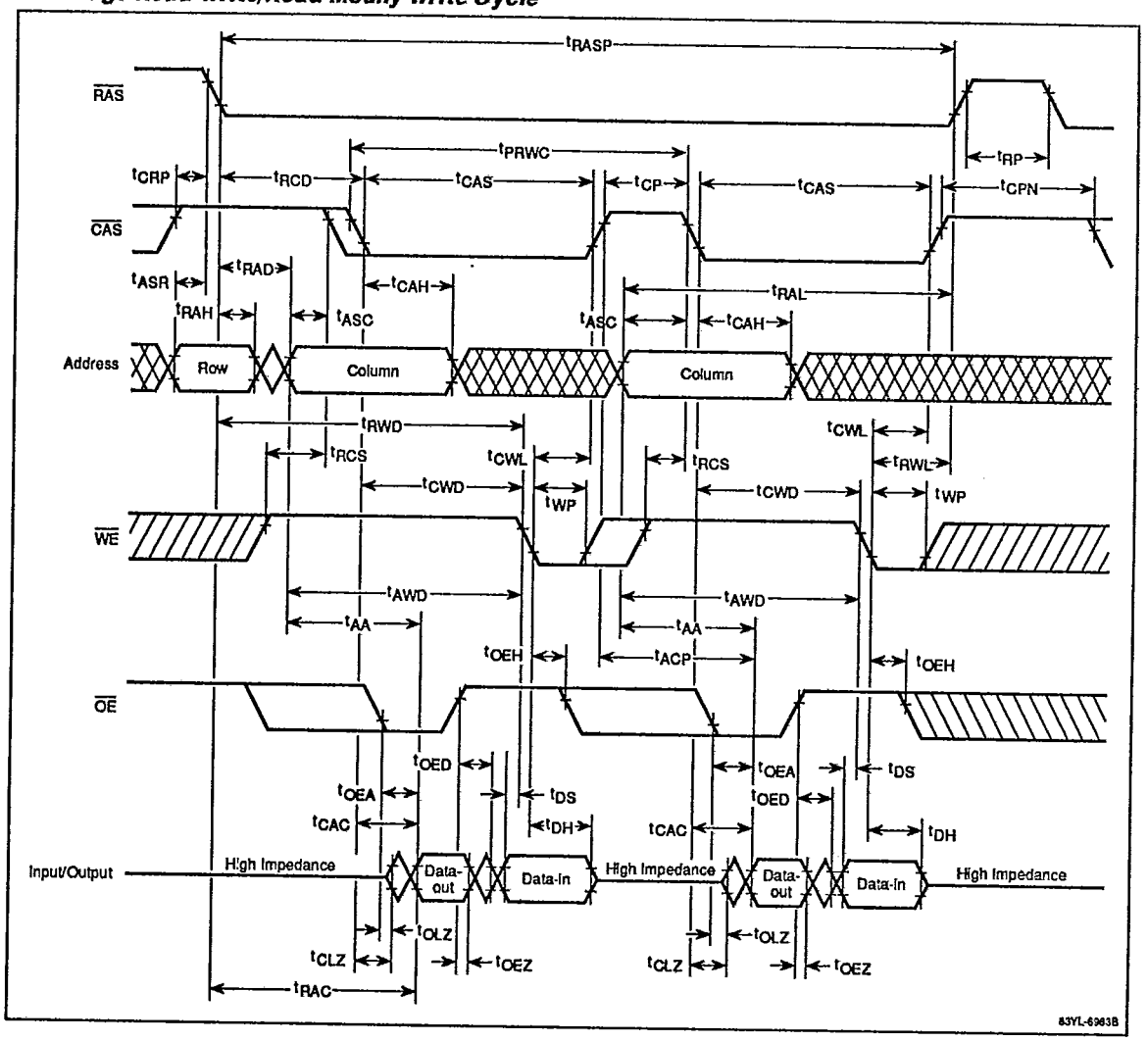
Timing Waveforms (cont)

Fast-Page Late Write Cycle



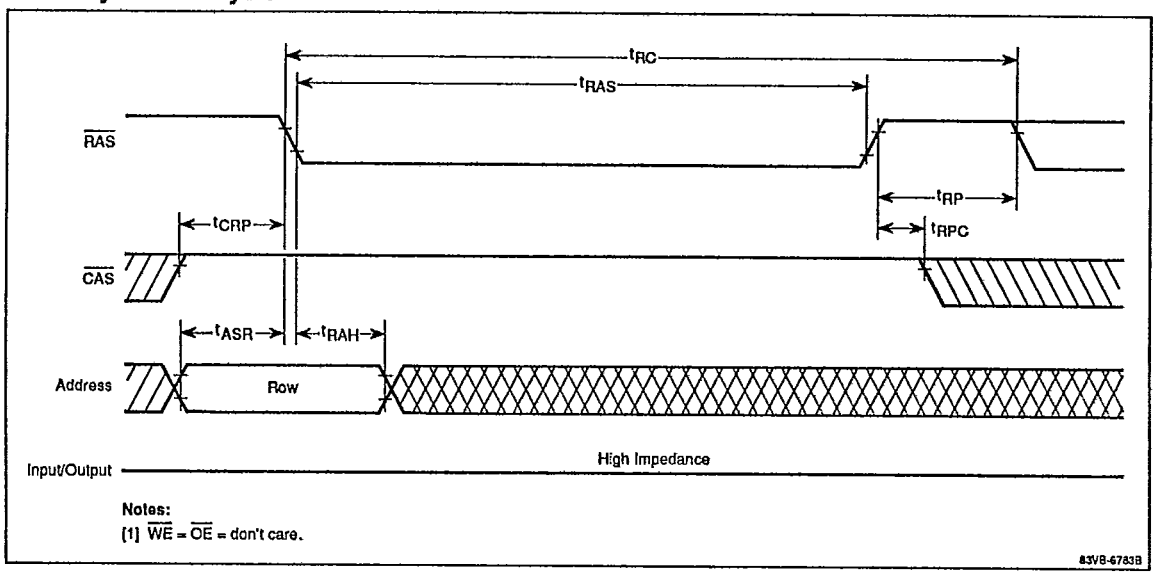
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle

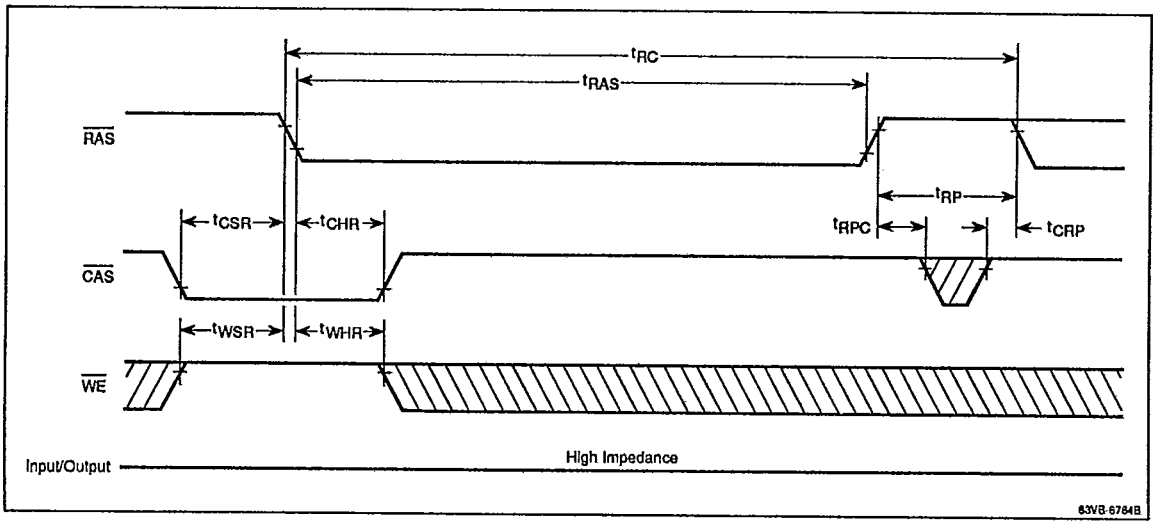


Timing Waveforms (cont)

RAS-Only Refresh Cycle

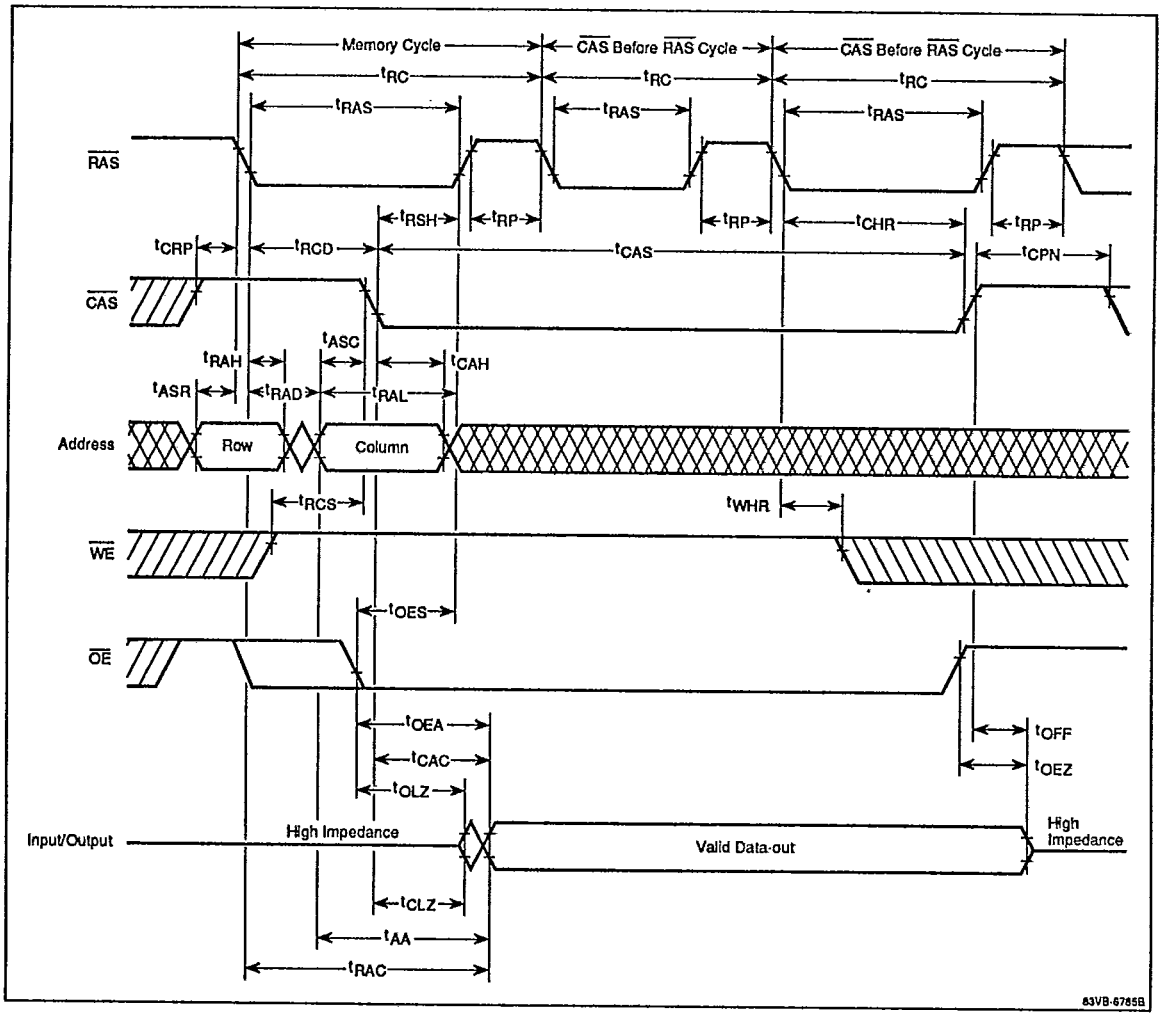


CAS Before RAS Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



NEC

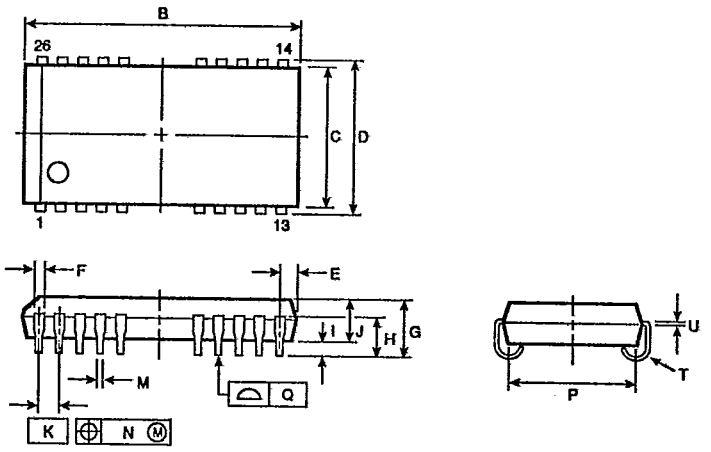
Package Drawings

26/20-Pin Plastic SOJ (350 mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ±0.2	.385 ±.008
E	1.08 ±0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ±0.2	.142 $^{+.008}_{-.007}$
H	2.45 ±0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	8.06 ±0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

P26LB-350A



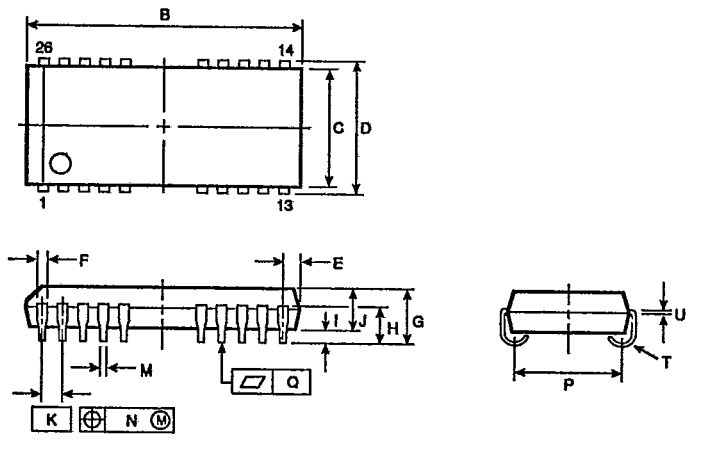
49NR-673B (2/90)

26/20-Pin Plastic SOJ (300 mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ±0.2	.333 $^{+.009}_{-.008}$
E	1.08 ±0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ±0.2	.138 ±.008
H	2.4 ±0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	6.73 ±0.20	.265 ±.008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

P26LA-50A

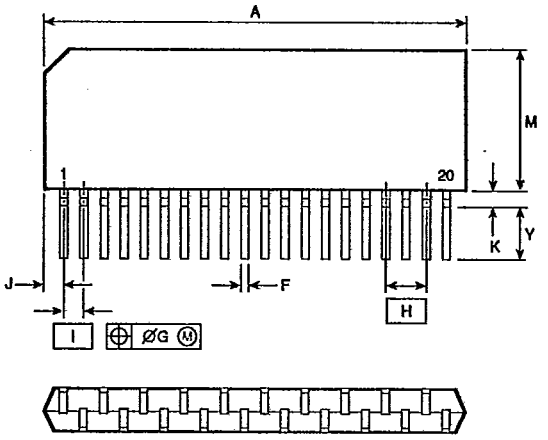


49NR-651B (12/89)

Package Drawings (cont)

20-Pin Plastic ZIP

Item	Millimeters	Inches
A	26.67 max	1.050 max
F	0.5 ±0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ±0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ±0.5	.130 ±.020

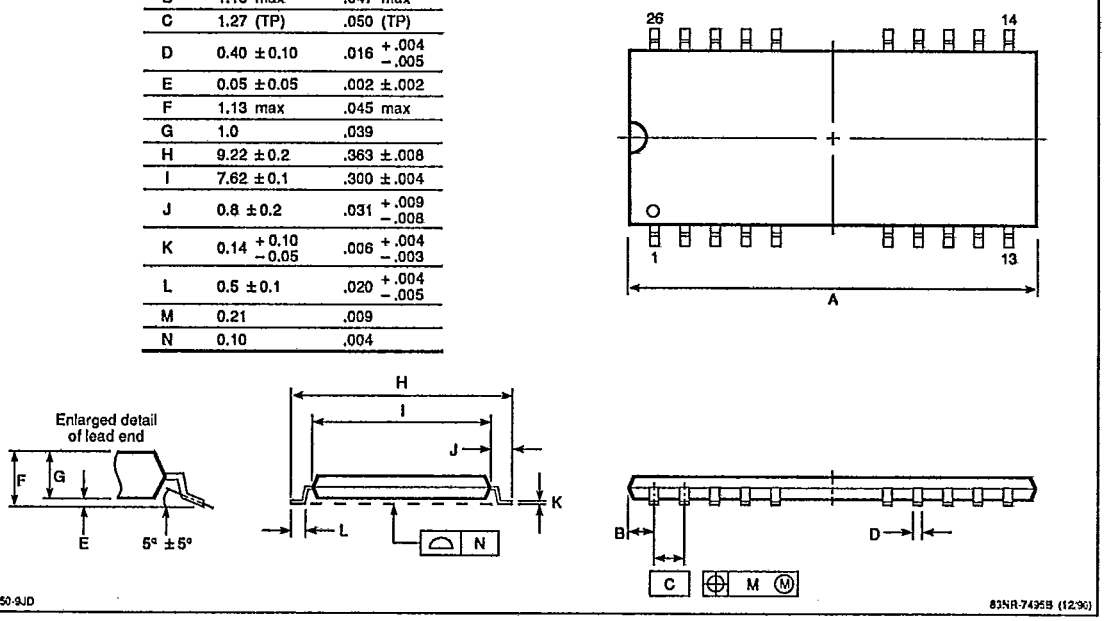


P20V-254-400A-1

43NR-626B (11/89)

26/20-Pin Plastic TSOP (Normal Leads)

Item	Millimeters	Inches
A	17.54 max	.691 max
B	1.18 max	.047 max
C	1.27 (TP)	.050 (TP)
D	0.40 ±0.10	.016 $^{+.004}_{-.005}$
E	0.05 ±0.05	.002 ±.002
F	1.13 max	.045 max
G	1.0	.039
H	9.22 ±0.2	.363 ±.008
I	7.62 ±0.1	.300 ±.004
J	0.8 ±0.2	.031 $^{+.009}_{-.008}$
K	0.14 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
L	0.5 ±0.1	.020 $^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004



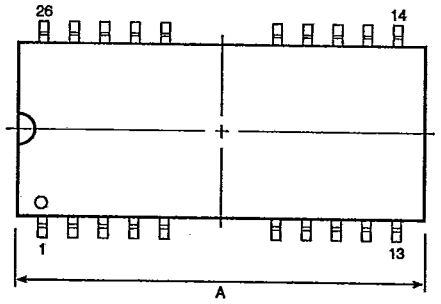
S26GS-50-9JD

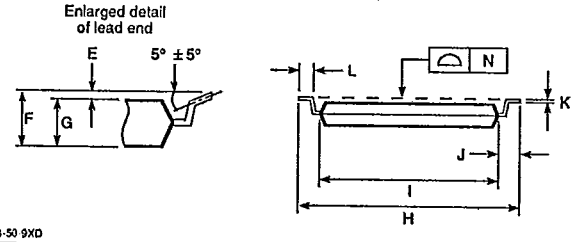
63NR-7435B (12/90)

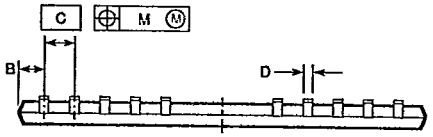
Package Drawings (cont)

26/20-Pin Plastic TSOP (Reverse Bent Leads)

Item	Millimeters	Inches
A	17.54 max	.691 max
B	1.18 max	.047 max
C	1.27 (TP)	.050 (TP)
D	0.40 ±0.10	.016 $^{+.004}_{-.005}$
E	0.05 ±0.05	.002 ±.002
F	1.13 max	.045 max
G	1.0	.039
H	9.22 ±0.2	.363 ±.008
I	7.62 ±0.1	.300 ±.004
J	0.8 ±0.2	.031 $^{+.009}_{-.008}$
K	0.14 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
L	0.5 ±0.1	.020 $^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004







S26GS-50 9XD

83NR-7496B (12/90)