Board Layout Considerations for Am79865 and Am79866

Application Note

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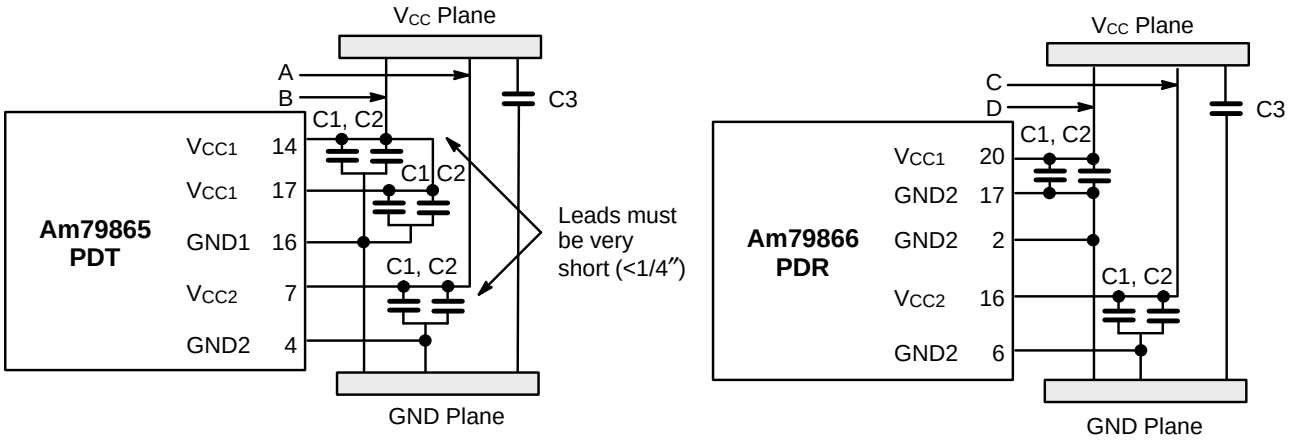
The Physical Data Transmitter (PDT) and Physical Data Receiver (PDR) contain high frequency analog Phase Lock Loops (PLLs). Reliable operation in a high frequency analog and digital environment requires that some simple board layout rules be followed.

For example, most high speed applications which are laid out on a wire wrap board will not work reliably. Because they have at most one power and ground plane, most wire wrap cards have insufficient separation between small signal current and digital switching current. Digital switching noise can couple into the analog PLL, causing phase errors and loss of synchronization. The preferred realization of a high speed application is on a printed circuit board, where the user can control the layout of power and ground planes.

Another source of information on board layout techniques is AMD publication #16356A, "High-Speed-Board Design Techniques".

GENERAL BOARD LAYOUT GUIDELINES

1. Use a PC board with separate GND and V_{CC} planes. Ensure that the connection between each supply pin and the corresponding power/ground plane is as short as possible (not more than 1/4 inch).
2. Use two capacitors which differ by at least a factor of ten in value to decouple the PDT/PDR chips. The reactance of large capacitors has a significant inductive component at high frequencies. Because of this inductive component, a single large capacitor is not very effective against high frequency noise. Two capacitors, one typically of 1µF and one of 0.1 µF are more efficient at decoupling than a single large capacitor of 1.1 µF. The recommended layout is as shown in Figure 1.
3. Keep all bypass capacitors as close to the power pins of the device as possible. Lead lengths should be minimized.
4. Use high quality RF grade capacitors, such as type COG or X7R. The use of type Z5U capacitors is not recommended.



C1 = 0.1 µF (ceramic)
C2 = 0.047 µF (ceramic)
C3 = 1 µF (tantalum)

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To further decouple the power supplies, ferrite beads may be used at locations A, B, C, and D.

Figure 1. PDT/R Decoupling Layouts

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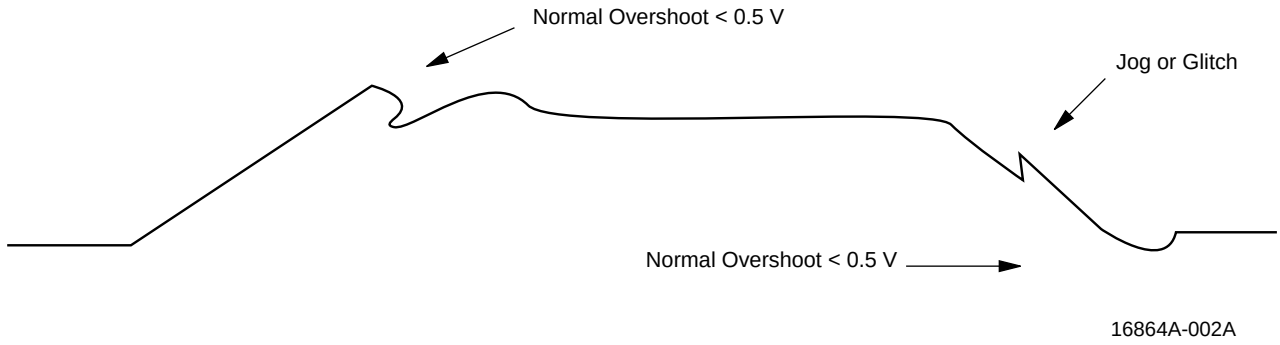

Figure 2. Jogs and Glitches in the LSCLK Line

5. Ensure that the power supply does not have more than 100 mV of peak-to-peak noise at any of the PDT/R V_{CC} pins. Make this check while sending random data.
6. Care should be taken to ensure that jogs or glitches will be kept to a minimum in the LSCLK signal as shown in Figure 2. If present, these glitches will be passed onto the PLL and can cause an occasional error.
7. Run serial differential outputs parallel to each other, or one on top of the other at all times and route them away from the PDT. Do the same for serial inputs on the PDR. Running the serial traces adjacently will minimize noise coupling to other traces caused by the extremely fast signals present on the serial traces. Use impedance controlled strip lines for serial traces that are less than 1 inch in length. Semi-rigid micro coax should be used for longer lengths.
8. When terminating serial lines to or from the PDT/R, ensure that the V_{CC} rail or ground tap is not at a noisy location. Resistors can couple noise from a power supply rail into the serial lines. Decoupling capacitors should be used adjacent to the termination resistors (R1, R2) when using a pull-up/pull-down termination scheme as shown in Figure 3. When using only a pull-down (RE) on the output of the PDT, do not use decoupling as this could add V_{CC} noise into the serial signals.
9. Care should be taken to minimize the undershoot present on the RSCLK output of the PDR (keep undershoot less than 0.5 V). Terminations should be placed on the traces driven by the RSCLK to minimize any reflections generated by the very fast edges of the output driver, The RSCLK output should only be used to drive 1–2 inputs. If additional inputs need to be driven, then use a buffer or clock driver connected between RSCLK and the additional loads.

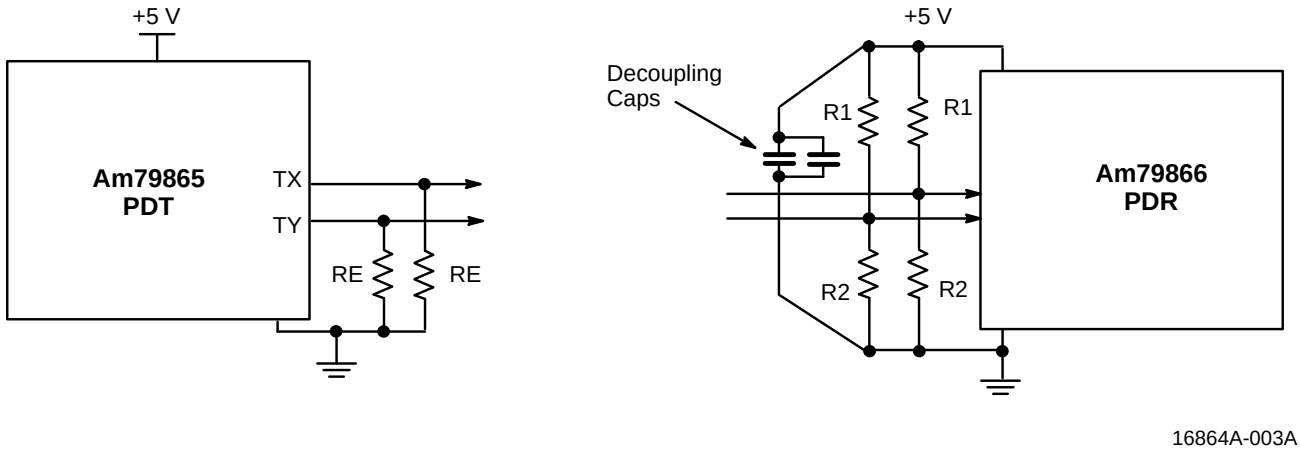

Figure 3. Decoupling Terminations

Board Layout Guidelines When Using Fiber Optic Data Links

Because of their small signals levels, fiber optic data links require some care in layout. Fiber optic data link receivers consist of a photo sensitive diode and a high gain amplifier. The photo-diode converts light pulses into currents on the order of a few hundred nano-amps. This signal current is then amplified and translated into an ECL signal.

If switching noise from the digital section of the board gets coupled into the optical data link, the signal from the light pulse data can be corrupted. To prevent the coupling of power supply noise, the user must ensure that small signal and digital switching currents do not flow in the same path. The optical V_{CC} and ground planes should be separated from the V_{CC} and ground planes used by other digital circuitry.

Figure 4 shows the recommended layout for power and ground planes when using optical data links. Note that this connection includes a ferrite bead in the Vcc circuit of the fiber optic components. The part number shown for the ferrite bead is representative of a typical part. The user should adjust the value to match the particular noise filtering requirements present in their system.

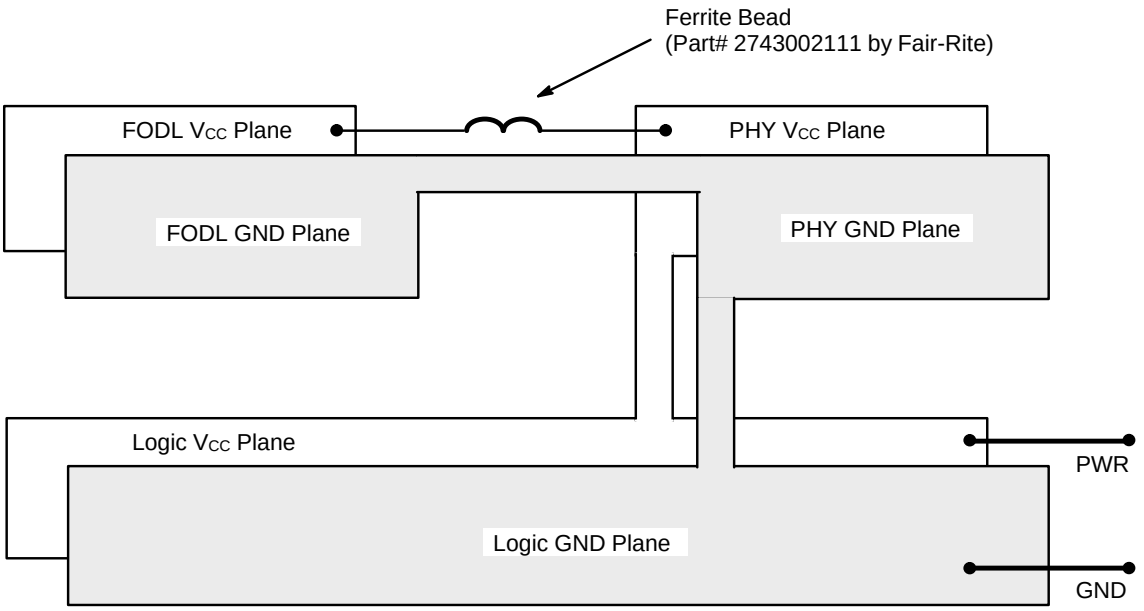

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Figure 4. Fiber Optic Data Link Decoupling