PAL devices 20L8, 20R8, 20R6, 20R4

PLQ20R8-5 SERIES

FEATURES

- Ultra high-speed
  - t_{PD} = 5ns and f_{MAX} = 118MHz
- 100% functionally and pin-for-pin compatible with industry standard 24-pin PAL ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 24 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs
- Register preload for testability
- Power-up 3-State
- 24-Pin DIP and 28-Pin PLCC

DESCRIPTION

The Signetics PLQ20XX family consists of ultra high-speed 5ns versions of Series 24 PAL devices.

The PLQ20XX family is 100% functional and pin-compatible with the 20L8, 20R8, 20R6, and 20R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLQ20R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art BiCMOS process, known as QUBiC, has been employed to achieve higher levels of operating performance for the PLQ20XX family of PLDs. The QUBiC transistors have been optimized to provide two-thirds more speed at less than half the power consumed from products using our last generation of bipolar technology. QUBiC reduces on-chip delays and provides high output drive currents while consuming power at very low levels.

The PLQ20XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLQ20XX series as well as other PLD devices from Signetics. The PLQ20XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLQ20L8	14	8 (6 I/O)	0
PLQ20R8	12	0	8
PLQ20R6	12	2 I/O	6
PLQ20R4	12	4 I/O	4

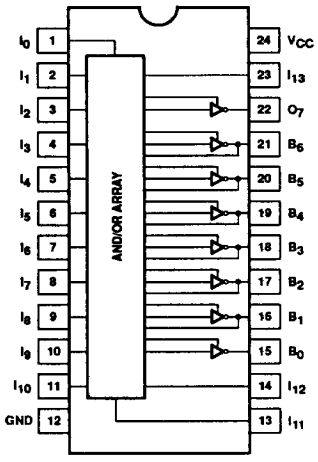
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 300mil-wide	PLQ20R8–5N PLQ20R6–5N PLQ20R4–5N PLQ20L8–5N
28-Pin Plastic Leaded Chip Carrier (PLCC)	PLQ20R8–5A PLQ20R6–5A PLQ20R4–5A PLQ20L8–5A

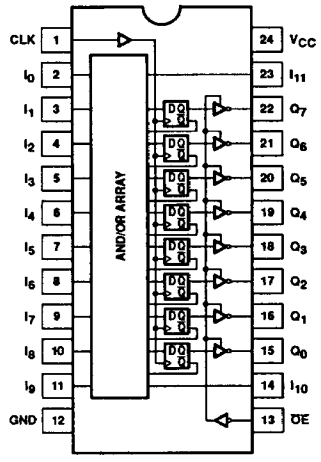
NOTE:
The PLQ20XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

PIN CONFIGURATIONS

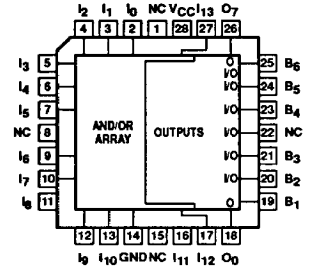
PLQ20L8



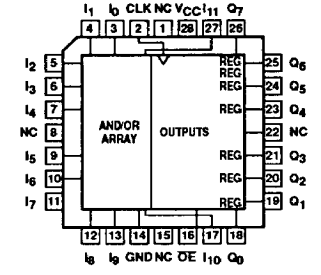
PLQ20R8



PLQ20L8



PLQ20R8

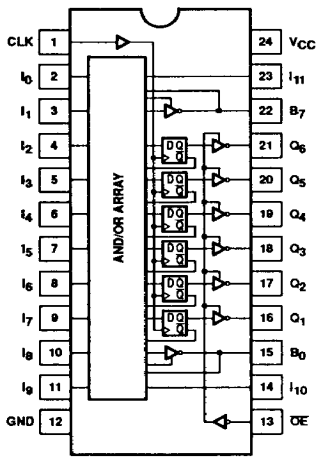


SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

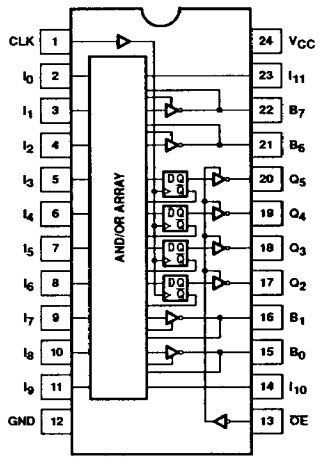
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

PIN CONFIGURATIONS

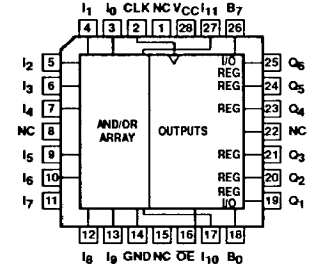
PLQ20R6



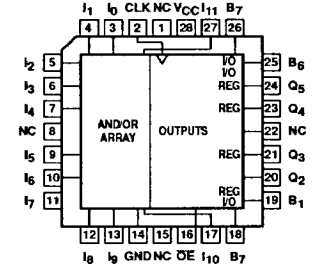
PLQ20R4



PLQ20R6



PLQ20R4



SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinatorial Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

SYMBOL	DESCRIPTION
I	Dedicated Input
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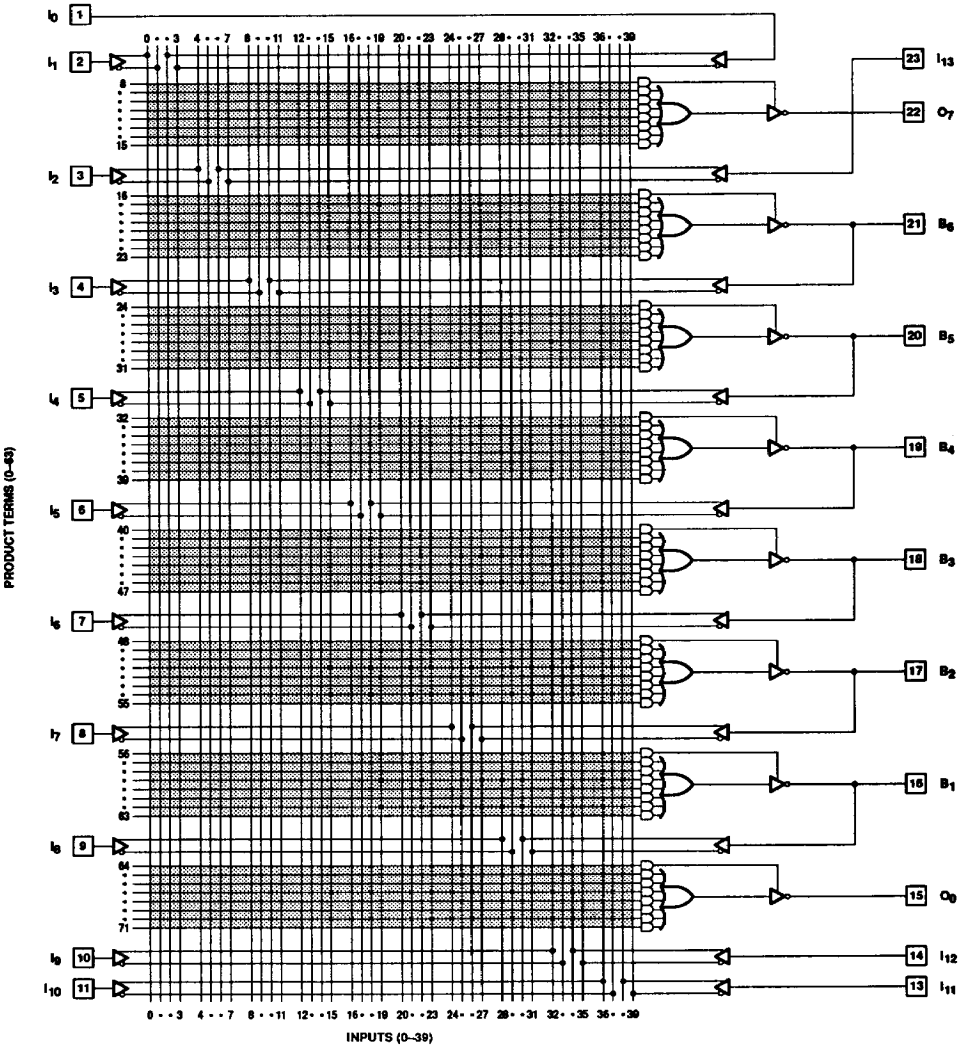
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

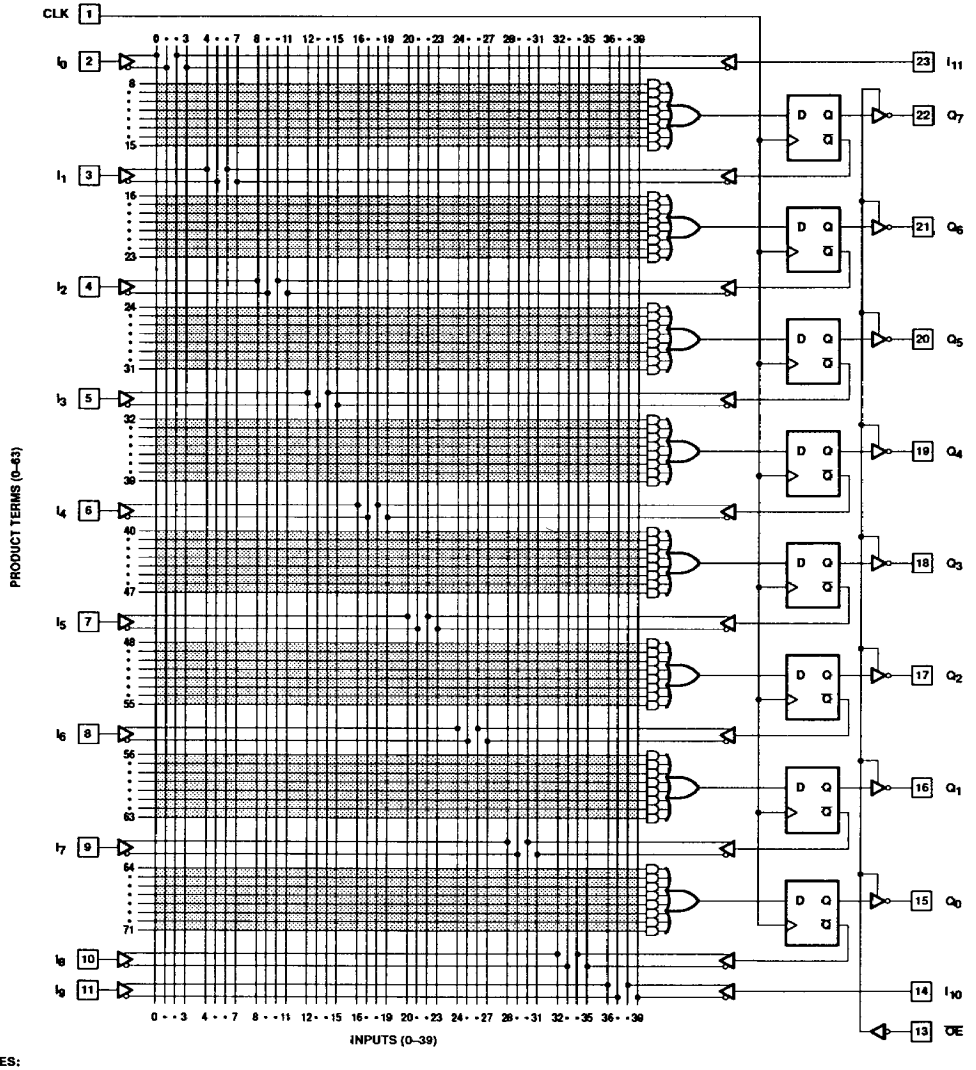
LOGIC DIAGRAM

PLQ20L8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

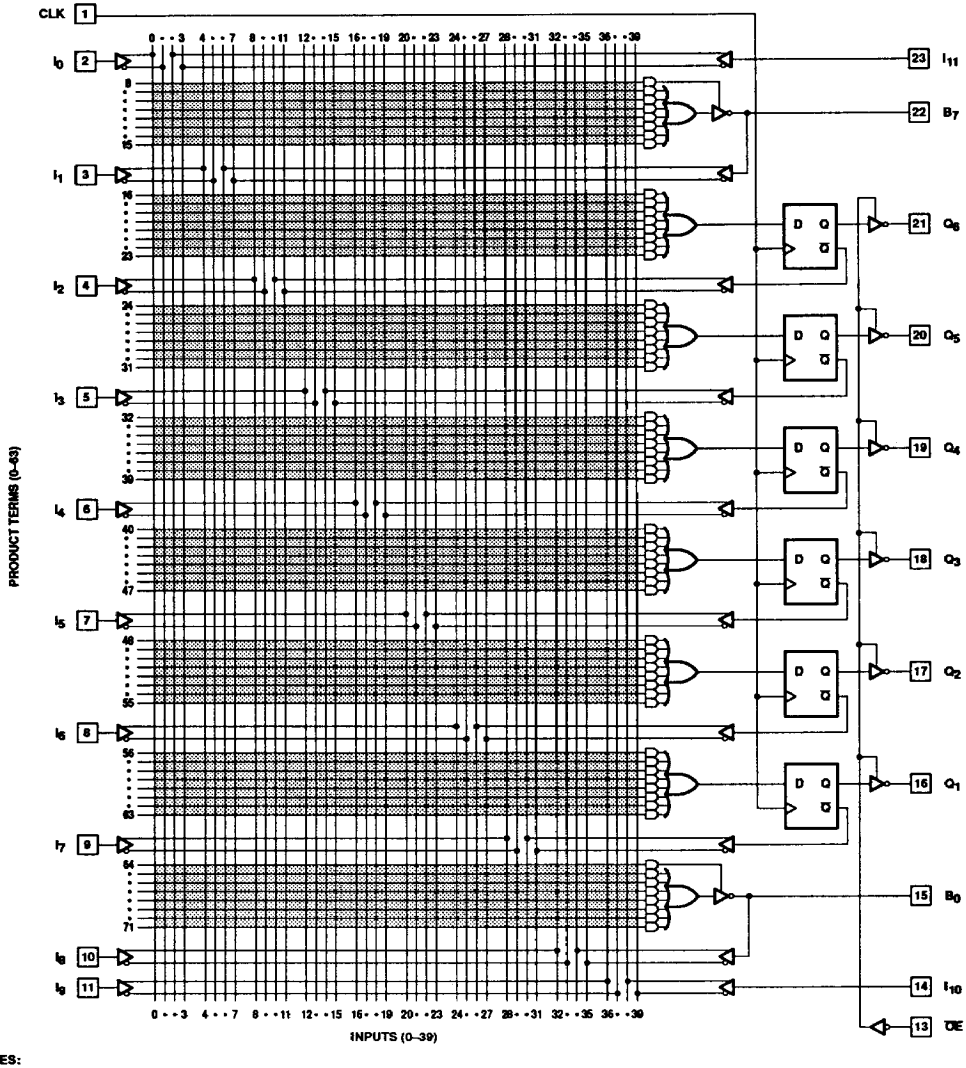
LOGIC DIAGRAM — PLQ20R8



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

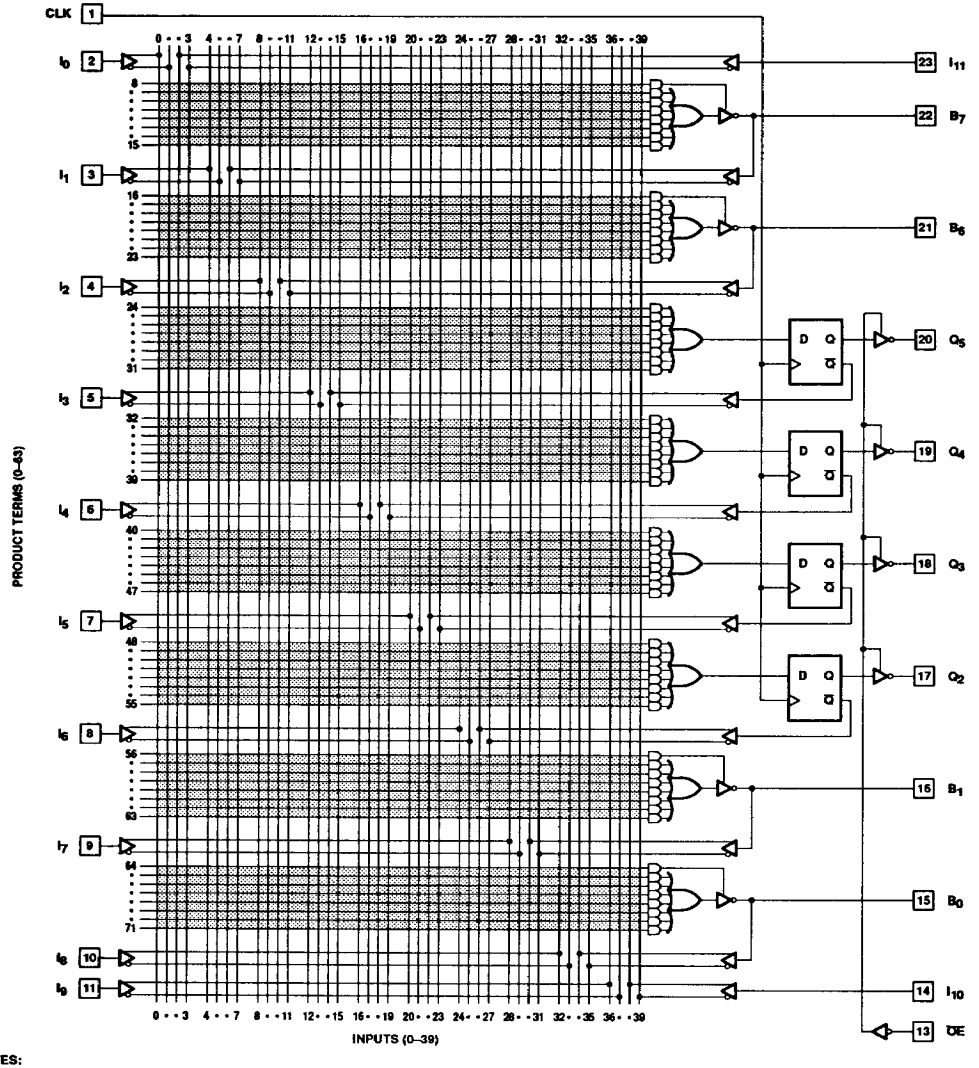
PLQ20R6



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

LOGIC DIAGRAM

PLQ20R4



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0".
2. ▒ Programmable connections.

FUNCTIONAL DESCRIPTIONS

The PLQ20XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLQ20XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLQ20L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLQ20R8, PLQ20R6, PLQ20R4, have respectively 8, 6, and 4 output registers.

3-State Outputs

The PLQ20XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

Programmable Bidirectional Pins

The PLQ20XX products feature variable Input/Output ratios. In addition to 12 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLQ20L8 provides 14 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

Output Registers

The PLQ20R8 has 8 output registers, the 20R6 has 6, and the 20R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLQ20R8, R6, R4 enhance state machine design and initialization capability.

Register Preload

Preload function allows the register to be loaded from the output pins. This feature allows functional testing of sequential patterns by loading output states.

Power-up 3-State

All outputs will be disabled when V_{CC} is 3.0V ± 20% (25°C). This special feature keeps outputs 3-Stated during power-up. Only when V_{CC} reaches its normal operating range will device function normally.

Software Support

Like other Programmable Logic Devices from Signetics, the PLQ20XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLQ20XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

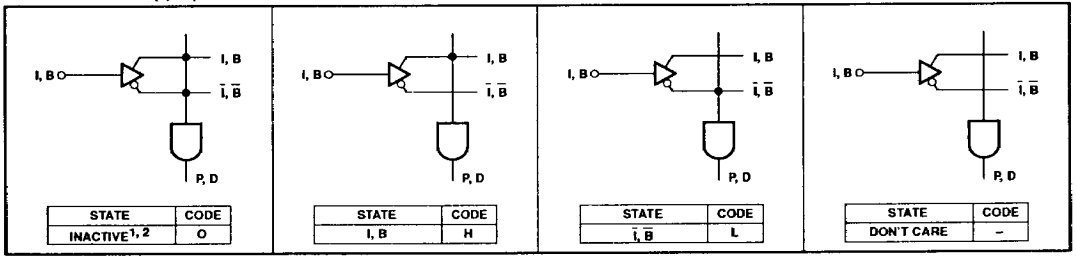
SLICE is available free of charge to qualified users.

Logic Programming

The PLQ20XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLQ20XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

AND ARRAY – (I, B)



STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I, B}$	L

STATE	CODE
DON'T CARE	–

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All P_n terms are disabled.
2. All P_n terms are active on all outputs.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage	–1.2	+7.0	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = −18mA		−0.8	−1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = 24mA			0.5	V
V_{OH}	High	I_{OH} = −3.2 mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low[3]	V_{IN} = 0.40V			−250	µA
I_{IH}	High[3]	V_{IN} = 2.7V			25	µA
I_I	Maximum input current	V_{IN} = 5.5V, V_{CC} = MAX			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage	V_{OUT} = 2.7V			100	µA
I_{OZL}	Output leakage	V_{OUT} = 0.4V			−100	µA
I_{OS}	Short circuit[4, 5]	V_{OUT} = 0.5V	−30		−130	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		150	210	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5V				
		V_{OUT} = 2.0V		8		pF
C_B	I/O (B)	V_{OUT} = 2V, f = 1MHz		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 200\Omega$, $R_2 = 390\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

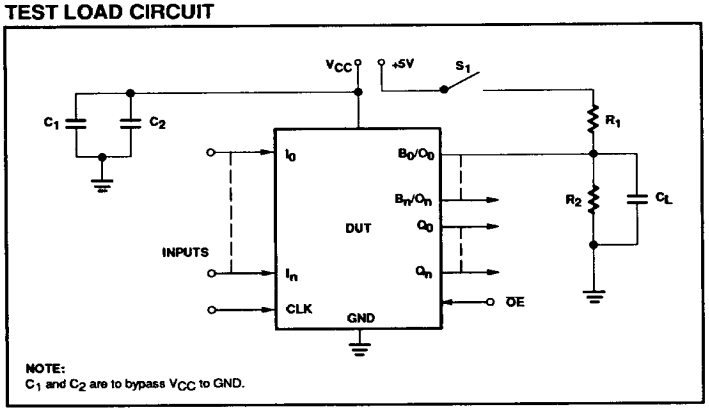
SYMBOL	PARAMETER	FROM	TO	LIMITS MIN[1]	LIMITS MAX	UNIT
Pulse Width						
t_{CKH}	Clock High	CLK+	CLK–	3.0		ns
t_{CKL}	Clock Low	CK–	CLK+	3.0		ns
t_{CKP}	Period	CLK+	CLK+	6.0		ns
Setup & Hold time						
t_{IS}	Input	Input or feedback	CLK+	4.0		ns
t_{IH}	Input	CLK+	Input or feedback	0		ns
Propagation delay						
t_{CKO}	Clock	CLK±	Q±		4.5	ns
t_{CKF}	Clock[3]	CLK±	$\overline{Q}$		2.5	ns
t_{PD}	Output (20L8, R6, R4)[2]	I, B	Output		5.0	ns
t_{OE1}	Output enable[4]	$\overline{OE}$	Output enable		6.0	ns
t_{OE2}	Output enable[4,5]	I	Output enable		8.0	ns
t_{OD1}	Output disable[4]	$\overline{OE}$	Output disable		6.0	ns
t_{OD2}	Output disable[4,5]	I	Output disable		8.0	ns
t_{SKW}	Output	Q	Q		1.0	ns
t_{PPR}	Power-Up Reset	V_{CC}+	Q+		8.0	ns
Frequency (20R8, R6, R4)						
f_{MAX}	No feedback $1/(t_{CKL} + t_{CKH})$[6]				167	MHz
	Internal feedback $1/(t_{IS} + t_{CKF})$[6]				154	MHz
	External feedback $1/(t_{IS} + t_{CKO})$[6]				118	MHz

* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

NOTES:

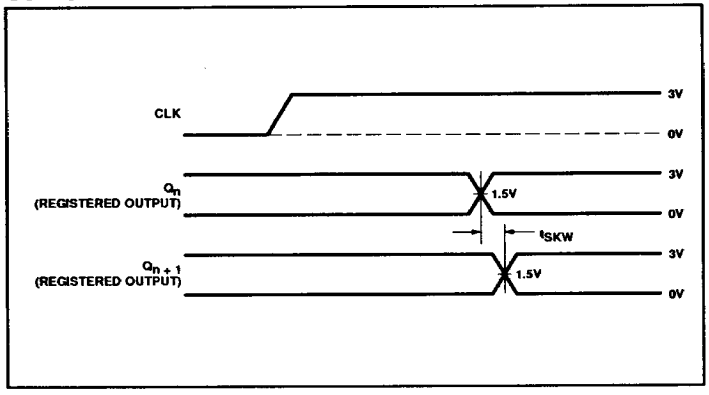
1. C_L = 0pF while measuring minimum output delays.
2. t_{PD} test conditions: C_L = 50pF (with jig and scope capacitance), V_{IH} = 3V, V_{IL} = 0V, $V_{OH} = V_{OL}$ = 1.5V.
3. t_{CKF} was calculated from measured Internal f_{MAX}.
4. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
5. Same function as t_{OE1} and t_{OD1}, with the difference of using product term control.
6. Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

TEST LOAD CIRCUIT

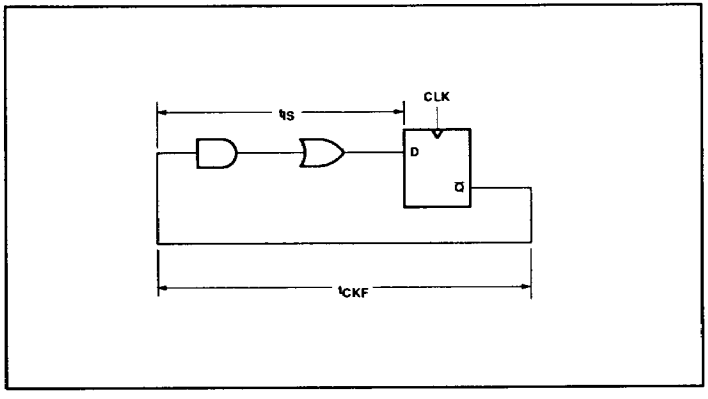


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

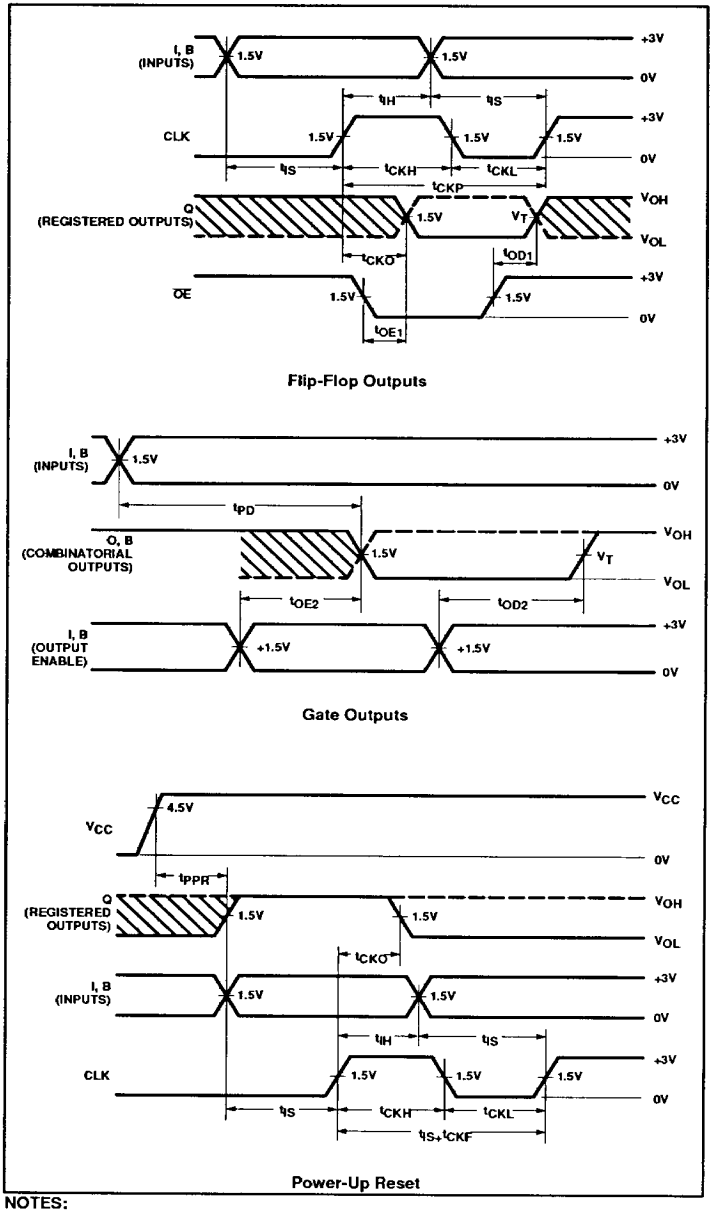
OUTPUT REGISTER SKEW



CLOCK TO FEEDBACK PATH



TIMING DIAGRAMS[1, 2]



TIMING DEFINITIONS

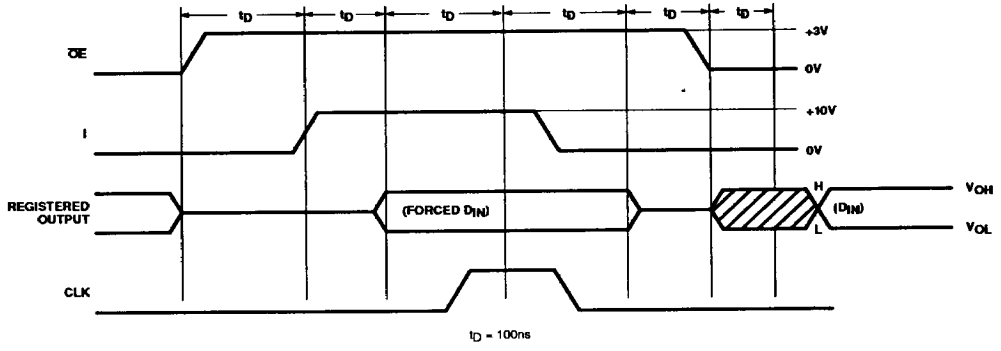
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{IS}	Required delay between beginning of valid input and positive transition of clock.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKF}	Delay between positive transition of clock and when internal $\overline{Q}$ output of flip-flop becomes valid.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_D	Delay between each input change

FREQUENCY DEFINITIONS

f_{MAX}	**No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **Internal feedback:** Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{IS} + t_{CKF})$. **External feedback:** Determined by clock-to-output delay and input setup time, $1/(t_{IS} + t_{CKO})$.

NOTES:
1. Input pulse amplitude is 0V to 3V.
2. Input rise and fall times are 2.0ns typical.

TIMING DIAGRAMS (Continued)

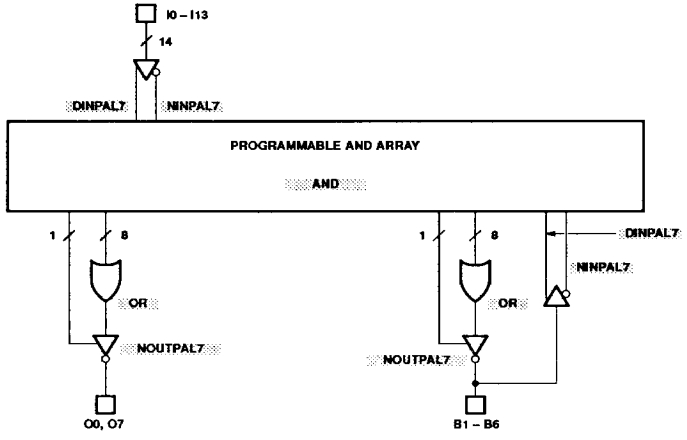


Output Register Preload

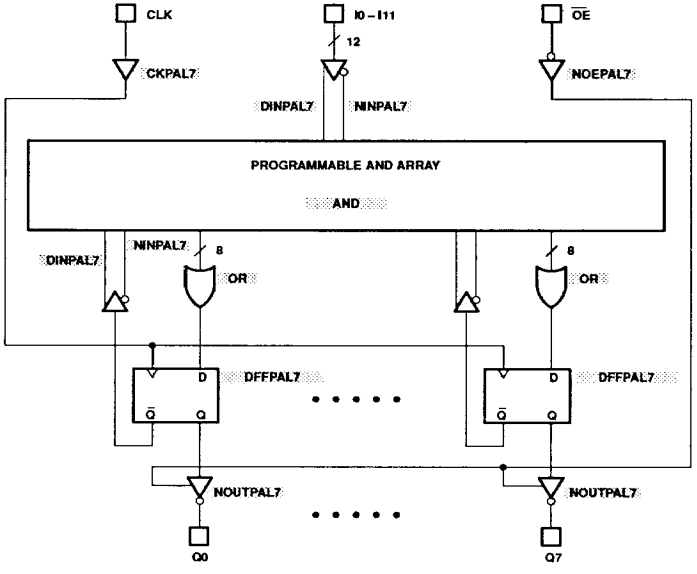
PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 8 *(Development Software)* and Section 9 *(Third-Party Programmer/ Software Support)* for additional information.

SNAP RESOURCE SUMMARY DESIGNATIONS



PLQ20L8



PLQ20R8

SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)