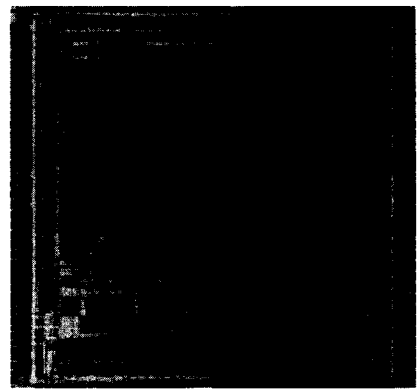
LSI LOGIC

L64032
32 x 32-Bit
Multiplier-Accumulator

Description

The L64032 is a high-speed 32 x 32-bit parallel multiplier-accumulator which provides single precision (32 x 32) and multiple precision (64 x 64) fixed point multiplication and single precision multiplication with accumulation. The device is fabricated with a 1.5-micron drawn gate length (0.9-micron effective channel length) HCMOS process. High speed is obtained through the use of modified Booth encoding, Wallace tree adders and a high-speed carry select adder.

The L64032 is useful in DSP (Digital Signal Processing) applications such as Fourier transforms, digital filtering, power series expansions and correlations. In these applications, the 32-bit word length yields a signal to noise ratio and dynamic range of up to 192 dB. This device is also useful for general computational tasks such as matrix manipulations, graphics processing and arithmetic acceleration.



L64032 Chip

Features

- 32 x 32-bit parallel multiplication and product accumulation
- 64 x 64-bit fixed-point multiplication
- Fast cycle times

Commercial	Military
125 ns	160 ns
100 ns	125 ns
80 ns	100 ns

- Low power consumption–900 mW at 10 MHz
- Supports unsigned integer, two's complement integer, unsigned fractional and two's complement fractional input formats
- Supports unsigned integer, two's complement integer, unsigned fractional, two's complement fractional (shifted) and two's complement fractional (unshifted) output formats
- Positive and negative product accumulation
- TEMP register supports product register preloading
- Full rounding capability
- All registers offer full built-in scan testing capability
- 132-pin CPGA or PPGA (Ceramic or Plastic Pin Grid Array) package

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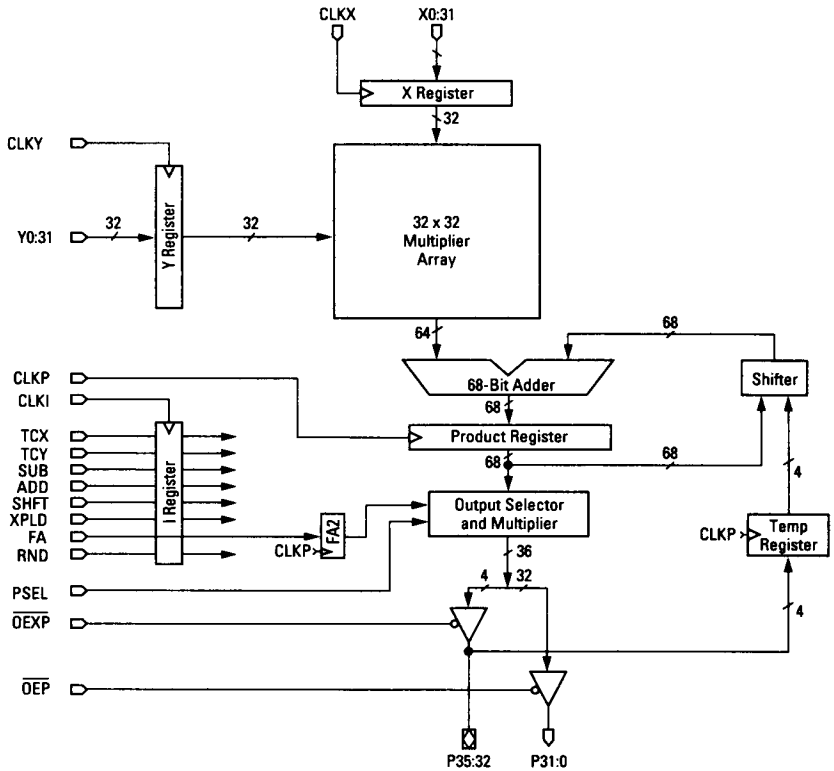
Block Diagram



Architecture

The L64032 is a HCMOS 32 x 32-bit fixed point parallel multiplier with a 68-bit accumulator. This device features a three bus architecture to maximize system performance as well as full on-chip scan test circuitry built into all registers for board and system level test schemes.

The L64032 supports a wide variety of input and output data formats including two's complement, unsigned and mixed mode for both integer and fractional notation. A format adjust control provides a left shifted data output for reading two's complement fractional notation without the use of additional external circuitry.

Both positive and negative accumulation are supported. This selection is controlled by the ADD and SUB inputs, respectively. The SHFT input performs a 32-bit arithmetic shift of the Product Register and positive accumulation for multiple precision operations. Using the ADD and SHFT inputs, a double precision 64-bit multiply can be performed in four pipelined or six non-pipelined cycles.

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Architecture
(Continued)

Input Format Controls
Two independent input format controls (TCX and TCY) are provided. When the format control is LOW, the associated input data is interpreted as unsigned. When the signal is HIGH, the associated input data is interpreted as being two's complement.

If both TCX and TCY are LOW, the resultant output will be in unsigned format. Otherwise the output will be in two's complement format.

Accumulator Operation
The accumulator is controlled by three separate inputs, ADD, SUB and SHFT. All three inputs invoke the accumulation operation. Each of the three inputs acts in a different way.

ADD performs standard positive accumulation where the current product is added to the previous product stored in the 68-bit product register.

SUB performs negative accumulation where the previous product stored in the 68-bit product register is subtracted from the current product.

SHFT works the same as the ADD input except the previous product stored in the 68-bit product register is arithmetically shifted right by 32 bits before it is added to the current product. This input is generally used in multiple precision operations.

Normally, at most one of these inputs is HIGH during any given cycle.

TEMP Register
The TEMP register facilitates preloading of the extended product register (PR64:67 or XTP). The balance of the product register can easily be preloaded through a series of multiplications from the X and Y inputs. The XTP presents a problem since to load this section of the register, using only the X and Y inputs, several overflow operations would have to be invoked. Therefore, the TEMP register is loaded directly through the P32:35 inputs. The output for the TEMP register is the feedback loop to the accumulator so simultaneous loading of the XTP and either the MSP and LSP can occur. The inclusion of TEMP into the feedback loop is controlled by the XPLD input.

Format Adjust
Since most multiplication operations operate during a single machine cycle, it is advantageous to have all the controls for that operation available to the device during the same cycle that input data is applied to the device.

Most operations occur while the input data is being clocked into the input registers. The single exception to this is the format adjust (FA) control which occurs after the result of a multiplication or multiply accumulation operation is being clocked into the product register. Thus LSI Logic has inserted an additional register after the instruction register for the format adjust input only. This register is clocked by CLKP. It should also be noted that this register is the last in the scan chain for the product register.

Format adjust should be HIGH for operations on two's complement fractions whenever a single precision product is desired. By shifting the product register and extended product register left one position before output, FA adds an additional significant bit to the most significant product (MSP). The shifting also serves to place the MSP binary point at the same relative position as in the inputs. FA also adjusts the point where rounding occurs when RND is HIGH.

Rounding
The RND control adds "1" to the most significant bit (MSB) of the least significant product. This addition occurs before the product register. The relative position of this addition is a function of the numerical representation of the output as determined by the format adjust (FA) input. When FA is LOW, a 1 is added to bit PR31. When FA is HIGH, a 1 is added to bit PR30.

Scan Testing
In order to facilitate chip and system level testing, LSI Logic has designed single phase scan into all registers of the L64032.

By placing the TEST input HIGH, all registers within the L64032 are linked into one of two separate serial scan chains. Each of these chains is a large serial shift register with a separate data input and output.

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Architecture (Continued)

The input scan chain links the X Register, Y Register and I Register from the least significant to the most significant bit respectively. Data is shifted into TIX (Test Input X) input, through the X, Y and I Register and out through TOI (Test Output I) output. The shifting within this chain is controlled by CLKX, CLKY and CLKI in each of their associated registers. Care must be taken to clock I at or before Y, and to clock Y at or before X.

The output scan chain links the P Register, TEMP Register and FA2 Register. Data is shifted from TIP (Test Input P) to TOP (Test Output P). This entire chain is controlled by CLKP.

Pin Listing and Description

X0:31, Y0:31
The two 32-bit operand inputs.

P0:35
The 36-bit product output. $\overline{OEP}$ is the 3-state control for P0:31. $\overline{OEXP}$ is the 3-state control for P32:35.

CLKX, CLKY, CLKI and CLKP
Clocks for the X, Y, Instruction and Product Register, respectively. The rising edge is the active edge for all clocks.

Control Inputs
TCX, TCY, (Two's complement X, Y)
When either signal is HIGH the data input associated with the signal is interpreted as a two's complement number. Otherwise, the associated data input is unsigned.

ADD (Positive accumulation)
When ADD is HIGH the data in the P Register is added to the multiplier output for storage in the P Register.

SUB (Negative accumulation)
When SUB is HIGH the data in the P Register is subtracted from the multiplier output for storage in the P Register.

SHFT (Shift and Add)
SHFT causes the data in the P Register to be arithmetically shifted right by 32 bits (with sign extension) and added to the multiplier output. At most one of the ADD, SUB and SHFT signals will normally be HIGH during a given cycle.

RND (Round)
The RND signal causes rounding of the most significant bit of the least significant product.

FA (Format Adjust)
FA should be HIGH for operations on single precision two's complement fractions. The FA input has a cycle compensating register to hold the signal until it is required. This register is controlled by CLKP.

XPLD (Extended Product Load)
XPLD selects the 4 bits of the TEMP register to be fed into the feedback loop for accumulation. This is used to preload the XTP register.

OEP, OEXP
Active LOW 3-state enables for P0:31 and P32:35, respectively.

PSEL
When PSEL is LOW, the least significant bits of the P Register are available on the output bus. When PSEL is HIGH, the most significant bits of the P Register are available. The interaction of PSEL and FA is summarized in Table 1. The table shows the outputs at pins P0, P1:31 and at pins P32:35, in terms of the bits in the P and XTP Registers, PR0:67.

Table 1. Control Inputs for the P Register Outputs

FA	PSEL	P0	P1:31	P32:35
0	0	PR0	PR1:31	PR32:35
0	1	PR32	PR33:63	PR64:67
1	0	0	PR0:30	PR31:34
1	1	PR31	PR32:62	PR63:66

TEST
When HIGH, all internal registers operate in the scan-test mode. Scan registers are clocked via the normal input clocks for each set of registers.

TIP, TIX (Test Inputs P and X)
The scan test inputs to the P and X Registers. The inputs are to the least significant bits of each register. The scan test output from the X Register passes through the Y and I Registers before becoming available externally. The scan test output from the P Register passes through the TEMP register and FA2 (Format Adjust Delay) register before becoming available externally.

TOP, TOI (Test Outputs P and I)
The scan test outputs from the P and I Registers.

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X and Y Data Input Formats

Unsigned integer (TCX, TCY = 0)

31	30	29	• • •	2	1	0
2^{31}	2^{30}	2^{29}	• • •	2^{2}	2^{1}	2^{0}

Two's complement integer (TCX, TCY = 1)

31	30	29	• • •	2	1	0
-2^{31}	2^{30}	2^{29}	• • •	2^{2}	2^{1}	2^{0}

Unsigned fractional (TCX, TCY = 1)

31	30	29	• • •	2	1	0
2^{-1}	2^{-2}	2^{-3}	• • •	2^{-30}	2^{-31}	2^{-32}

Two's complement fractional (TCX, TCY = 1)

31	30	29	• • •	2	1	0
-2^{0}	2^{-1}	2^{-2}	• • •	2^{-29}	2^{-30}	2^{-31}

Numerical Output Formats

Unsigned integer (FA = HIGH)

	P31	P30	P29	• • •	P2	P1	P0
PSEL = 1	2^{63}	2^{62}	2^{61}	• • •	2^{34}	2^{33}	2^{32}
PSEL = 0	2^{31}	2^{30}	2^{29}	• • •	2^{2}	2^{1}	2^{0}

Two's complement integer (FA = HIGH)

	P31	P30	P29	• • •	P2	P1	P0
PSEL = 1	-2^{63}	2^{62}	2^{61}	• • •	2^{32}	2^{33}	2^{32}
PSEL = 0	2^{31}	2^{30}	2^{29}	• • •	2^{2}	2^{1}	2^{0}

Unsigned fractional (FA = HIGH)

	P31	P30	P29	• • •	P2	P1	P0
PSEL = 1	2^{-1}	2^{-2}	2^{-3}	• • •	2^{-30}	2^{-31}	2^{-32}
PSEL = 0	2^{-33}	2^{-34}	2^{-35}	• • •	2^{-62}	2^{-63}	2^{-64}

Two's complement fractional, unshifted (FA = HIGH)

	P31	P30	P29	• • •	P2	P1	P0
PSEL = 1	-2^{1}	2^{0}	2^{-1}	• • •	2^{-28}	2^{-29}	2^{-30}
PSEL = 0	2^{-31}	2^{-32}	2^{-33}	• • •	2^{-60}	2^{-61}	2^{-62}

Two's complement fractional, shifted (FA = HIGH)

	P31	P30	P29	• • •	P2	P1	P0
PSEL = 1	-2^{0}	2^{-1}	2^{-2}	• • •	2^{-29}	2^{-30}	2^{-31}
PSEL = 0	2^{-32}	2^{-33}	2^{-34}	• • •	2^{-61}	2^{-62}	0

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Accumulator Operation

Table 2. Accumulator Operation–Normal Operation (XPLD = LOW)

Control Inputs				
ADD	SUB	SHFT	Operation	Result
L	L	L	Pass	PRi = X • Y
H	L	L	Positive Accumulation	PRi = X • Y + PR (i-1)
L	H	L	Negative Accumulation	PRi = X • Y - PR (i - 1)
L	L	H	Shift and Positive Accumulation	PRi = X • Y + [PR (i - 1) ÷ 2^{32}]

PRi = Product currently being calculated.
PR (i-1) = Product which was previously stored in the output register.

Table 3. Accumulator Operation During Preload (XPLD = HIGH) P64 Through P67 Only

Control Inputs				
ADD	SUB	SHFT	XPLD	Operation
L	L	L	H	XP ←TEMP
H	L	L	H	XP ←TEMP and PRi ←X • Y + PR (i-1)

Preloading Product Register

The 67-bit Product Register can be preloaded either through the output scan chain or through the TEMP register and a series of multipliers.

The output scan chain becomes active when TEST = HIGH. Preload data can then be serially shifted into the Product Register through the TIP input. The shifting operation is controlled by CLKP which cycles 67 times to load the entire Product Register.

Alternately, the Product Register may be preloaded as described in Table 4. The TEMP register is used to preload the 4-bit eXTended Product (XTP) while the balance of the Product Register is loaded by a series of three multiples with accumulation. Using this technique, the Product Register can be preloaded in five clock cycles.

Table 4. Product Register Preload

Cycle	0	1	2	3	4
Operation	Input A Input B and (2^{32} - 1)	Multiply B x 2^{32} - 1 Input B Load XTP Register	Multiply B x 1 and Add to Previous Result Input C	Multiply C x 1 and Add to Previous Result	Operation Complete
Data Inputs					
X0:31	B	B	C	X	
Y0:31	2^{32} - 1	1	1	1	
P32:35	A	X	X	X	
Register Contents					
X Register		B	B	C	
Y Register		2^{32} - 1	1	1	
TEMP Register		A	–	–	
P Register			B x (2^{32} - 1)	B = [B x (2^{32} - 1)]	(B x 2^{32}) + C
XTP Register			A	A	A

Notes:
1. 2^{32} - 1 is the largest number which can be entered into a 32-bit input.
2. An alternate preload method would be to scan data directly into the Product Register from TIP while TEST = HIGH.

Performs Operation of
(XTP x 2^{64}) + (MSP x 2^{32}) + LSP =
(XTP x 2^{64}) + [MSP x (2^{32} - 1)] + MSP + LSP
Where A = XTP = P67 to P64
B = MSP = P63 to P32
C = LSP = P31 to P0

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64 x 64-Bit Multiplication

Double precision 64 x 64-bit multiplication can be accomplished using the L64032. This operation will take a maximum of six clock cycles as shown below. In a pipelined mode, a new 64 x 64-bit result can be obtained in four clock cycles by overlapping cycles 0 and 4 and cycles 1 and 5.

Each 64-bit input must be split into two 32-bit inputs; a most significant half and a least significant half (X1 and X0 or Y1 and Y0, respectively). These 32-bit inputs are then used to perform the four multiplications necessary to obtain the 128-bit product. The product is represented by four 32-bit words (P3 through P0).

Table 5. 64 x 64 Multiplication

Cycle Operation	0 Load Inputs	1 Multiply	2 Multiply Shift/Accumulate	3 Multiply Accumulate	4 Multiply Shift/Accumulate	5 Display Results
Data Inputs						
X	X0	X1	X0	X1		
Y	Y0	Y0	Y1	Y1		
Control Signals						
TCX	0	1	0	1		
TCY	0	0	1	1		
ADD	0	0	1	0		
SHFT	0	1	0	1		
PSEL	Don't Care	Don't Care	0	Don't Care	0	0/1*
Register Contents						
X Register	–	X0	X1	X0	X1	
Y Register	–	Y0	Y0	Y1	Y1	
Data Output			P0	Note 1	P1	P2/P3 Note 2

Notes:
1. Output state dependent upon PSEL Input.
2. Two words of product read in a single cycle.

64 x 64 Multiplication

```
                X1   X0
x               Y1   Y0
-----------------------
                X0 x Y0
          X1 x Y0
          X0 x Y1
+ X1 x Y1
-----------------------
  P3   P2   P1   P0
```

X1, X0 = 64-bit X input
Y1, Y0 = 64-bit Y input
P3–P0 = 128-bit product

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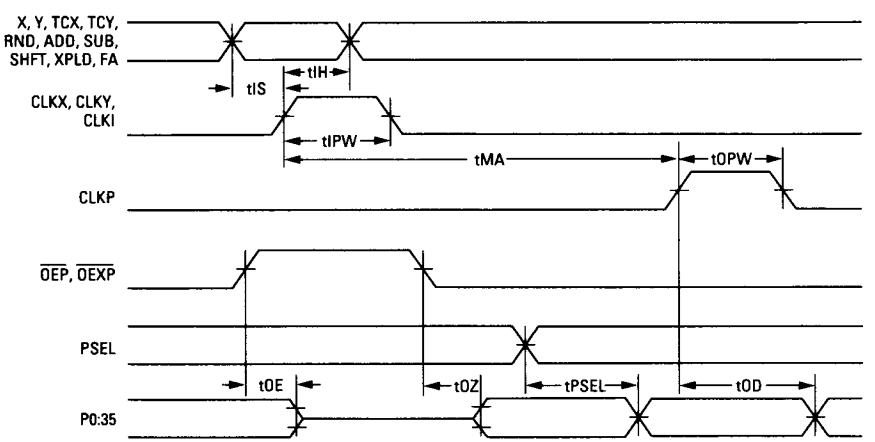
AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64032-12		L64032-10		L64032-80		Units	Notes
		Min	Max	Min	Max	Min	Max		
Normal Operation									
tMA	Multiply-accumulate cycle time		125		100		80	ns	
tIS	Input data setup time	20		15		15		ns	
tIH	Input data hold time	3		3		3		ns	
tIPW	Input register minimum pulse width	20		20		20		ns	
tOD	Output delay from CLKP		45		35		30	ns	
tPSEL	Output delay from PSEL		45		35		30	ns	
tOPW	Output register minimum pulse width (CLKP)	20		20		20		ns	CL = 50 pF
tOE	Output enable time		40		30		25	ns	
tOZ	Output disable time							ns	

AC Switching Characteristics: Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64032-16		L64032-12		L64032-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Normal Operation									
tMA	Multiply-accumulate cycle time		165		125		100	ns	
tIS	Input data setup time	25		20		20		ns	
tIH	Input data hold time	5		3		3		ns	
tIPW	Input register minimum pulse width	20		20		20		ns	
tOD	Output delay from CLKP		60		45		35	ns	
tPSEL	Output delay from PSEL		60		45		35	ns	
tOPW	Output register minimum pulse width (CLKP)	20		20		20		ns	CL = 50 pF
tOE	Output enable time		55		40		30	ns	
tOZ	Output disable time							ns	

AC Timing Waveforms **Normal Operation (TEST = LOW)**



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DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	LOW level input voltage						0.8	V
VIH	HIGH level input voltage Commercial temperature range Military temperature range				 2.0 2.25			 V V
IIN	Input current	VIN = VDD			-10	±1	10	µA
VOH	HIGH level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	LOW level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOZ	3-State output leakage current	VOH = VSS or VDD			-10	±1	10	µA
IOS	Output short circuit current[2]	VDD = Max, VO = VDD			25		90	mA
		VDD = Max, VO = 0V			-15		-60	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current[3]	tMA = tCYCLE = 10MHz				180		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ± 10% power supply; commecial temperature range is 0°C to 70°C, ± 5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to + 7	V
Input voltage	VI	-0.3 to VDD + 0.3	V
DC input current	II	±10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to + 6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

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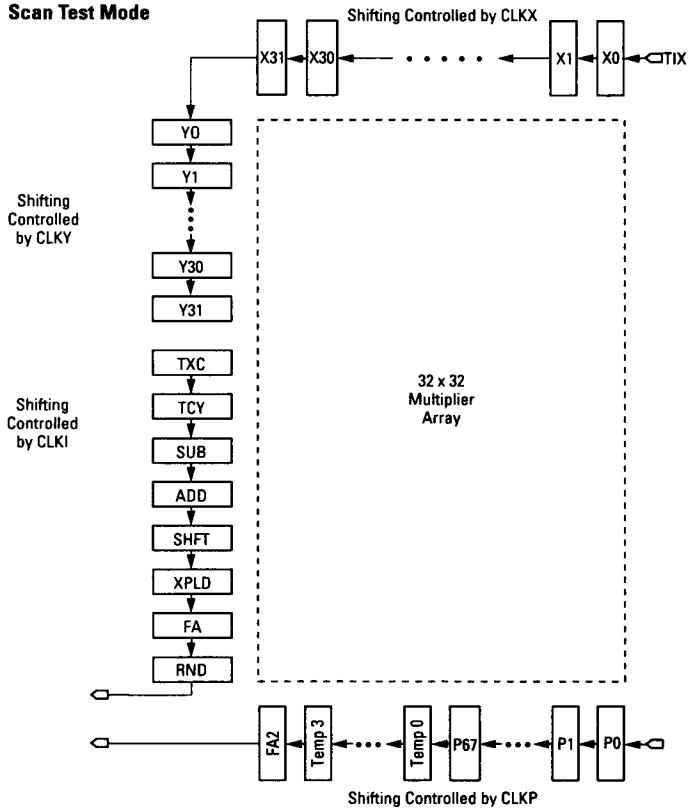
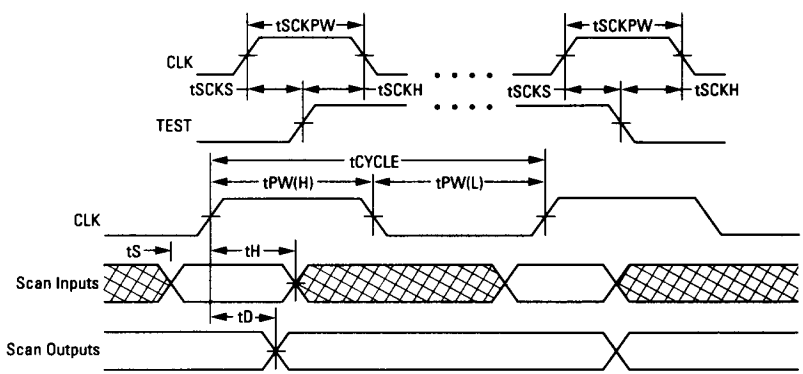
Block Diagram

Scan Test Mode



Scan Test Timing Waveforms



Notes:
1. On input scan chain, always apply CLKI at or before CLKY. Likewise apply CLKY at or before CLKX.
2. All clocks should be HIGH while entering and leaving TEST mode.

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Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	Y6	Y3	Y0	X31	X30	X27	X26	X23	X22	X19	X16	X14	X11	X9
B	Y8	Y7	Y4	Y1	CLKY	X28	X25	X24	X21	X18	X15	X12	VSS	X6
C	Y11	Y9	VSS	Y5	Y2	X29	VSS	VDD	X20	X17	X13	X10	X7	X3
D	Y13	Y12	Y10									X8	X4	X1
E	Y16	Y15	Y14									X5	X2	X0
F	Y19	Y18	Y17									CLKX	TIX	TEST
G	Y20	Y21	VDD				Top View					VSS	VDD	CLKP
H	Y23	Y22	VSS									PSEL	$\overline{OEP}$	TIP
J	Y24	Y25	Y26									P2	P1	P0
K	Y27	Y29	CLKI									P5	P4	P3
L	Y28	Y31	P33									P9	P7	P6
M	Y30	P34	TCX	ADD	RND	TOP	P27	VSS	P23	P17	P14	P12	P10	P8
N	P35	VSS	SUB	XPLD	TOI	P31	P28	VDD	P24	P20	P18	P15	VSS	P11
P	P32	TCY	SHFT	FA	$\overline{OEXP}$	P30	P29	P26	P25	P22	P21	P19	P16	P13

Packaging

132-Pin Ceramic Pin Grid Array: See FH Package in Package Selector Guide

Ordering Information

L64032 G C -XX

Cycle Time
80 = 80 nsecs
10 = 100 nsecs
12 = 125 nsecs
16 = 160 nsecs

Temperature Range/Flow Option
C – Commercial (0°C to 70°C)
M – Military (-55°C to + 125°C)

Package Code
G – 132-Lead Ceramic Pin Grid Array

Device Type
32 x 32-bit
Multiplier-Accumulator

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