

Section 20 Electrical Specifications

20.1 Absolute Maximum Ratings

Table 20-1 lists the absolute maximum ratings.

Table 20-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	−0.3 to +7.0	V
Programming voltage	V _{PP}	−0.3 to +13.5	V
Input voltage (except port 8)	V _{in}	−0.3 to V _{CC} + 0.3	V
(port 8)	V _{in}	−0.3 to AV _{CC} + 0.3	V
Analog supply voltage	AV _{CC}	−0.3 to +7.0	V
Analog input voltage	VA _N	−0.3 to AV _{CC} + 0.3	V
Operating temperature	T _{opr}	Regular specifications: −20 to +75	°C
		Wide-range specifications: −40 to +85	°C
Storage temperature	T _{stg}	−55 to +125	°C

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions.

20.2 Electrical Characteristics

20.2.1 DC Characteristics

Table 20-2 lists the DC characteristics.

Table 20-2 DC Characteristics

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%^{*1}$, $AV_{CC} = 5.0\text{ V} \pm 10\%^{*1}$, $V_{SS} = AV_{SS} = 0\text{ V}$,
 $T_a = -20\text{ to }+75^{\circ}\text{C}$ (Regular Specifications)
 $T_a = -40\text{ to }+85^{\circ}\text{C}$ (Wide-Range Specifications)

		Sym- bol	Measurement				
Item		Min	Typ	Max	Unit	Conditions	
Input High voltage	<u>RES, STBY,</u>	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	<u>MD2, MD1, MD0</u>		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	<u>EXTAL</u>		2.2	—	$AV_{CC} + 0.3$	V	
	Port 8		2.2	—	$V_{CC} + 0.3$	V	
	Other input pins (except port 7)						
Input Low voltage	<u>RES, STBY,</u>	V_{IL}	−0.3	—	0.5	V	
	<u>MD2, MD1, MD0</u>		−0.3	—	0.8	V	
	Other input pins (except port 7)						
Schmitt trigger input voltage	Port 7	V_T^-	1.0	—	2.5	V	
		V_T^+	2.0	—	3.5	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input leakage current	<u>RES</u>	$ I_{in} $	—	—	10.0	μA	$V_{in} = 0.5$ to
	<u>STBY, NMI,</u>		—	—	1.0	μA	$V_{CC} - 0.5$ V
	<u>MD2, MD1, MD0</u>						
	Port 8		—	—	1.0	μA	$V_{in} = 0.5$ to $AV_{CC} - 0.5$ V
Leakage current in 3-state (off state)	Port 9, ports 7 to 1	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0.5$ to $V_{CC} - 0.5$ V
Input pull-up MOS current	Ports 6 and 5	$-I_P$	50	—	200	μA	$V_{in} = 0$ V
Output High voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu A$
			3.5	—	—	V	$I_{OH} = -1$ mA
Output Low voltage	All output pins (except RES)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6$ mA
	Port 4		—	—	1.0	V	$I_{OL} = 8$ mA
			—	—	1.2	V	$I_{OL} = 10$ mA
			—	—	—		
	<u>RES</u>		—	—	0.4	V	$I_{OL} = 2.6$ mA

Note: *1 AV_{CC} must be connected to a power supply line, even when the A/D converter is not used.

Table 20-2 DC Characteristics (cont)

Item		Sym- bol	Min	Typ	Max	Unit	Measurement Conditions
Input capacitance	$\overline{\text{RES}}$ H8/534	C_{in}	—	—	60	pF	$V_{\text{in}} = 0 \text{ V}$
	H8/536		—	—	100	pF	$f = 1 \text{ MHz}$
	NMI		—	—	30	pF	$T_{\text{a}} = 25^{\circ}\text{C}$
	All input pins except $\overline{\text{RES}}$, NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{cc}	—	25	40	mA	$f = 6 \text{ MHz}$
			—	30	50	mA	$f = 8 \text{ MHz}$
			—	35	60	mA	$f = 10 \text{ MHz}$
	Sleep mode		—	12	25	mA	$f = 6 \text{ MHz}$
			—	16	30	mA	$f = 8 \text{ MHz}$
			—	20	35	mA	$f = 10 \text{ MHz}$
	Standby		—	0.01	5.0	μA	$T_{\text{a}} \leq 50^{\circ}\text{C}$
			—	—	20.0	μA	$T_{\text{a}} > 50^{\circ}\text{C}$
Analog supply current	During A/D conversion	A_{Icc}	—	1.2	2.0	mA	
	While waiting		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

*2 Current dissipation values assume that V_{IH} min = V_{CC} − 0.5 V, V_{IL} max = 0.5 V, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 20-3 Allowable Output Current Sink Values

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,

T_a = −20 to +75°C (Regular Specifications)

T_a = −40 to +85°C (Wide-Range Specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Port 4	I _{OL}	—	—	10	mA
	RES		—	—	3.0	mA
	Other output pins		—	—	2.0	mA
Allowable output Low current sink (total)	Port 4, total of 8 pins	Σ I _{OL}	—	—	40	mA
	Total of all output pins		—	—	80	mA
Allowable output High current sink (per pin)	All output pins	−I _{OH}	—	—	2.0	mA
Allowable output High current sink (total)	Total of all output pins	Σ −I _{OH}	—	—	25	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 20-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 20-1 and 20-2.

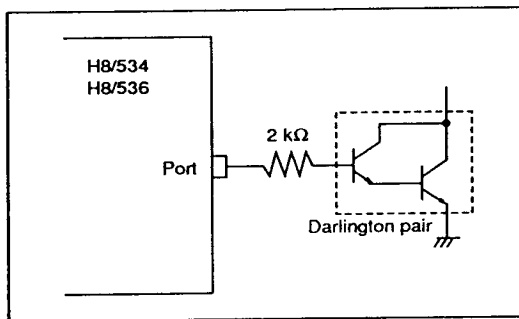


Figure 20-1 Example of Circuit for Driving a Darlington Transistor Pair

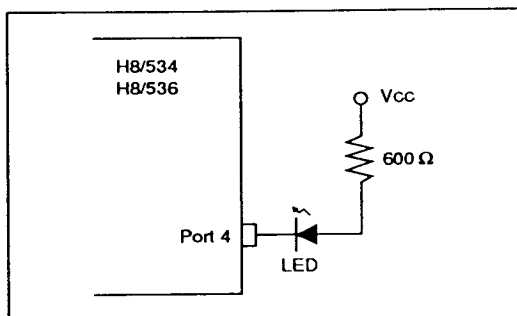


Figure 20-2 Example of Circuit for Driving an LED

20.2.2 AC Characteristics

The AC characteristics of the H8/534 and H8/536 are listed in three tables. Bus timing parameters are given in table 20-4, control signal timing parameters in table 20-5, and timing parameters of the on-chip supporting modules in table 20-6.

Table 20-4 Bus Timing

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $\phi = 0.5$ to 10 MHz , $V_{SS} = 0 \text{ V}$

$T_a = -20$ to $+75^\circ\text{C}$ (Regular Specifications)

$T_a = -40$ to $+85^\circ\text{C}$ (Wide-Range Specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
Clock cycle time	t_{cyc}	166.7	2000	125	2000	100	2000	ns	See figure 20-4
Clock pulse width Low	t_{CL}	65	—	45	—	35	—	ns	
Clock pulse width High	t_{CH}	65	—	45	—	35	—	ns	
Clock rise time	t_{Cr}	—	15	—	15	—	15	ns	
Clock fall time	t_{Cf}	—	15	—	15	—	15	ns	
Address delay time	t_{AD}	—	70	—	60	—	55	ns	
Address hold time	t_{AH}	30	—	25	—	20	—	ns	
Data strobe delay time 1	t_{DSD1}	—	70	—	60	—	40	ns	
Data strobe delay time 2	t_{DSD2}	—	70	—	60	—	50	ns	
Data strobe delay time 3	t_{DSD3}	—	70	—	60	—	50	ns	
Write data strobe pulse width	t_{DSWW}	200	—	150	—	120	—	ns	
Address setup time 1	t_{AS1}	25	—	20	—	15	—	ns	

Table 20-4 Bus Timing (cont)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
Address setup time 2	tAS2	105	—	80	—	65	—	ns	See figure 20-4
Read data setup time	tRDS	60	—	50	—	40	—	ns	
Read data hold time	tRDH	0	—	0	—	0	—	ns	
Read data access time	tACC	—	280	—	190	—	160	ns	
Write data delay time	tWDD	—	70	—	65	—	65	ns	
Write data setup time	tWDS	30	—	15	—	10	—	ns	
Write data hold time	tWDH	30	—	25	—	20	—	ns	
Wait setup time	tWTS	40	—	40	—	40	—	ns	See figure 20-5
Wait hold time	tWTH	10	—	10	—	10	—	ns	
Bus request setup time	tBRQS	40	—	40	—	40	—	ns	See figure 20-10
Bus acknowledge delay time 1	tBACD1	—	70	—	60	—	55	ns	
Bus acknowledge delay time 2	tBACD2	—	70	—	60	—	55	ns	
Bus floating delay time	tBZD	—	tBACD1	—	tBACD1	—	tBACD1	ns	
E clock delay time	tED	—	20	—	15	—	15	ns	See figure 20-11
E clock rise time	tEr	—	15	—	15	—	15	ns	
E clock fall time	tEf	—	15	—	15	—	15	ns	
Read data hold time (E clock sync)	tRDHE	0	—	0	—	0	—	ns	See figure 20-6
Write data hold time (E clock sync)	tWDHE	50	—	40	—	30	—	ns	

Table 20-5 Control Signal Timing

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $\phi = 0.5$ to 10 MHz , $V_{SS} = 0\text{ V}$

$T_a = -20$ to $+75^\circ\text{C}$ (Regular Specifications)

$T_a = -40$ to $+85^\circ\text{C}$ (Wide-Range Specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
RES setup time	tRESS	200	—	200	—	200	—	ns	See figure 20-7
RES pulse width 1 *	tRESW1	6.0	—	6.0	—	6.0	—	t _{cyc}	
RES pulse width 2 *	tRESW2	500	—	520	—	520	—	t _{cyc}	
RES output delay time	tRESO	—	100	—	100	—	100	ns	See figure 20-8
RES output pulse width	tRESOW	132	—	132	—	132	—	t _{cyc}	
NMI setup time	tNMIS	150	—	150	—	150	—	ns	See figure 20-9
NMI hold time	tNMIH	10	—	10	—	10	—	ns	
IRQ ₀ setup time	tIRQ0S	50	—	50	—	50	—	ns	
IRQ ₁ setup time	tIRQ1S	50	—	50	—	50	—	ns	
IRQ ₁ hold time	tIRQ1H	10	—	10	—	10	—	ns	
A/D trigger setup time	tTRGS	50	—	50	—	50	—	ns	See figure 20-22
A/D trigger hold time	tTRGH	10	—	10	—	10	—	ns	
NMI pulse width	tNMIW	200	—	200	—	200	—	ns	
(for recovery from software standby mode)									
Crystal oscillator settling time (reset)	tOSC1	20	—	20	—	20	—	ms	See figure 20-12
Crystal oscillator settling time (software standby)	tOSC2	10	—	10	—	10	—	ms	See figure 18-1

* tRESW2 applies at power-on and when the RSTOE bit in the reset control/status register (RSTCSR) is set to 1. tRESW1 applies when RSTOE is cleared to 0.

Table 20-6 Timing Conditions of On-Chip Supporting Modules

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $\phi = 0.5$ to 10 MHz , $V_{SS} = 0 \text{ V}$

$T_a = -20$ to $+75^\circ\text{C}$ (Regular Specifications)

$T_a = -40$ to $+85^\circ\text{C}$ (Wide-Range Specifications)

Item		Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
			Min	Max	Min	Max	Min	Max		
FRT	Timer output delay time	tFTOD	—	100	—	100	—	100	ns	See figure 20-14
	Timer input setup time	tFTIS	50	—	50	—	50	—	ns	
	Timer clock input setup time	tFTCS	50	—	50	—	50	—	ns	See figure 20-15
	Timer clock pulse width	tFTCWL, tFTCWH	1.5	—	1.5	—	1.5	—	t _{cyc}	
TMR	Timer output delay time	tTMOD	—	100	—	100	—	100	ns	See figure 20-16
	Timer clock input setup time	tTMCS	50	—	50	—	50	—	ns	See figure 20-17
	Timer clock pulse width	tTMCWL, tTMCWH	1.5	—	1.5	—	1.5	—	t _{cyc}	
	Timer reset input setup time	tTMRS	50	—	50	—	50	—	ns	See figure 20-18
	PWM	Timer output delay time	tPWOD	—	100	—	100	—	100	ns
SCI	Input clock cycle	(Async) tS _{cyc}	2	—	2	—	2	—	t _{cyc}	See figure 20-20
		(Sync)	4	—	4	—	4	—	t _{cyc}	
	Input clock pulse width	tSCKW	0.4	0.6	0.4	0.6	0.4	0.6	tS _{cyc}	
	Transmit data delay time	(Sync) tTXD	—	100	—	100	—	100	ns	See figure 20-21
	Receive data setup time	(Sync) tRXS	100	—	100	—	100	—	ns	
	Receive data hold time	(Sync) tRXH	100	—	100	—	100	—	ns	
Port	Output data delay time	tPWD	—	100	—	100	—	100	ns	See figure 20-13
	Input data setup time	tPRS	50	—	50	—	50	—	ns	
	Input data hold time	tPRH	50	—	50	—	50	—	ns	

• Measurement Conditions for AC Characteristics

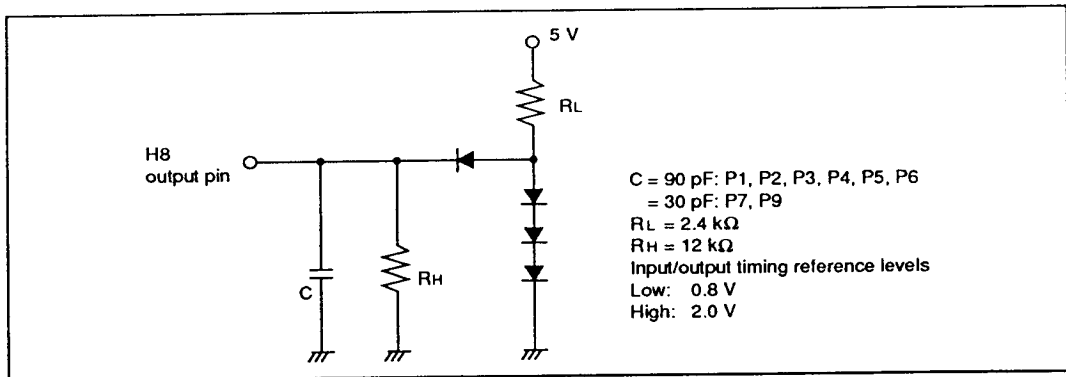


Figure 20-3 Output Load Circuit

20.2.3 A/D Converter Characteristics

Table 20-7 lists the characteristics of the on-chip A/D converter.

Table 20-7 A/D Converter Characteristics

Conditions: $V_{CC} = 5.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$,

$T_a = -20$ to $+75^\circ C$ (Regular Specifications)

$T_a = -40$ to $+85^\circ C$ (Wide-Range Specifications)

Item	6 MHz			8 MHz			10 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	μs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	k Ω
Nonlinearity error	—	—	± 2.0	—	—	± 2.0	—	—	± 2.0	LSB
Offset error	—	—	± 2.0	—	—	± 2.0	—	—	± 2.0	LSB
Full-scale error	—	—	± 2.0	—	—	± 2.0	—	—	± 2.0	LSB
Quantizing error	—	—	± 0.5	—	—	± 0.5	—	—	± 0.5	LSB
Absolute accuracy	—	—	± 2.5	—	—	± 2.5	—	—	± 2.5	LSB

20.3 MCU Operational Timing

This section provides the following timing charts:

20.3.1 Bus timing	Figures 20-4 to 20-6
20.3.2 Control Signal Timing	Figures 20-7 to 20-10
20.3.3 Clock Timing	Figures 20-11 and 20-12
20.3.4 I/O Port Timing	Figure 20-13
20.3.5 16-Bit Free-Running Timer Timing	Figures 20-14 and 20-15
20.3.6 8-Bit Timer Timing	Figures 20-16 to 20-18
20.3.7 Pulse Width Modulation Timer Timing	Figure 20-19
20.3.8 Serial Communication Interface Timing	Figure 20-20 and 20-21

20.3.1 Bus Timing

1. Basic Bus Cycle (without Wait States) in Expanded Modes

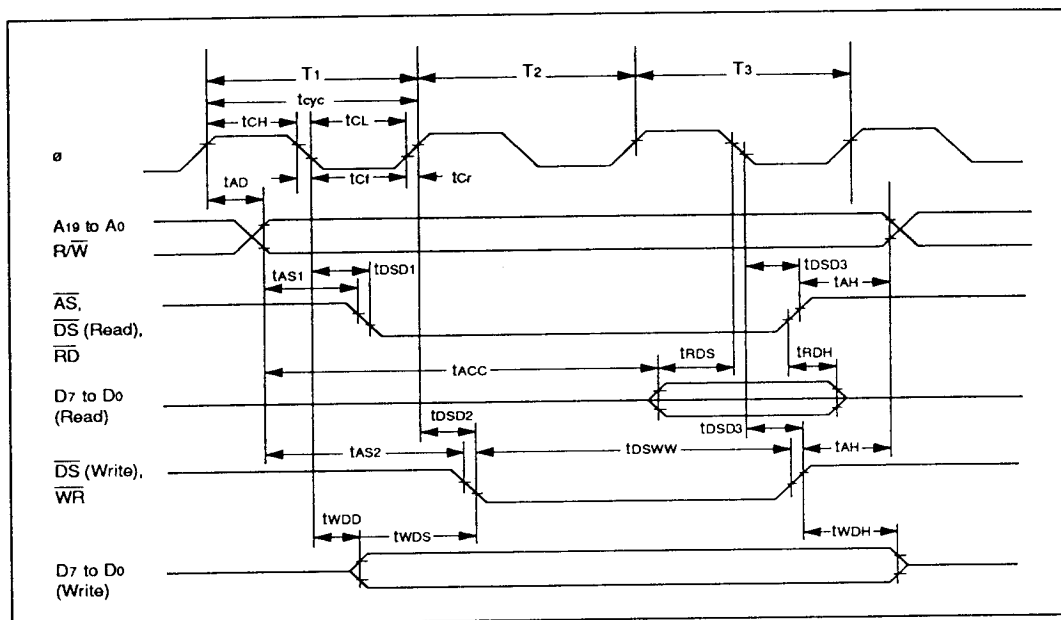


Figure 20-4 Basic Bus Cycle (without Wait States) in Expanded Modes

2. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

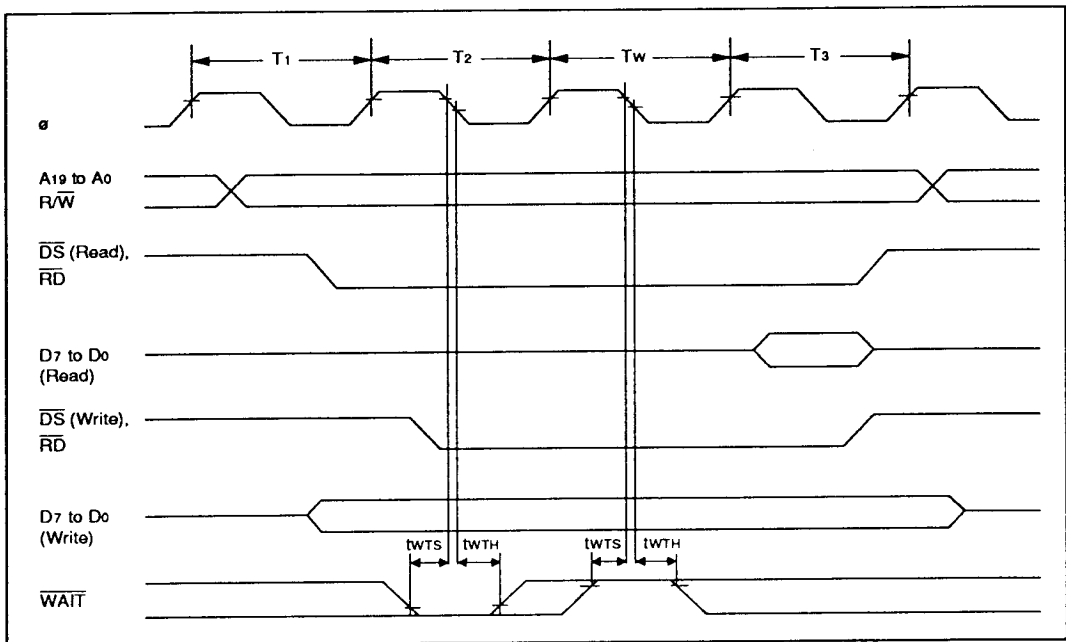


Figure 20-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes

3. Bus Cycle Synchronized with E Clock

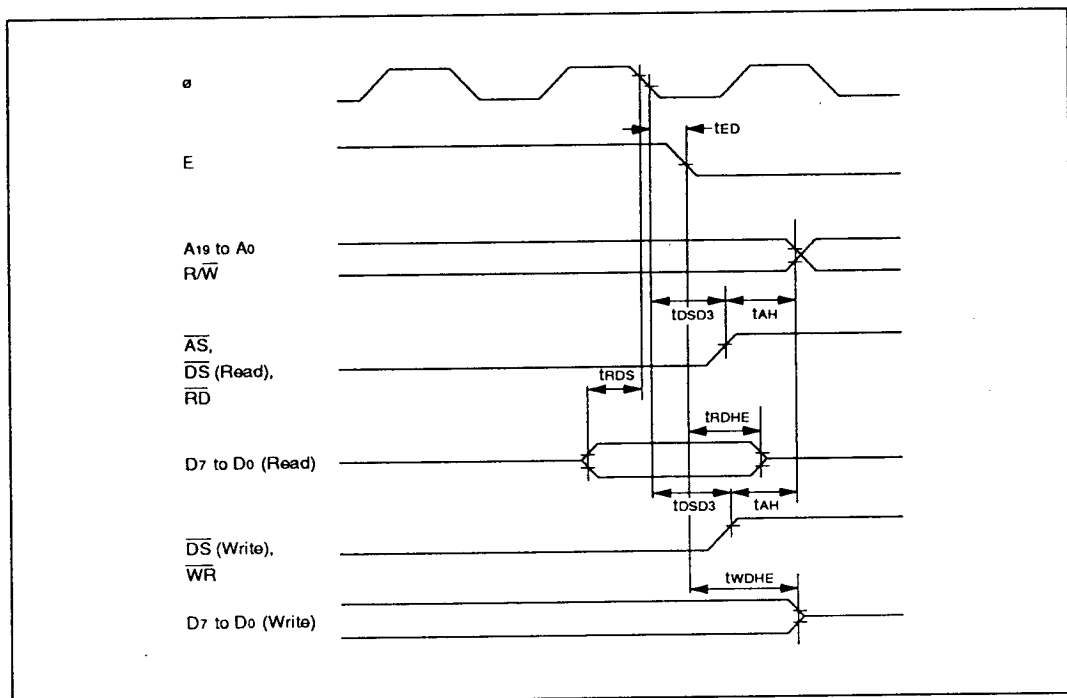


Figure 20-6 Bus Cycle Synchronized with E Clock

20.3.2 Control Signal Timing

1. Reset Input Timing

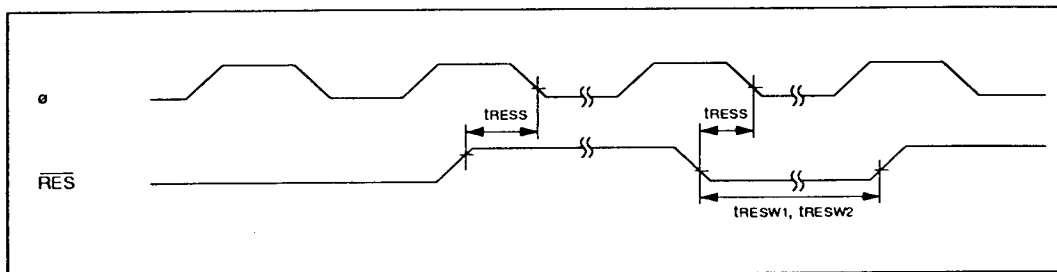


Figure 20-7 Reset Input Timing

2. Reset Output Timing

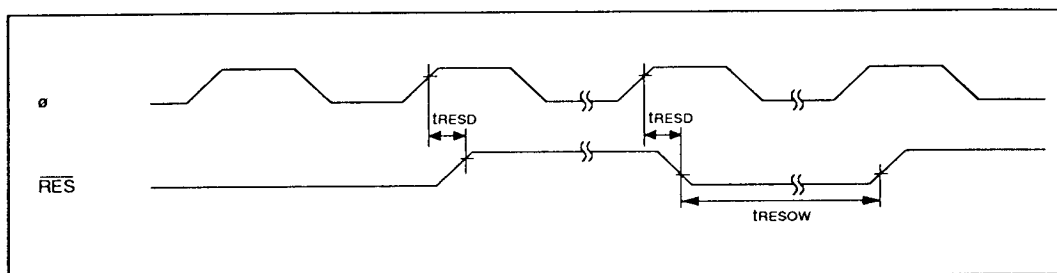


Figure 20-8 Reset Output Timing

3. NMI Pulse Width

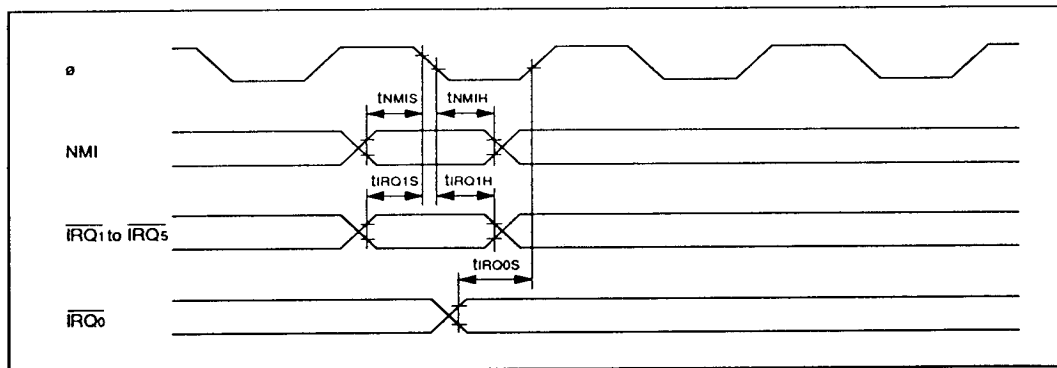


Figure 20-9 Interrupt Input Timing

4. Bus Release State Timing

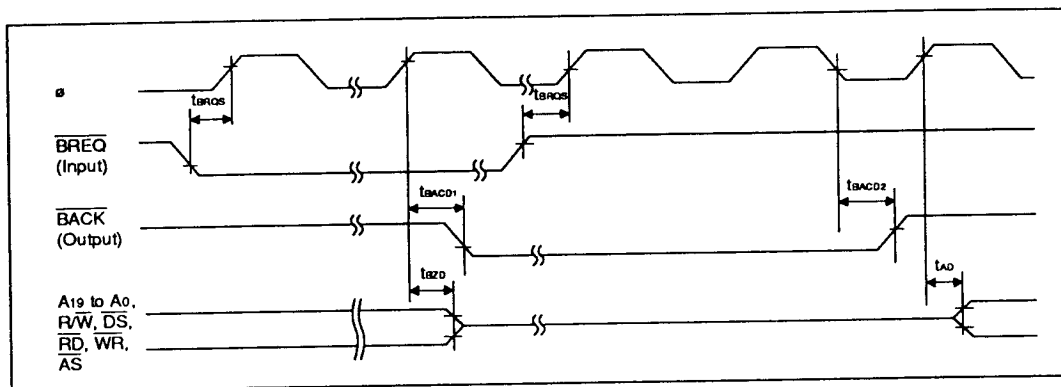


Figure 20-10 Bus Release State Timing

20.3.3 Clock Timing

1. E Clock Timing

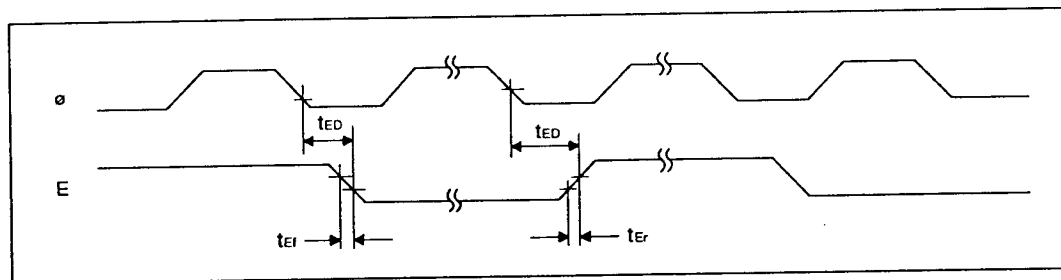


Figure 20-11 E Clock Timing

2. Clock Oscillator Stabilization Timing

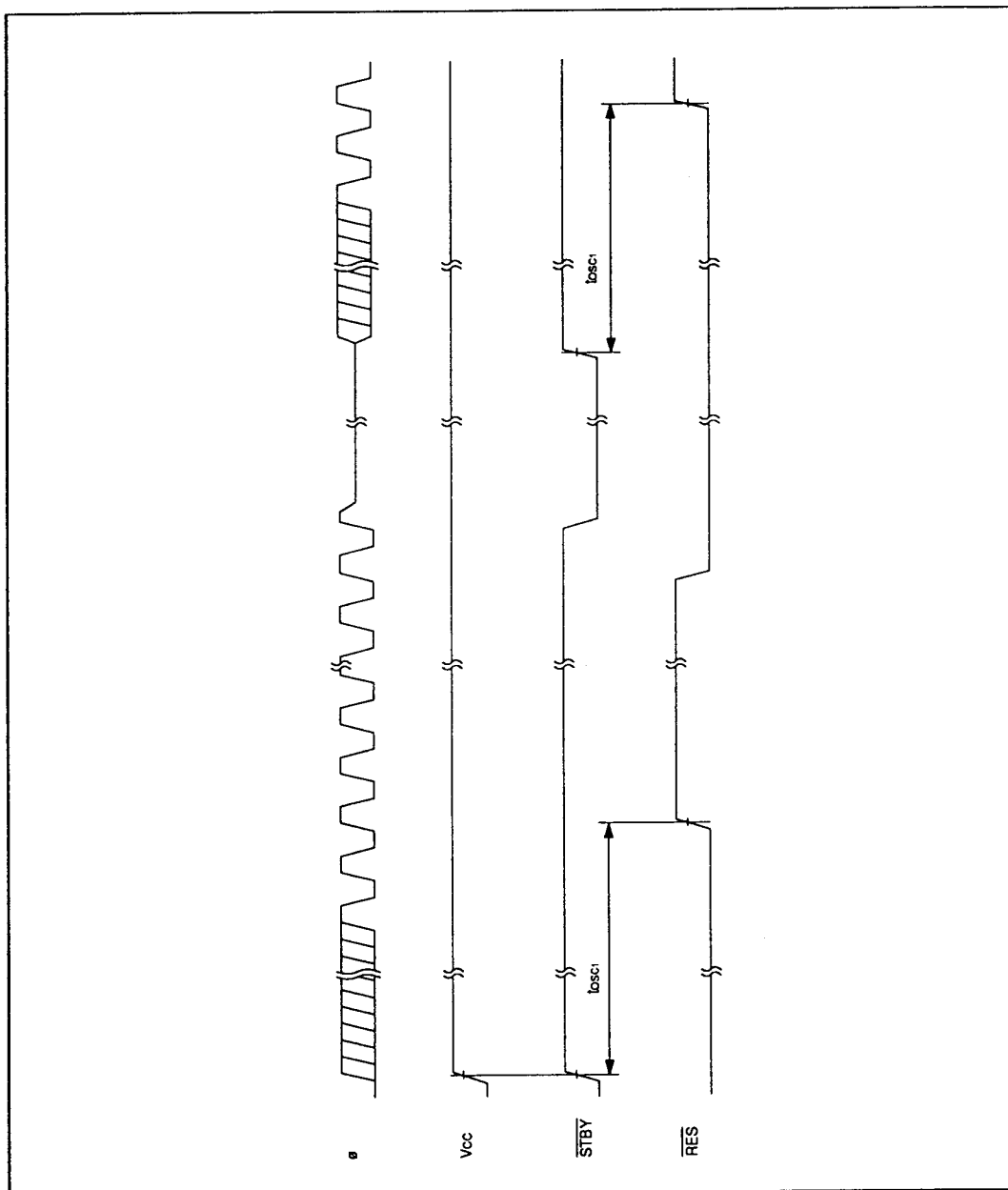


Figure 20-12 Clock Oscillator Stabilization Timing

20.3.4 I/O Port Timing

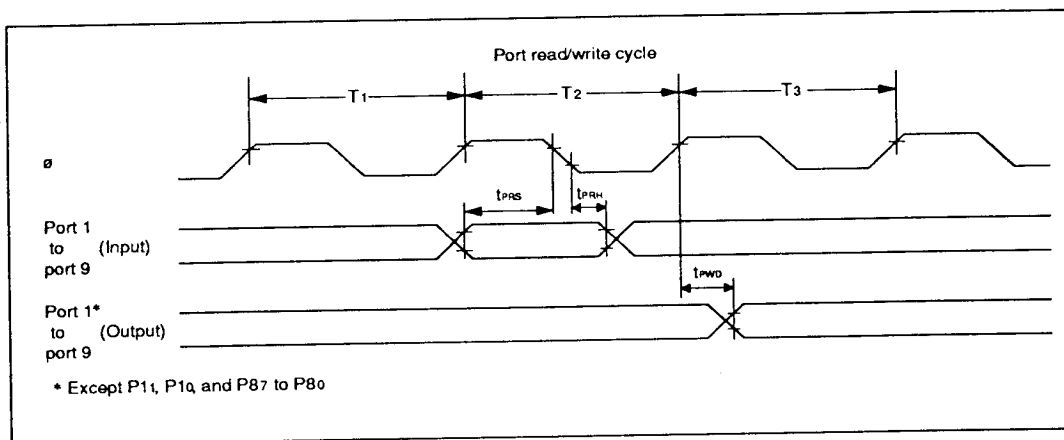


Figure 20-13 I/O Port Input/Output Timing

20.3.5 16-Bit Free-Running Timer Timing

1. Free-Running Timer Input/Output Timing

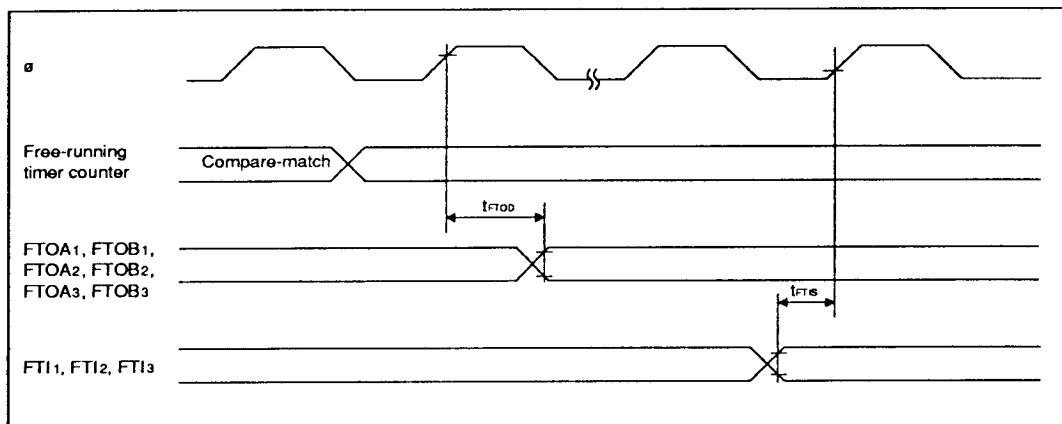


Figure 20-14 Free-Running Timer Input/Output Timing

2. External Clock Input Timing for Free-Running Timers

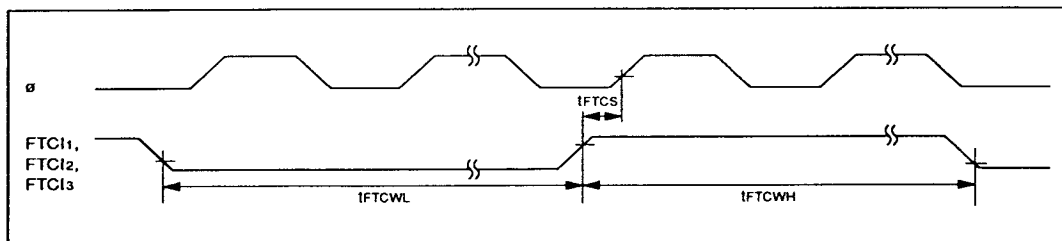


Figure 20-15 External Clock Input Timing for Free-Running Timers

20.3.6 8-Bit Timer Timing

1. 8-Bit Timer Output Timing

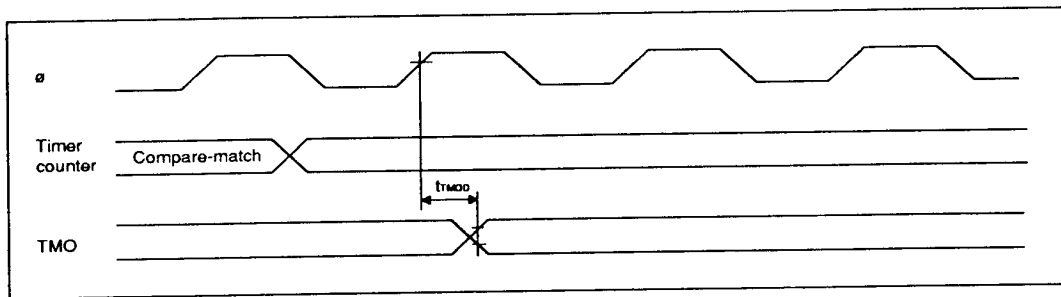


Figure 20-16 8-Bit Timer Output Timing

2. 8-Bit Timer Clock Input Timing

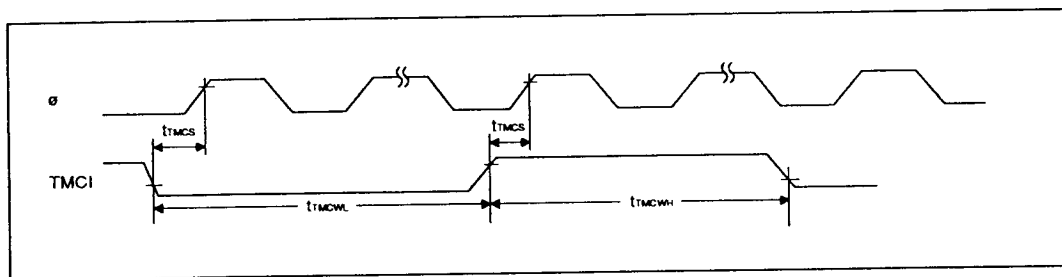


Figure 20-17 8-Bit Timer Clock Input Timing

3. 8-Bit Timer Reset Input Timing

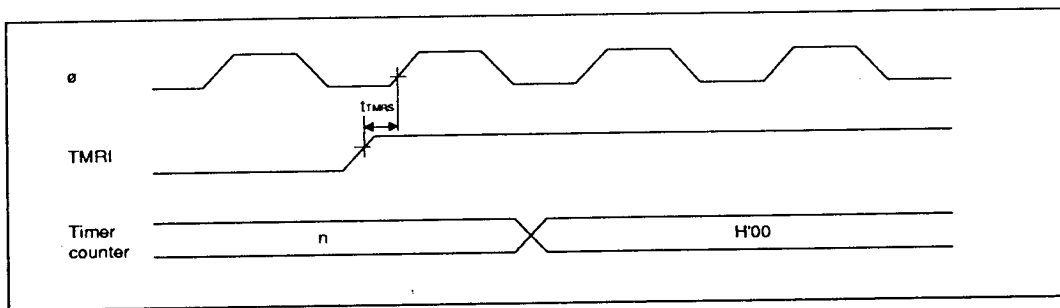


Figure 20-18 8-Bit Timer Reset Input Timing

20.3.7 Pulse Width Modulation Timer Timing

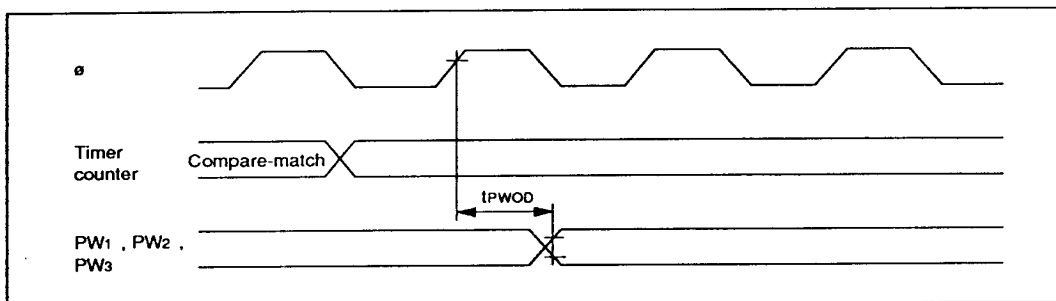


Figure 20-19 PWM Timer Output Timing

20.3.8 Serial Communication Interface Timing

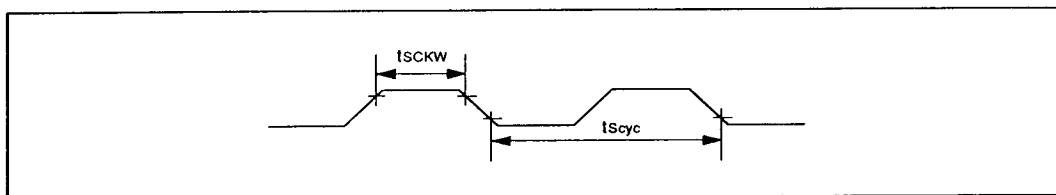


Figure 20-20 SCI Input Clock Timing

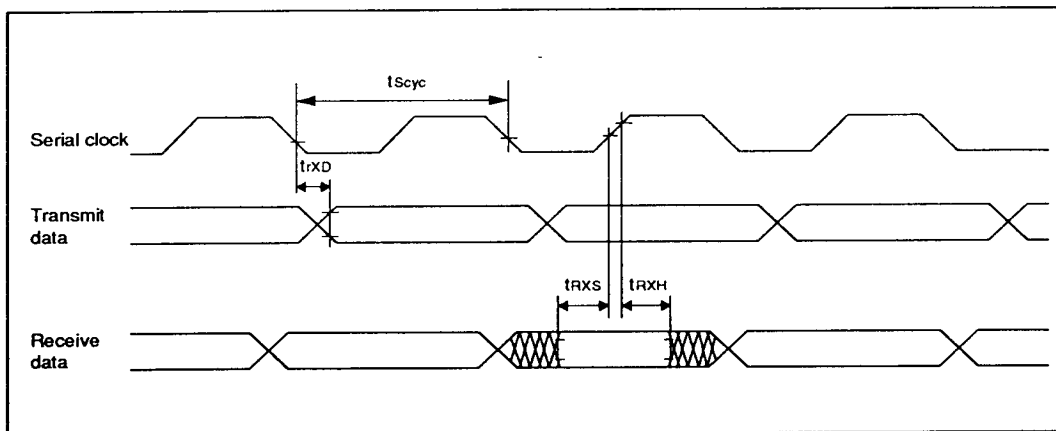


Figure 20-21 SCI Input/Output Timing (Synchronous Mode)

20.3.9 A/D Trigger Signal Input Timing

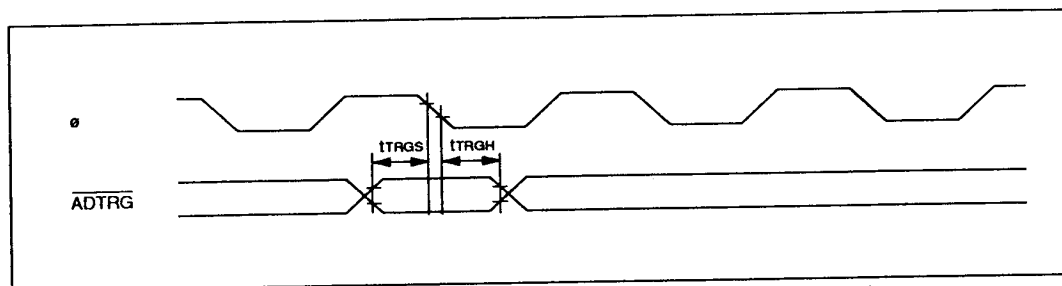


Figure 20-22 A/D Trigger Signal Input Timing