



# CEP9060N/CEB9060N

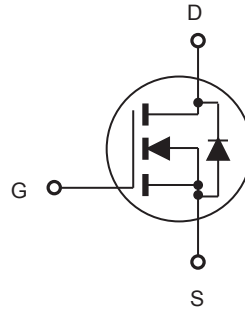
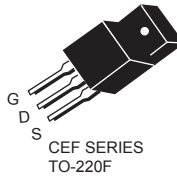
## CEF9060N

### N-Channel Enhancement Mode Field Effect Transistor

#### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP9060N	55V	10.5mΩ	90A	10V
CEB9060N	55V	10.5mΩ	90A	10V
CEF9060N	55V	10.5mΩ	90A <sup>e</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 package & TO-220F full-pak for through hole.



#### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	55		V
Gate-Source Voltage	V <sub>GS</sub>	±20		V
Drain Current-Continuous	I <sub>D</sub>	90	90 <sup>e</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>f</sup>	360	360 <sup>e</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	166	49	W
		1.11	0.33	W/°C
Single Pulsed Avalanche Energy <sup>d</sup>	E <sub>AS</sub>	325	325	mJ
Single Pulsed Avalanche Current <sup>d</sup>	I <sub>AS</sub>	50	50	A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175		°C

#### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.9	3	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



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### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	55			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 55V, V_{GS} = 0V$			25	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 62A$		8.5	10.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 25V, I_D = 62A$		30		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		3695		pF
Output Capacitance	$C_{oss}$			765		pF
Reverse Transfer Capacitance	$C_{rss}$			60		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 28V, I_D = 62A, V_{GS} = 10V, R_{GEN} = 4.5\Omega$		24	48	ns
Turn-On Rise Time	$t_r$			11.9	23.8	ns
Turn-Off Delay Time	$t_{d(off)}$			60	120	ns
Turn-Off Fall Time	$t_f$			19	38 <input type="checkbox"/>	ns
Total Gate Charge	$Q_g$	$V_{DS} = 44V, I_D = 62A, V_{GS} = 10V$		68.1	90.5	nC
Gate-Source Charge	$Q_{gs}$			12.6		nC
Gate-Drain Charge	$Q_{gd}$			22.7		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				62	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 62A$			1.3	V
<b>Notes :</b> <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . <input type="checkbox"/> c.Guaranteed by design, not subject to production testing. <input type="checkbox"/> d.L = 260 $\mu H$ , $I_{AS} = 50A, V_{DD} = 24V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ e.Limited only by maximum temperature allowed . f.Pulse width limited by safe operating area .						



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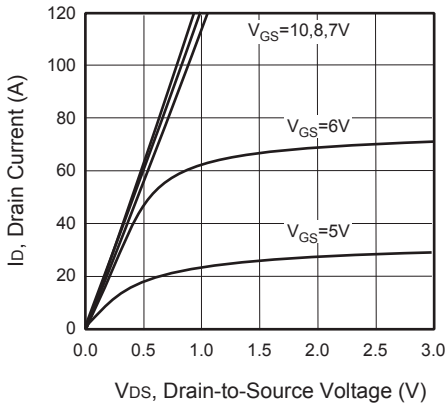


Figure 1. Output Characteristics

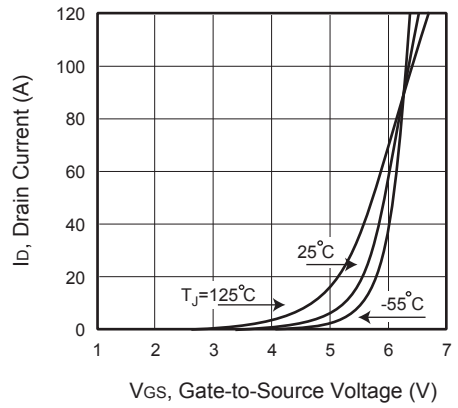


Figure 2. Transfer Characteristics

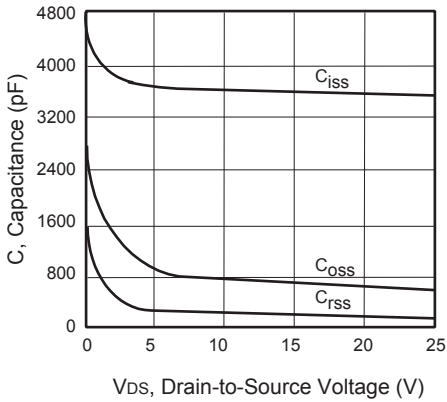


Figure 3. Capacitance

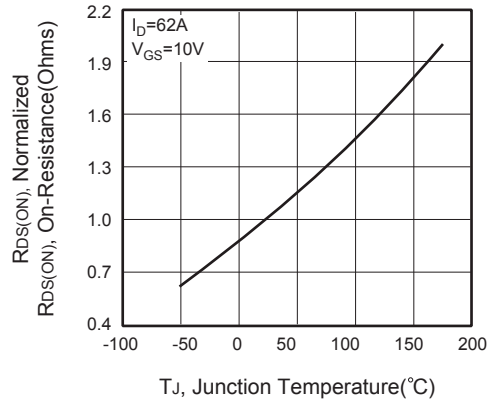


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

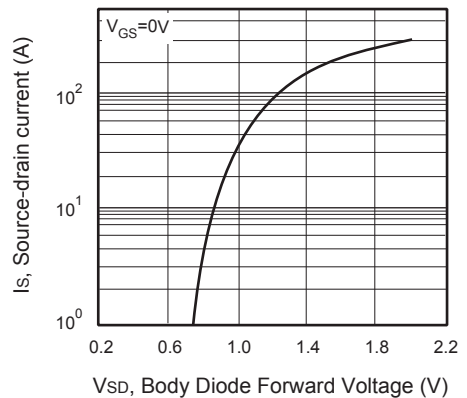
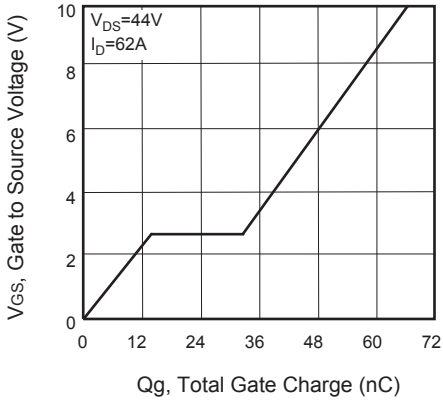


Figure 6. Body Diode Forward Voltage Variation with Source Current

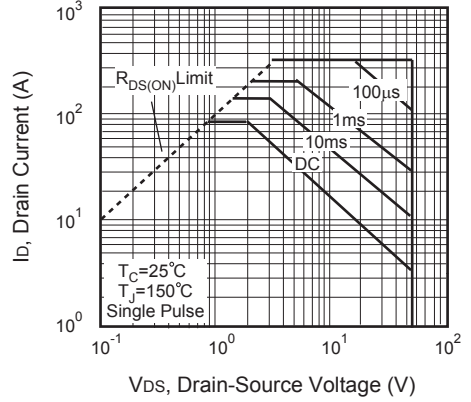


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**Figure 7. Gate Charge**



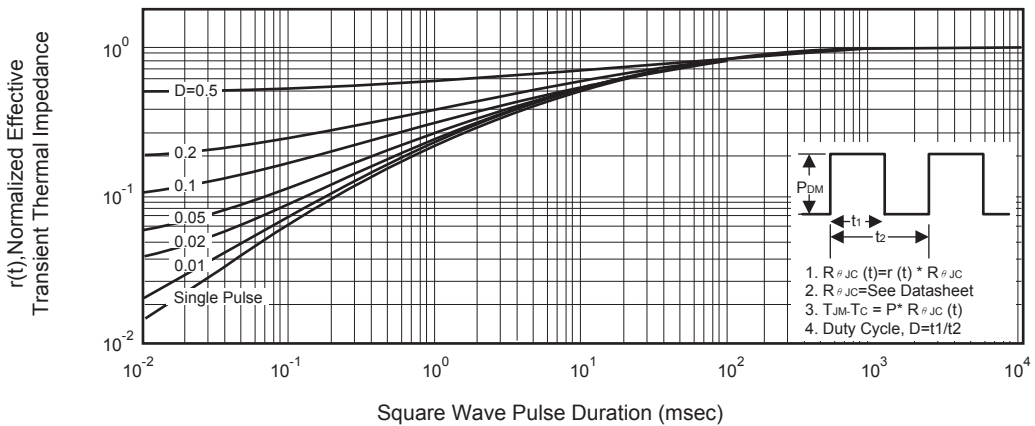
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Switching Test Circuit**



**Figure 10. Switching Waveforms**



**Figure 11. Normalized Thermal Transient Impedance Curve**