

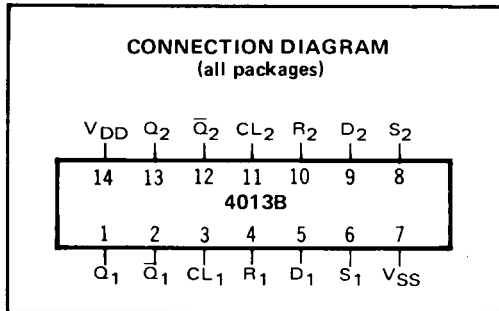
## CMOS DUAL D-TYPE FLIP-FLOP

### FEATURES

- ◆ Independent Set and Reset Controls
- ◆ Static Operation
- ◆ Logic Edge-Clocked Design
- ◆ 16MHz Toggle Rate @ 10Vdc

### DESCRIPTION

The 4013B consists of two identical, independent D-type Flip-Flops. These devices can be used for shift register applications, and, by connecting the  $\bar{Q}$  output to the Data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the Clock pulse. Setting or resetting is independent of the Clock and is accomplished by a high level on the Set or Reset line, respectively.



### RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

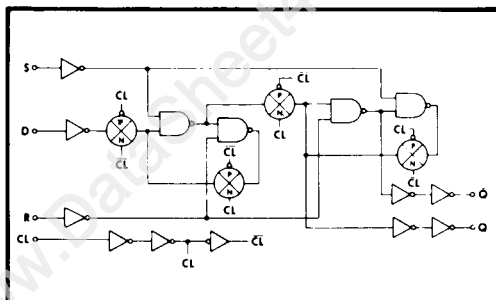
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	$T_A$	-55 to +125	°C
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

### TRUTH TABLE

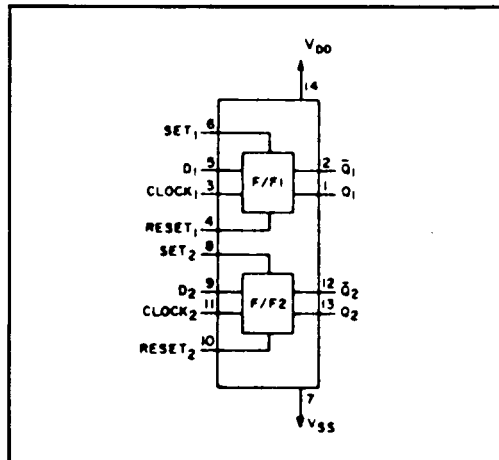
CL $\Delta$	D	R	S	Q	$\bar{Q}$	
	0	0	0	0	1	
	1	0	0	1	0	
	x	0	0	Q	$\bar{Q}$	NO CHANGE
x	x	1	0	0	1	
x	x	0	1	1	0	
x	x	1	1	1	1	

$\Delta$  = Level Change  
x = Don't Care

### LOGIC DIAGRAM



### BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	V <sub>DD</sub> (Vdc)	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	V <sub>DD</sub>	V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	-	1.0	-	0.005	1.0	-	30	μA <sub>dc</sub>
			-	2.0	-	0.01	2.0	-	60	
			-	4.0	-	0.02	4.0	-	120	

NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications."

<sup>2</sup> T<sub>LOW</sub> = -55°C for C, D, F, H device.

= -40°C for E device.

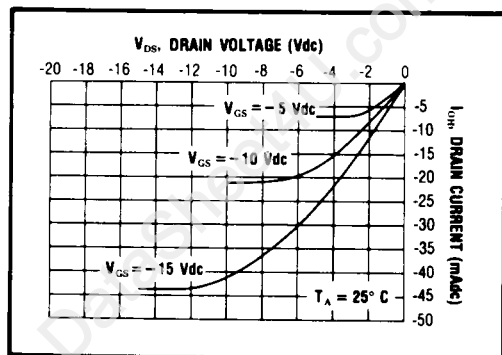
T<sub>HIGH</sub> = +125°C for C, D, F, H device.

= + 85°C for E device.

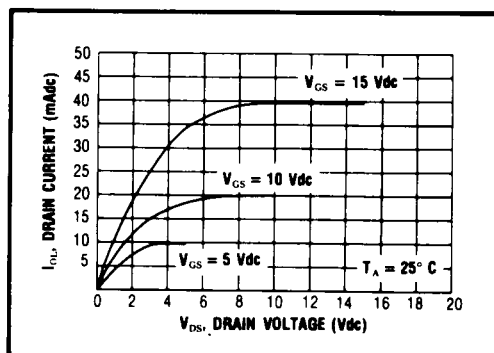
### DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C)

PARAMETER		V <sub>DD</sub> (Vdc)	Min.	Typ.	Max.	Units
<b>CLOCKED OPERATION</b>						
PROPAGATION DELAY TIME	t <sub>PLH</sub> , t <sub>PHL</sub>	5	-	125	250	ns
		10	-	65	130	
		15	-	45	90	
OUTPUT TRANSITION TIME	t <sub>TLH</sub> , t <sub>THL</sub>	5	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
MINIMUM CLOCK PULSE WIDTH	PW <sub>CL</sub>	5	-	70	140	ns
		10	-	30	60	
		15	-	20	40	
MAXIMUM CLOCK FREQUENCY	f <sub>CL</sub>	5	4.0	7.0	-	MHz
		10	8.0	16	-	
		15	12.5	25	-	
MAXIMUM CLOCK RISE AND FALL TIME <sup>1</sup>	t <sub>rCL</sub> , t <sub>fCL</sub>	5	15	-	-	μs
		10	10	-	-	
		15	5	-	-	
MINIMUM SETUP TIME	t <sub>setup</sub>	5	-	25	50	ns
		10	-	10	20	
		15	-	7.5	15	
MINIMUM HOLD TIME	t <sub>hold</sub>	5	-	-25	0	ns
		10	-	-10	0	
		15	-	-5	0	
<b>SET AND RESET OPERATIONS</b>						
PROPAGATION DELAY TIME S to Q, R to Q	t <sub>PLH</sub>	5	-	125	250	ns
		10	-	65	130	
		15	-	45	90	
MINIMUM SET AND RESET PULSE WIDTH	PW <sub>S</sub> , PW <sub>R</sub>	5	-	65	130	ns
		10	-	30	60	
		15	-	25	50	
SET AND RESET REMOVAL TIME	t <sub>rem</sub>	5	-	0	25	ns
		10	-	0	10	
		15	-	0	5	

<sup>1</sup>When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel  
Source Current Characteristics



Typical N-Channel  
Sink Current Characteristics