FEATURES

- Integrates two duplex DSX-1 compatible line interface circuits in a single monolithic device.
- Provides clock recovery and line performance monitoring in the receivers.
- Provides jitter attenuation and programmable line build out in the transmitters.
- Utilizes digital phase-locked loops for receive and transmit clock derivation without use of tuned circuits.
- Provides a crystal oscillator and clock doubler for optional on-chip generation of all required clock signals using either a 37.056 MHz or 18.528 MHz master clock.
- Provides a generic microprocessor interface for initial configuration, ongoing control, and status monitoring.
- Generates an interrupt upon detection of any of various alarms, events, or changes in status. Identification of interrupt sources, masking of interrupt sources, and acknowledgement of interrupts is provided via internal registers.
- Low power CMOS technology, 800 mW maximum power dissipation processing all ones signals.
- 84-pin PLCC package.

Each receiver section

- Supports reception of DSX-1 compatible signals using only an external 1:2 turns ratio transformer and passive attenuator components.
- Minimum sensitivity of 75 mV with a 1:2 turns ratio transformer allows for terminating or bridged performance monitoring applications.
- Recovers a 1.544 MHz clock and DS-1 data using a digital phase-locked loop to achieve high jitter accommodation.
- Accommodates up to 0.4 UI peak-to-peak, high frequency jitter as required by AT&T TR 64211.
- Optionally outputs either dual rail recovered line pulses or a single rail DS-1 signal.
- Optionally performs B8ZS decoding when processing a single rail DS-1 signal.

- Detects line code violations (LCVs), B8ZS signatures, 8 successive zeros, and 16 successive zeros.
- Accumulates up to 4095 line code violations (LCVs), for performance monitoring purposes, over accumulation intervals defined by the period between software write accesses to the LCV register.
- Detects loss of signal (LOS), which is defined as 176 successive zeros.
- Detects both programmable inband loopback activate and deactivate code sequences received in the DS-1 data stream when they are present for 5 seconds.
- Detects any pair of arbitrary inband codes from three to eight bits in length.
- The inband code detection algorithm operates in the presence of a 10^{-2} bit error rate.
- Programmable to detect CSU (Channel Service Unit), network, and far-end loopback codes.
- Detects in-band code sequences in both framed and unframed DS-1 streams.

Each transmitter section

- Generates DSX-1 compatible pulses with programmable pulse shape using only an external 1:1.36 turns ratio transformer.
- Selectable line length and line type for transmit pulse build out.
- Accommodates standard cable types such as ABAM or PIC.
- Includes special universal, square, and long line build out settings.
- Allows bipolar violation (BPV) transparent operation for error restoring regenerator applications.
- Supports all ones transmission for alarm indication signal (AIS) generation.
- Provides a digital phase-locked loop for generation of jitter reduced transmit output timing. The DPLL utilizes a 37.056 MHz master clock.
- Digital phase-locked loop locks 1.544 MHz output timing to the average frequency of the 1.544 MHz jittered transmit input clock.
- Provides a 2 x 48 bit FIFO for jitter attenuation in the transmit path.
- Provides up to 55 dB of jitter attenuation as per AT&T TR 62411.

- Digital phase-locked loop introduces minimal phase jitter; ± 0.042 UI peak to peak.
- Provides FIFO overrun and underrun indicators.
- Inhibits FIFO overrun and underrun for excessive jitter amplitudes.
- Generates a programmable inband loopback code sequence in the PCM voice channel data stream of a DS1 signal.
- Programmable to transmit repetitions of any arbitrary code from three to eight bits in length.
- Supports transmission of unframed loopback code sequences.
- Optionally inputs either dual rail transmit line pulses or a single rail DS-1 signal.
- Optionally performs B8ZS encoding when processing a single rail DS-1 signal.

APPLICATIONS

- Electronic DSX-1 Cross-connects (EDSX)
- Digital Access and Cross-connect Systems (DACS)
- Multiplexers
- Channel Service Units (CSUs)
- DSX-1 Repeaters
- Test Equipment

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DESCRIPTION

The PM4312 DDSX Dual DSX-1 Line Interface is a monolithic integrated circuit that supports DSX-1 compatible transmit and receive interfaces for two 1.544 Mbit/s data streams.

In the incoming direction, DSX-1 signals for each half of the DDSX are first processed by a receive data slicer. The receive data slicer converts the line signal received via a coupling transformer to dual rail RZ digital pulses. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. Through use of passive external attenuation circuitry, either terminated or bridge monitored DSX-1 signal levels can be accommodated. The low signal level condition or signal squelch may be enabled to generate interrupts. Clock and data are recovered from the dual rail RZ digital pulses using a digital phase-locked loop that provides excellent high frequency jitter accommodation. The recovered data is decoded using AMI, or optionally, B8ZS line code rules and is presented either as a DS-1 stream or presented in an undecoded dual rail NRZ format. Loss of signal and line code violations are detected as well as 8 successive zeros, 16 successive zeros, and the B8ZS signature. The presence of either of two programmable inband loopback codes is also detected. These various events or changes in status may be enabled to generate interrupts. Additionally, loss of signal and line code violations are also indicated on outputs.

In the outgoing direction, each half of the DDSX may accept either a DS-1 stream to be encoded using AMI, or optionally B8ZS, line code rules, or it may accept pre-encoded data in dual rail NRZ format. Jitter attenuation is provided by passing outgoing data through a FIFO. A low jitter clock is generated by an integral digital phase-locked loop and is used to read data from the FIFO. FIFO overrun or underrun may be enabled to generate interrupts. Alarm indication signal (all ones) may be substituted for the FIFO data. The digital data is converted to high drive, dual rail RZ pulses that drive the DSX-1 interface through a coupling transformer. The shape of the pulses is programmable to ensure that the DSX-1 pulse template is met after the signal is passed through various lengths of cable. Driver performance monitoring is provided and may be enabled to generate interrupts upon driver failure.

Internal high speed timing for both halves of the DDSX is provided by a common 37.056 MHz master clock. Support is provided for an external crystal. An 18.528 MHz crystal or clock source may be utilized by enabling an integral clock doubler circuit.

Diagnostic loopback is provided and the loopback may be invoked past the analog transmit outputs using the driver performance monitors or invoked prior to the

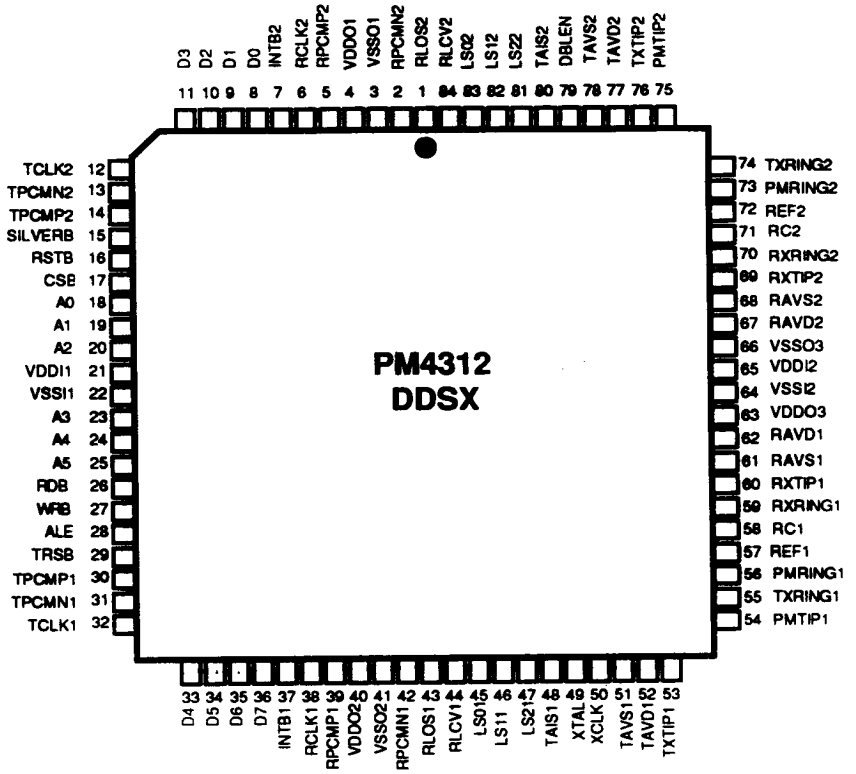
conversion to analog. Line loopback with jitter attenuation is provided and may be enabled for automatic operation based on detected inband loopback codes.

The DDSX may insert inband loopback code sequences into an outgoing unframed PCM data stream. These codes consist of continuous repetitions of specific bit sequences. Any arbitrary code from three to eight bits in length is programmable by writing to configuration registers.

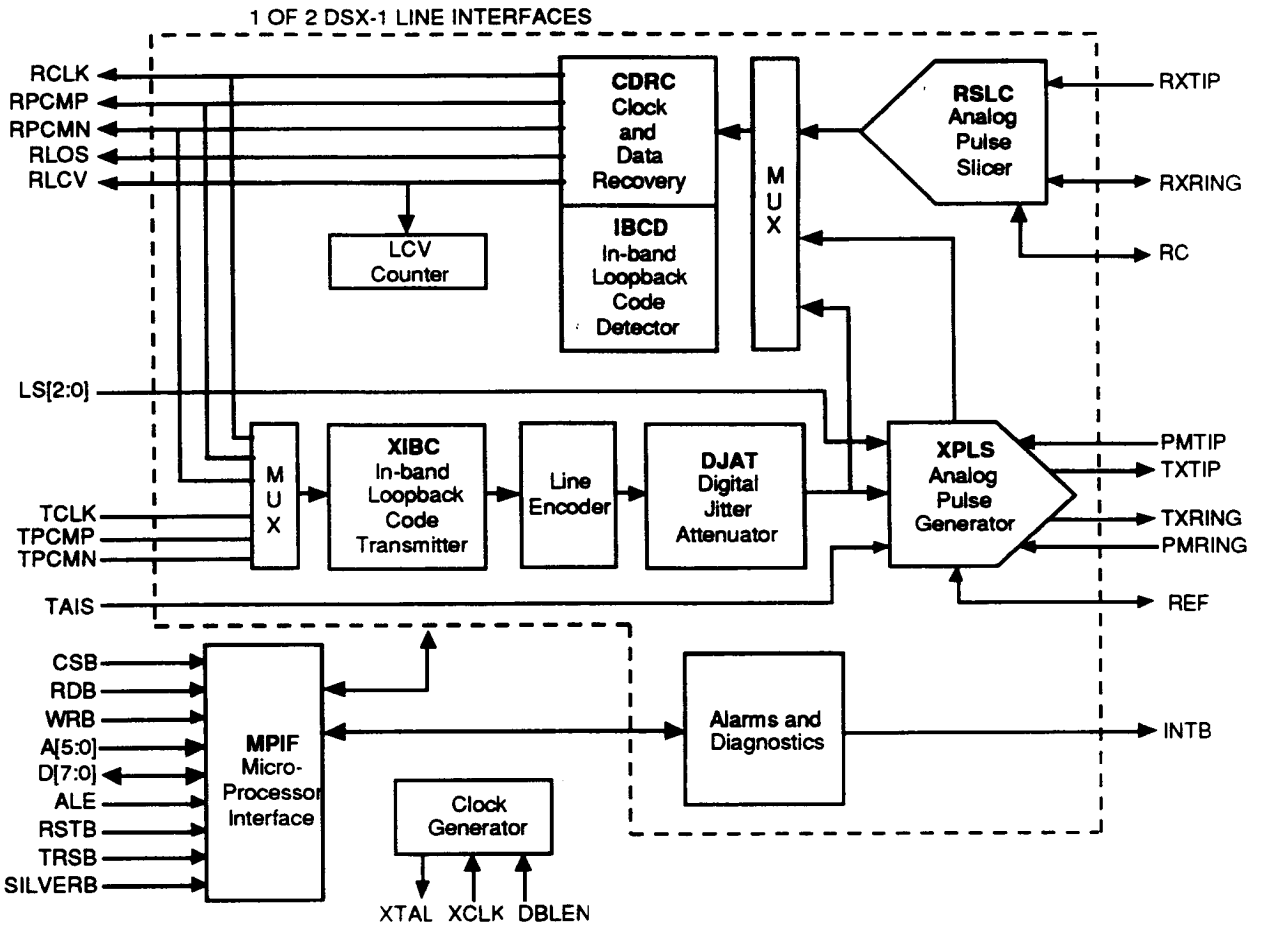
The DDSX operates in conjunction with external line coupling transformers, resistors, and capacitors. An external crystal may be used for high speed timing generation. The DDSX is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface.

PINOUT

The DDSX is packaged in an 84-pin PLCC package.



BLOCK DIAGRAM



PIN DESCRIPTION

Connector Name	Type	Pin No.	Function
XCLK/ VCLK	Input	50	The system clock (XCLK) provides timing for DDSX internal operation. XCLK may be driven externally or connected to an appropriate crystal. XCLK may be a 37.056 MHz or 18.528 MHz, 50% duty cycle clock, as selected by the DBLEN input. The test vector clock (VCLK) signal is used during DDSX production testing to verify internal functionality.
XTAL	Output	49	The crystal output (XTAL) may be connected to a crystal in conjunction with XCLK to form a crystal oscillator. When not used, XTAL should be left unconnected.
DBLEN	Input	79	The clock doubler enable (DBLEN) signal determines whether an internal clock doubler circuit is active. When DBLEN is low, the clock doubler is disabled and XCLK must be a 37.056 MHz clock for proper operation. When DBLEN is high, the clock doubler is enabled and XCLK must be a 18.528 MHz clock.
TXTIP1 TXTIP2	Analog Output	53 76	The transmit tip (TXTIP) signals drive the line through line coupling transformers associated with the corresponding DS-1 signal. These outputs can drive 54 Ω loads. Use of a 1:1.36 step up transformer is required.
TXRING1 TXRING2	Analog Output	55 74	The transmit ring (TXRING) signals drive the line through line coupling transformers associated with the corresponding DS-1 signal. These outputs can drive 54 Ω loads. Use of a 1:1.36 step up transformer is required.
PMRING1 PMRING2	Analog Input	56 73	The driver performance monitor ring (PMRING) inputs are used for driver performance monitoring. Each PMRING input can be connected to either its corresponding TXRING output, or an adjacent channel's TXRING output.

PMTIP1 PMTIP2	Analog Input	54 75	The driver performance monitor tip (PMTIP) inputs are used for driver performance monitoring. Each PMTIP input can be connected to either its corresponding TXTIP output, or an adjacent channel's TXTIP output.
TCLK1 TCLK2	I/O	32 12	The transmit PCM clock (TCLK) inputs provide timing for transmission of the corresponding DS-1 stream. The TCLK signals are nominally 1.544 MHz, 50% duty cycle clocks. The inputs TPCMP, TPCMN, and TAIS are sampled on the rising edge of the corresponding TCLK signal. Note that the TCLK signals may become outputs when SILVERB is low.
TPCMP1 TPCMP2	Input	30 14	The transmit positive PCM pulse (TPCMP) inputs are sampled on the rising edge of the corresponding TCLK signal. When a TPCMP input is high a positive pulse is generated across the corresponding TXTIP and TXRING outputs; TXTIP sources current and TXRING sinks current. Note that if a pair of TPCMP and TPCMN signals are both high, no pulse is generated. When dual rail interfacing is disabled, the TPCMP inputs carry DS-1 data that is encoded by the DDSX using AMI, or optionally, B8ZS line code rules.
TPCMN1 TPCMN2/ TEXP1 TEXP2	Input	31 13	The transmit negative PCM pulse (TPCMN) inputs are sampled on the rising edge of the corresponding TCLK signal. When a TPCMN input is high a negative pulse is generated across the corresponding TXTIP and TXRING outputs; TXRING sources current and TXTIP sinks current. Note that if a pair of TPCMP and TPCMN signals are both high, no pulse is generated. When dual rail interfacing is disabled, the TPCMN inputs are referred to as TEXP or are used to mark the framing bit position.
TAIS1 TAIS2	I/O	48 80	The transmit alarm indication signal (TAIS) inputs are sampled on the rising edge of the corresponding TCLK signal but may be asynchronous to TCLK. When TAIS is high, an all ones signal (alternating positive and negative pulses) is generated on the corresponding TXTIP and TXRING outputs. Note that the TAIS signals may become outputs when SILVERB is low.

RXTIP1 RXTIP2	Analog Input	60 69	The receive tip (RXTIP) inputs connect a line coupling transformer to the receive data slicer that processes the corresponding DS-1 stream. An external passive 20 dB attenuation network is required when interfacing to DSX-1 signal levels using a 1:2 step up transformer. The external attenuation network is not required in performance monitor applications where 20 dB of attenuation inherently occurs while bridging onto the DSX-1 signal.
RXRING1 RXRING2	Analog I/O	59 70	The receive ring (RXRING) signals provide a bias voltage for the line coupling transformer associated with the corresponding DS-1 stream. These nodes must be decoupled to ground with 0.1 µF capacitors.
RC1 RC2	Analog I/O	58 71	The external peak detector RC network (RC) signals connect the peak detector of the receive data slicer that processes the corresponding DS-1 stream to an external RC network. The RC network consists of a grounded, parallel resistor and capacitor network, with nominal values of 316K Ω and 47 nF, respectively.
RCLK1 RCLK2	Output	38 6	The recovered PCM clock (RCLK) signals are synchronized with the corresponding received 1.544 Mbit/s DS-1 signals. The RCLK signals are generated using digital phase-locked loops that use an 8 x (12.352 MHz) high speed clock. The instantaneous period of each RCLK signal can be seven, eight, or nine high speed clock (12.352 MHz) periods.
RPCMP1 RPCMP2	Output	39 5	The recovered positive PCM pulse (RPCMP) outputs are updated on the falling edge of the corresponding RCLK signal. When dual rail interfacing is disabled, the RPCMP outputs carry DS-1 data that is decoded by the DDSX assuming AMI, or optionally, B8ZS line code rules.
RPCMN1 RPCMN2	Output	42 2	The recovered negative PCM pulse (RPCMN) outputs are updated on the falling edge of the corresponding RCLK signal. When dual rail interfacing is disabled, the RPCMN outputs carry DS-1 data that is decoded by the DDSX assuming AMI line code rules.

RLOS1 RLOS2	Output	43 1	The receiver loss of signal (RLOS) outputs are set high upon detection of 176 consecutive zero bit intervals on the corresponding recovered PCM stream. The PCM streams are examined prior to optional B8ZS decoding. The RLOS outputs are reset low when a non-zero bit interval is detected on the corresponding recovered PCM stream. The RLOS outputs are updated on the falling edge of the corresponding RCLK signal.
RLCV1 RLCV2	Output	44 84	The receiver line code violation (RLCV) outputs are set high upon detection of a line code violation on the corresponding recovered PCM stream. Bipolar violations that are part of the B8ZS signature are not flagged as line code violations if optional B8ZS decoding is enabled. The RLCV outputs are updated on the falling edge of the corresponding RCLK signal.
REF1 REF2	Analog I/O	57 72	The voltage reference signals (REF) provide decoupling to the bias voltage generator in the Transmit Pulse Generator. These signals must be decoupled to TAVD with 470 nF capacitors, and must not be loaded.
LS01 LS02	I/O	45 83	The line length select (LS0) signals select the transmit pulse shape applied to the corresponding DSX-1 interface. The LS0 signal, and the corresponding LS1 and LS2 signals select one of eight transmit pulse shapes. Note that the LS0 signals become outputs when SILVERB is low. The LS0 signals have integral pull up resistors.
LS11 LS12	I/O	46 82	The line length select (LS1) signals select the transmit pulse shape applied to the corresponding DSX-1 interface. The LS1 signal, and the corresponding LS0 and LS2 signals select one of eight transmit pulse shapes. Note that the LS1 signals become outputs when SILVERB is low. The LS1 signals have integral pull up resistors.
LS21 LS22	I/O	47 81	The line length select (LS2) signals select the transmit pulse shape applied to the corresponding DSX-1 interface. The LS2 signal, and the corresponding LS0 and LS1 signals select one of eight transmit pulse shapes. Note that the LS2 signals become outputs when SILVERB is low. The LS2 signals have integral pull up resistors.

INTB1 INTB2	Output	37 7	The interrupt (INTB) signals go low when any of the various interrupting sources within the DDSX related to the corresponding DS-1 stream is active and is enabled to generate interrupts. The INTB signals go high when the interrupt is acknowledged by reading a status register or masked via the interrupt enable register. The INTB outputs are open drain outputs. Note that when SILVERB is low, the TSB interrupt signals reported on the INTB signals remain inverted.
CSB	Input	17	The active low chip select (CSB) signal is low during DDSX register accesses.
RDB	Input	26	The active low read enable (RDB) signal is low during a DDSX register read access. The DDSX drives the D7-D0 bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	27	The active low write strobe (WRB) signal is low during a DDSX register write access. The D7-D0 bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D0 D1 D2 D3 D4 D5 D6 D7	I/O	8 9 10 11 33 34 35 36	The bidirectional data bus (D7-D0) is used during DDSX register read and write accesses.
A0 A1 A2 A3-A5	Input	18 19 20 23:25	The address bus (A5-A0) selects specific registers during DDSX register accesses.
RSTB	Input	16	The active low reset (RSTB) signal provides an asynchronous DDSX reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	28	The address latch enable (ALE) is active high and latches the address bus (A5-A0) and TRSB when low. When ALE is high, the internal address latches are transparent. It allows the DDSX to interface to a multiplexed address/data bus. The ALE input will have an integral pull up resistor.

TRSB	Input	29	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test mode register accesses, and is high during normal mode register accesses. TRSB has an integral pull up resistor.
SILVERB	Input	15	The active low silicon verification mode select (SILVERB) signal places the DDSX in a mode where constituent TSBs are made visible for test purposes. In this mode, the functions of some of the digital inputs or outputs of the DDSX are redefined. For line interface operation this signal must be held high. SILVERB has an integral pull up resistor.
RAVD1 RAVD2	Power	62 67	The receive analog power (RAVD) connections each provide power to the receive data slicer in the corresponding DSX-1 interface. Each RAVD pin must be connected to a well decoupled +5 V DC supply.
RAVS1 RAVS2	Ground	61 68	The receive analog ground (RAVS) connections each provide ground for the receive data slicer in the corresponding DSX-1 interface.
TAVD1 TAVD2	Power	52 77	The transmit analog power (TAVD) connections each provide power for the transmit pulse generator in the corresponding DSX-1 interface. Each TAVD pin must be connected to a well decoupled +5 V DC supply.
TAVS1 TAVS2	Ground	51 78	The transmit analog ground (TAVS) connections each provide ground for the transmit pulse generator in the corresponding DSX-1 interface.
VDDI1 VDDI2	Power	21 65	The core power (VDDI) pins should be connected to a well decoupled +5 V DC in common with VDDO.
VSSI1 VSSI2	Ground	22 64	The core ground (VSSI) pins should be connected to GND in common with VSSO.
VDDO1 VDDO2 VDDO3	Power	4 40 63	The pad ring power (VDDO) pins should be connected to a well decoupled +5 V DC in common with VDDI.
VSSO1 VSSO2 VSSO3	Ground	3 41 66	The pad ring ground (VSSO) pins should be connected to GND in common with VSSI.

Notes on Pin Description:

1. All DDSX inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

2. All DDSX digital outputs and bidirectionals have 2 mA drive capability, except the INTB outputs and the D7-D0 bidirectionals, which have 4 mA drive capability.

3. The functions of inputs XCLK, DBLEN, TCLK, TCPMP, TPCMN, TAIS, and A5-A2 are redefined for test purposes when SILVERB is low.

4. The functions of outputs RCLK, RPCMP, RPCMN, RLOS, RLCV, and INTB are redefined for test purposes when SILVERB is low.

5. The VSSO, VSSI, TAVS, and RAVS ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the DDSX.

6. The VDDO, VDDI, TAVD, and RAVD power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the DDSX.

7. The drive capability of DDSX T1 line driver outputs is 70 ma.

FUNCTIONAL DESCRIPTION

Receive Data Slicer

The Receive Data Slicer (RSLC) Block provides the first stage of signal conditioning for a DSX-1 serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the RSLC Block, bipolar input signals must rise to 67% of their peak amplitude. This level is the Slicing Level. This threshold criteria insures accurate pulse or mark recognition in the presence of noise.

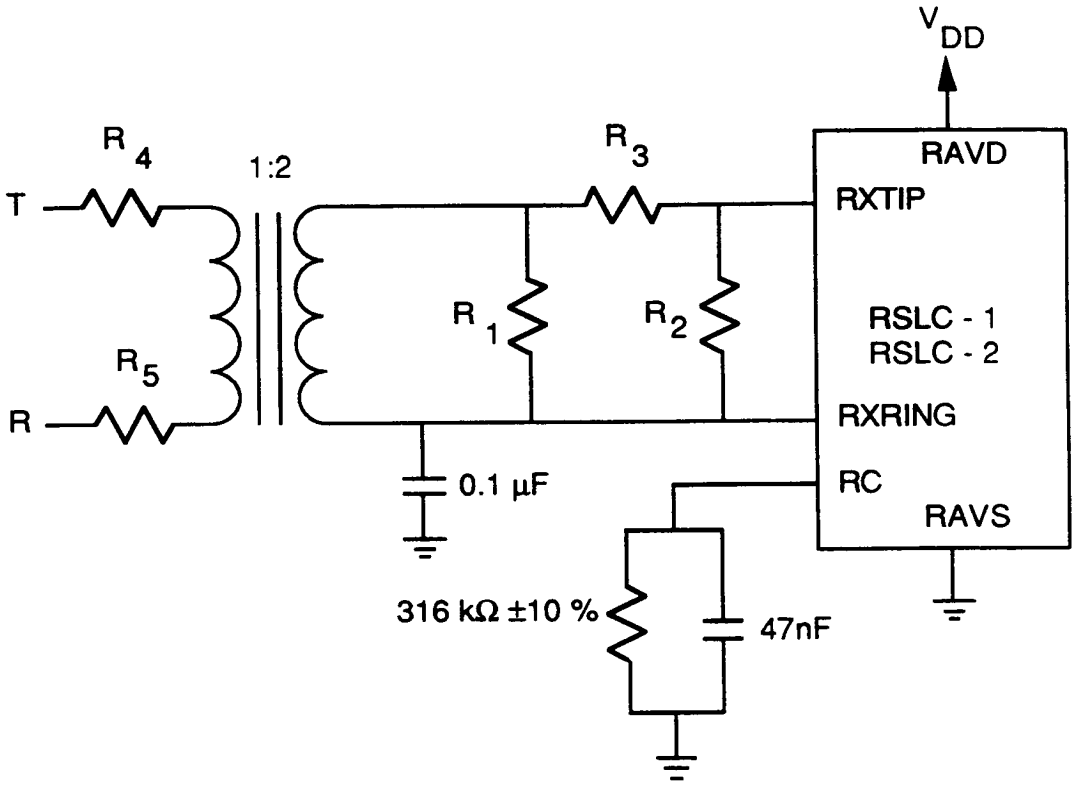
The RSLC Block is configured via an off-chip attenuator pad (see Fig. 1) to operate in one of two modes: normal mode or performance monitor mode. In normal mode, the amplitude of a received pulse at the line-coupling transformer's primary can be in the range from 3.6 V to 0.5 V, depending on the DDSX's distance from the DSX-1 cross-connect. In performance monitor mode, the DDSX is bridged across the line and the expected signal levels are 20 dB lower than standard DSX-1 levels. In each mode the sensitivity below minimum DSX-1 levels is -10 dB. The sensitivity of the receiver is defined as the difference between the worst case DSX-1 signal amplitude (2.4 V) and the squelching level.

The RSLC Block has two signal level alarms that are operational in both normal and performance monitor modes. The first alarm is the low signal level alarm. This alarm occurs when input pulses at the primary of the line-coupling transformer are below the low level threshold but above the squelching level threshold. During a low level alarm, the RSLC Block continues to operate and the LV status bit goes high. The low level signal threshold is 1.5 V for normal mode, and 150 mV for performance monitor mode. The RSLC Block can be configured to generate an interrupt when the LV status bit goes high.

The second alarm occurs when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. For the normal mode of operation, the squelching threshold is 0.5 V; for performance monitor mode, the squelching threshold is 50 mV. The SQ status bit goes high whenever the RSLC Block is squelching. The block can be configured to generate an interrupt whenever the SQ status bit goes high.

The RSLC Block meets the requirements for receiving a DSX-1 compatible signal as defined in ANSI T1.102 and the other cited references.

Fig. 1 External Analog Receive Interface Circuit



Normal Mode

R_1 = 412 Ω ± 1%
R_2 = 1.1 kΩ ± 1%
R_3 = 9.0 kΩ ± 1%
R_4 = R_5 = Closed Circuit

(All capacitors ceramic)

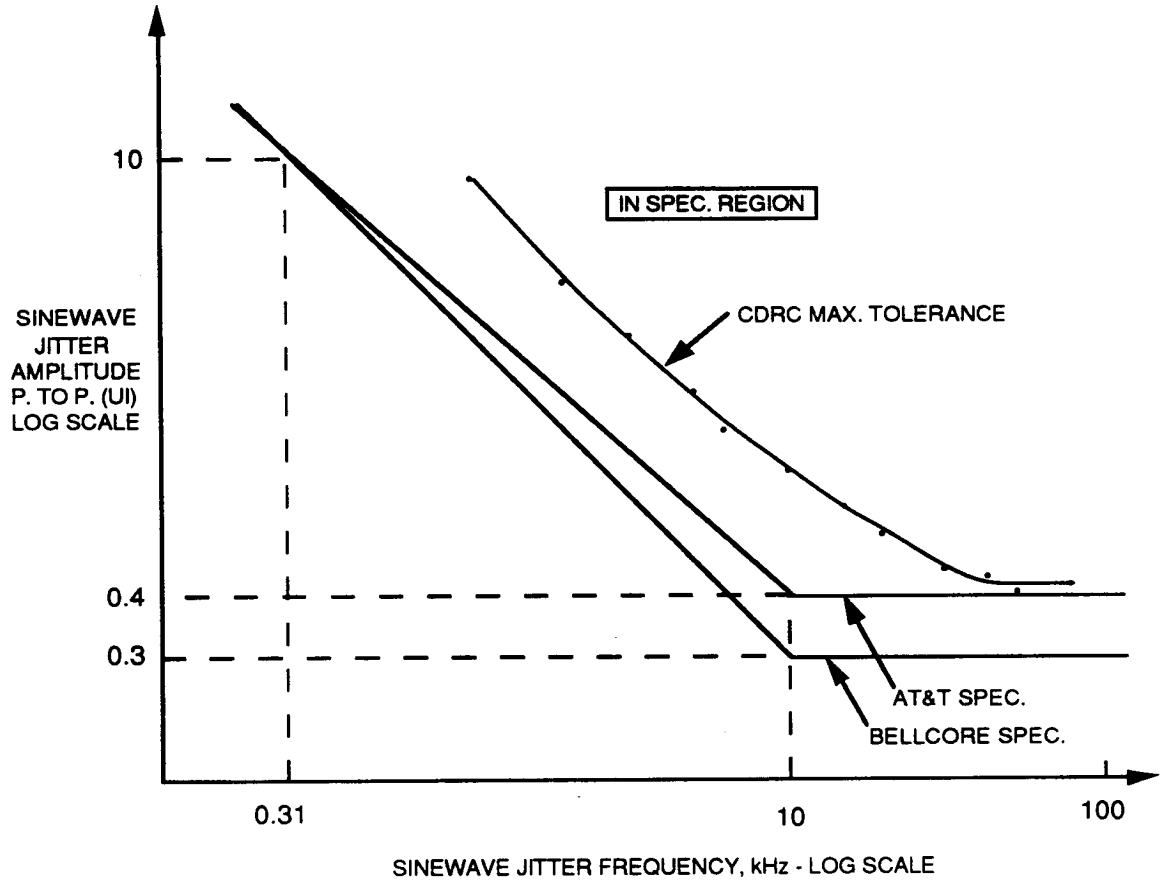
Clock & Data Recovery

The Clock and Data Recovery (CDRC) Block provides clock and PCM data recovery, B8ZS decoding, bipolar violation detection, and loss of signal detection. The CDRC Block recovers the clock from the incoming RZ data pulses using a digital phase-locked loop and recovers the NRZ data. Loss of signal is indicated after 176 consecutive bit periods of absence of pulses on both the positive and negative pulse inputs. Loss of Signal is cleared after the occurrence of a single line pulse. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and again when the signal returns.

Jitter Tolerance

The CDRC Block provides excellent high frequency jitter tolerance. It can accomodate up to 0.4 UIpp of jitter at jitter frequencies above 10 kHz. For jitter frequencies below 10 kHz, jitter tolerance increases 20 dB per decade reaching 10 UIpp at 700 Hz. In most applications the CDRC Block will limit jitter tolerance at higher jitter frequencies only. For low frequency jitter, below 10 kHz for example, other factors such as jitter attenuator buffer depth and transfer characteristics or slip buffer hysteresis may limit jitter tolerance and must be considered. The CDRC Block meets the stringent high frequency jitter tolerance requirements of AT&T TR 62411 and Bellcore TR-TSY-000170 and thus allows one to comply with these standards and the other less stringent jitter tolerance standards cited in the references.

Fig. 2 CDRC Jitter Tolerance



Inband Code Detector

The Inband Code Detector (IBCD) Block detects the presence of either of two programmable inband loopback activate and deactivate code sequences in either

framed or unframed received data streams. The code must be present continuously for at least 5.06Sec. ± 39.8msec. for detection. IBCD operates in the presence of 10^{-2} bit error rate. Inband loopback codes are specified in ANSI T1.403, Bellcore TR-TSY-000312, and TR-TSY-000303.

Line Code Violation Counter

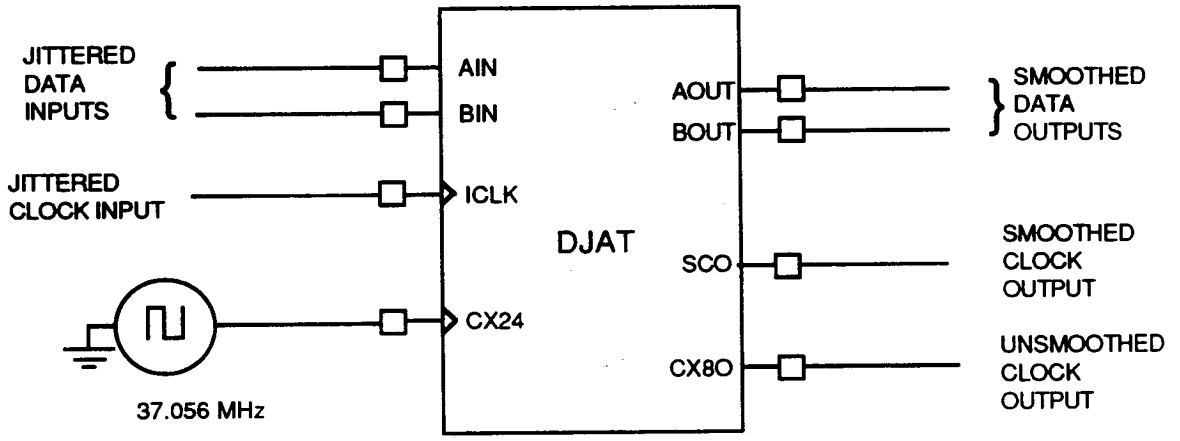
The Line Code Violation Counter block (PMON) accumulates the number of line code violations (LCVs) occurring in the incoming PCM stream during one accumulation interval. The counter is 12 bits long and can accumulate up to 4095 LCVs before saturating. This length provides a less than 0.001% probability of the counter saturating at a 10^{-3} bit error rate (BER) if the accumulation period is one second.

The PMON block contains a counter and a holding register. The current counter value is transferred to the holding register when triggered by a write access to the holding register via the microprocessor interface. Simultaneously, the counter is cleared in such a way that prevents an LCV event occurring during the clearing from being missed. The period between successive writes to the holding register defines the accumulation interval.

Digital Jitter Attenuator

The Digital Jitter Attenuator (DJAT) Block receives jittered T1 data in NRZ format at the positive and negative pulse inputs. The incoming data streams are stored in the FIFO registers on the rising edge of the input clock (ICLK). The positive and negative input data emerges jitter-attenuated from the FIFO on the falling edge of SCO.

Fig. 3 DJAT Configuration



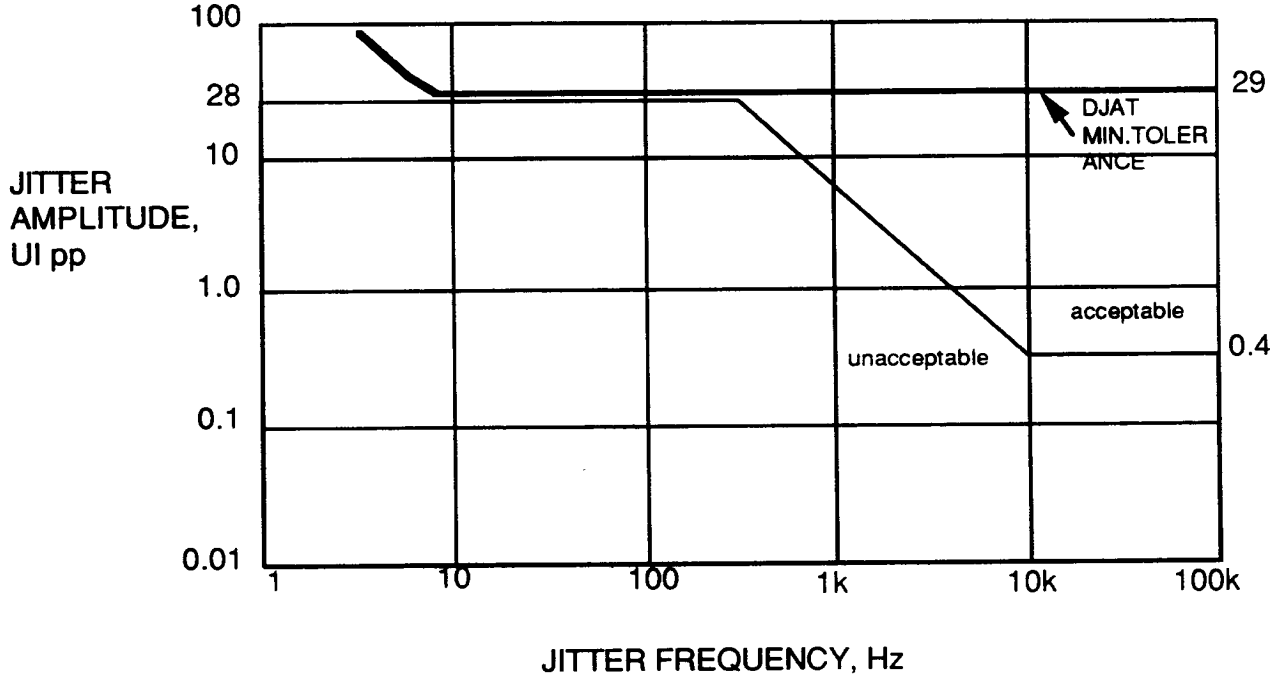
The jitter attenuator generates the 1.544 MHz SCO output by adaptively dividing the 37.056 MHz CX24 system clock according to the phase difference between SCO and ICLK. Jittered fluctuations in the phase of ICLK are attenuated by the phase-locked loop in DJAT so that the frequency of SCO is equal to the average frequency of ICLK. To best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 6.6 Hz are tracked by SCO. To provide a smooth flow of output data, SCO is used to shift data out of the FIFO.

Should the FIFO read pointer in DJAT come within one bit of the write pointer, DJAT will track the jitter of ICLK. Permitting the phase jitter to pass through unattenuated in this condition will inhibit the loss of data.

Jitter Tolerance

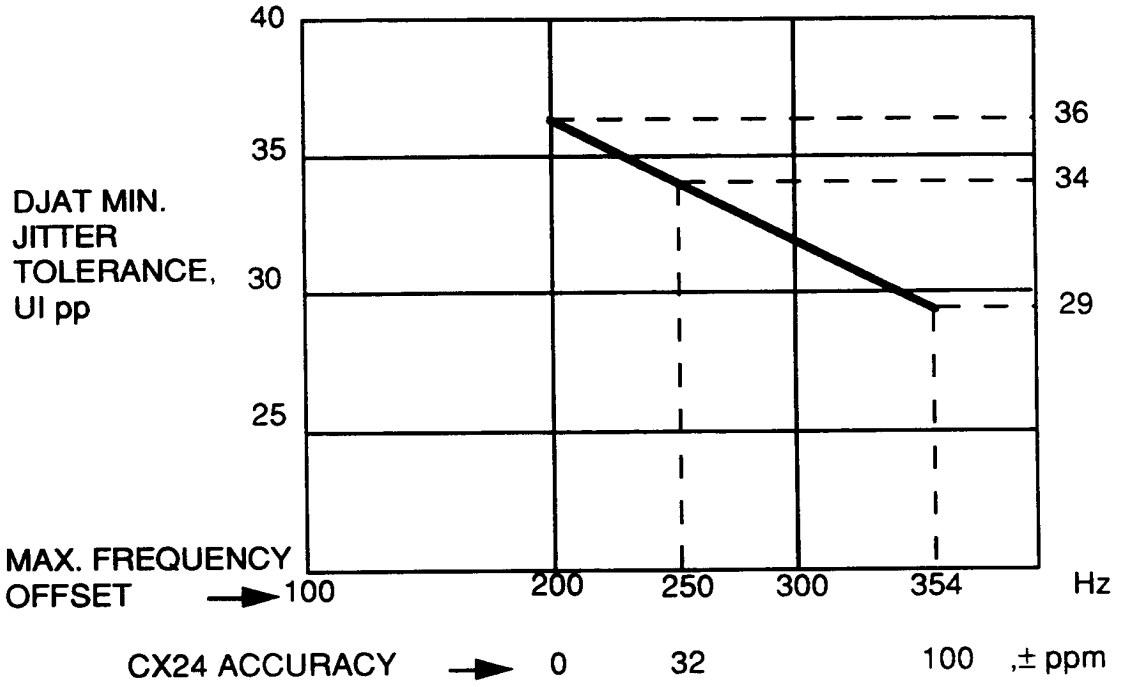
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of CX24 divided by 24 (CX24/24) and that of the ICLK clock input.

Fig. 4 DJAT Jitter Tolerance



The accuracy of the system clock frequency and that of the DJAT.REF input have an effect on the minimum jitter tolerance. Given that the frequency of DJAT.REF can be ±200 Hz from 1.544 MHz, figure 5 is a plot of minimum jitter tolerance for various differences between the frequency of DJAT.REF and DJAT.CX24/24.

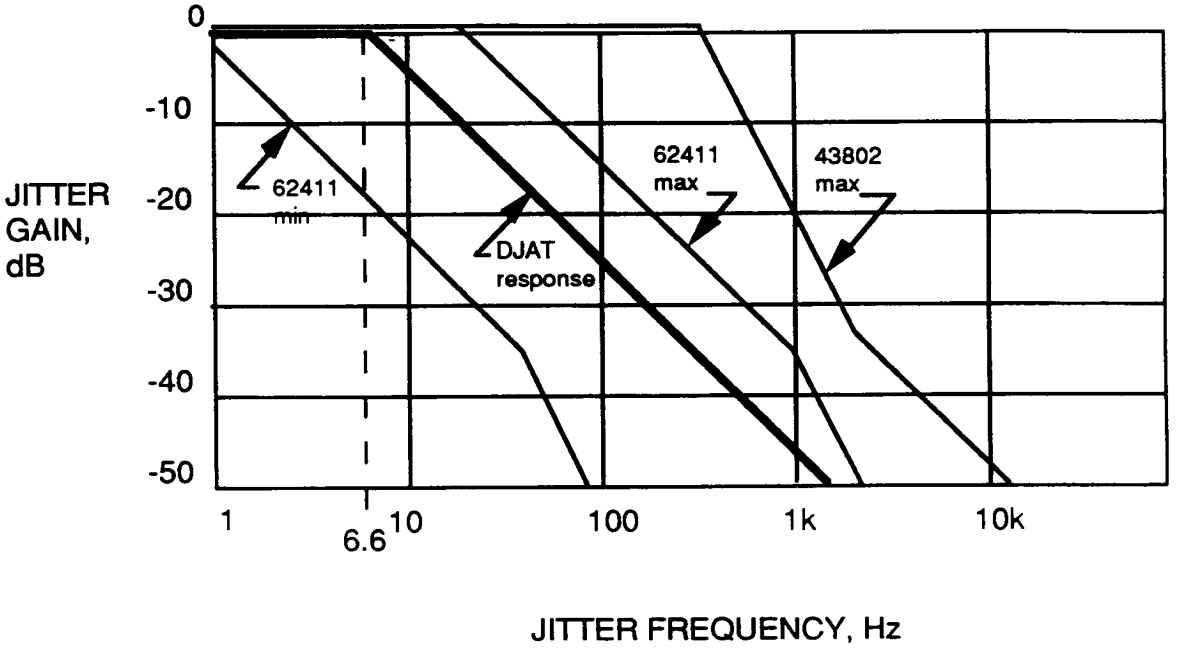
Fig. 5 DJAT Minimum Jitter Tolerance vs. CX24 Accuracy



Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz will be no more than 0.1 dB greater than the input jitter, excluding the 0.042 UI residual jitter. Jitter frequencies above 6.6 Hz are attenuated at a level of 6 dB per octave.

Fig. 6 DJAT Jitter Transfer



Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (29 UIpp) and maximum system clock frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or system clock frequency offset.

Jitter Characteristics

The DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accomodate up to 28 UIpp of jitter at jitter frequencies above 6 Hz. For jitter frequencies below 6 Hz, more correctly called wander, tolerance increases 20 dB per decade. In most applications the DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT Block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows one to comply with this standard and the other less stringent jitter tolerance standards cited in the references.

The DJAT Block exibits negligible jitter gain for jitter frequencies below 6.6 Hz, and attenuates jitter at frequencies above 6.6 Hz by 20 dB per decade. In most applications the DJAT Block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter will be dominated by the generated residual jitter of 0.042 UIpp in cases where incoming jitter is insignicant. This generated residual jitter is directly related to the use of 24X (37.056 MHz) digital phase locked loop for transmit clock generation. The frequency of this generated residual jitter will be below 8 kHz. The DJAT Block meets the jitter attenuation requirements of AT&T TR 62411 and also meets the requirements of AT&T PUB 43802. The DJAT Block allows one to meet the implied jitter attenuation requirements for a TE or NT1 given in ANSI Draft Standard T1E1.2/88-079R8, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403.

Inband Code Transmitter

The Inband Code Transmitter (XIBC) Block generates inband loopback code sequences for insertion into the PCM data stream. These codes consist of continuous repetitions of specific bit sequences. Inband loopback codes are specified in ANSI T1.403, Bellcore TR-TSY-000312, and TR-TSY-000303.

The XIBC supports repetitive transmission of any arbitrary code from three to eight bits in length on the inband code output by programming a control register to set the sequence length and transmit enable output. This programming is done over the Common Bus Interface by an external controller.

Transmit Pulse Generator

The Transmit Pulse Generator (XPLS) Block converts Non-Return-to-Zero (NRZ) pulses into Alternate Mark Inversion (AMI) line signals suitable for use in the DSX-1 intra-office environment. The dual-rail NRZ pulses are supplied by the DJAT Block. A logic 1 at the Transmit Positive input causes a positive pulse to be transmitted; a similar pulse at the Transmit Negative input causes a negative pulse to be transmitted. If both inputs are logic 0 or 1, no output pulse is transmitted.

The output pulse shape is synthesized digitally with an internal Digital-to-Analog (D/A) converter. The converter is updated at 8 x T1 rate with data stored in a ROM. These words define the output pulse shape. Eight SCLK periods constitute a single output pulse.

AMI signalling is created by exciting either the internal Tip or Ring drivers that drive a line-coupling transformer differentially. This differential driving scheme insures a small positive to negative pulse imbalance. The drivers and the step-up transformer amplify the output pulses to their final levels. The Tip and Ring drivers also supply the high current capability required to drive the low impedance output load.

The cable length used in the link between the XPLS and the DSX-1 cross-connect greatly affects the resulting pulse shapes. This is compensated for by selecting from one of eight different pulse output shapes built into XPLS. Setting the SM bit in the XPLS Configuration Register selects between the LS bus or ILS bits.

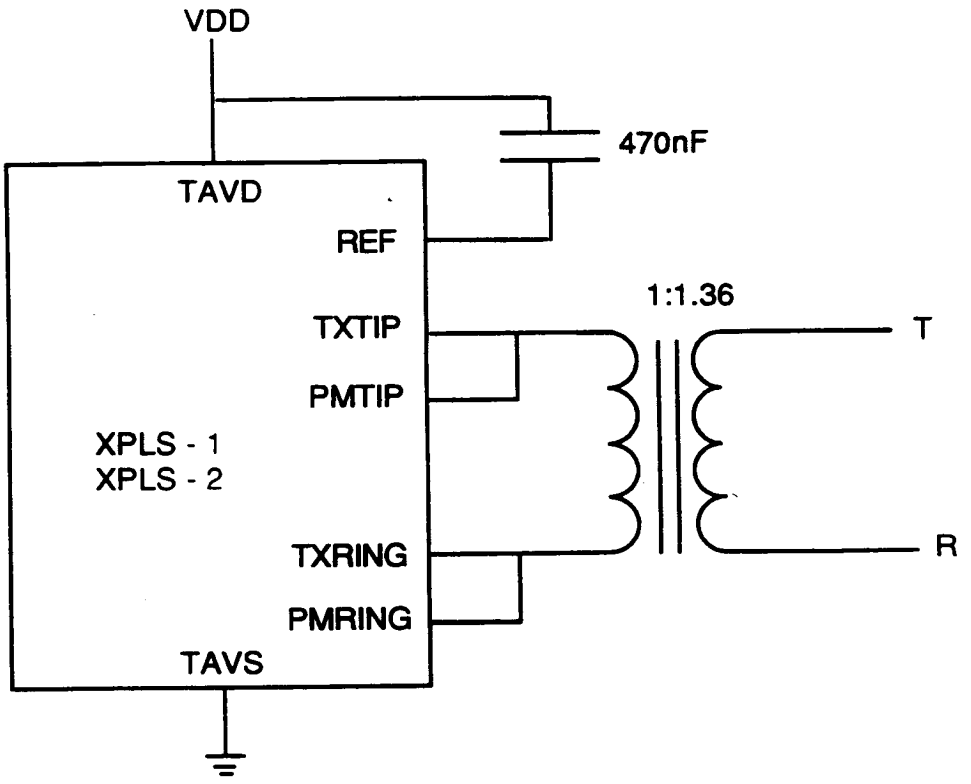
The XPLS includes a driver performance monitor to detect nonfunctional links. Two inputs, PMTIP and PMRING, can be connected to either the XPLS's own outputs or an adjacent link's outputs. If no pulses are detected alternately across inputs PMTIP or PMRING for 63 consecutive TCLK periods, the monitored link is considered failed, until the first correct pulse is received on the monitor inputs.

The XPLS provides outputs that are sliced versions of the analog signal presented to the performance monitor input pins. The DDSX can be programmed to loopback its own analog outputs by writing to the loopback control register, and by connecting PMTIP and PMRING to outputs TXTIP and TXRING, respectively. The PMTIP and PMRING inputs have a nominal slicing level of 2.3 Volts.

The XPLS Block provides Alarm Indication Signalling (AIS) generation capability. XPLS generates alternating mark signals on the link when the TAIS pin is held high, or when programmed via the Common Bus Interface.

The XPLS Block meets the requirements for transmitting a DSX-1 compatible signal as defined in ANSI T1.102 and the other cited references.

Fig. 7 External Analog Transmit Interface Circuit



Clock Generator

Fig. 8 Typical External Crystal Oscillator Circuit

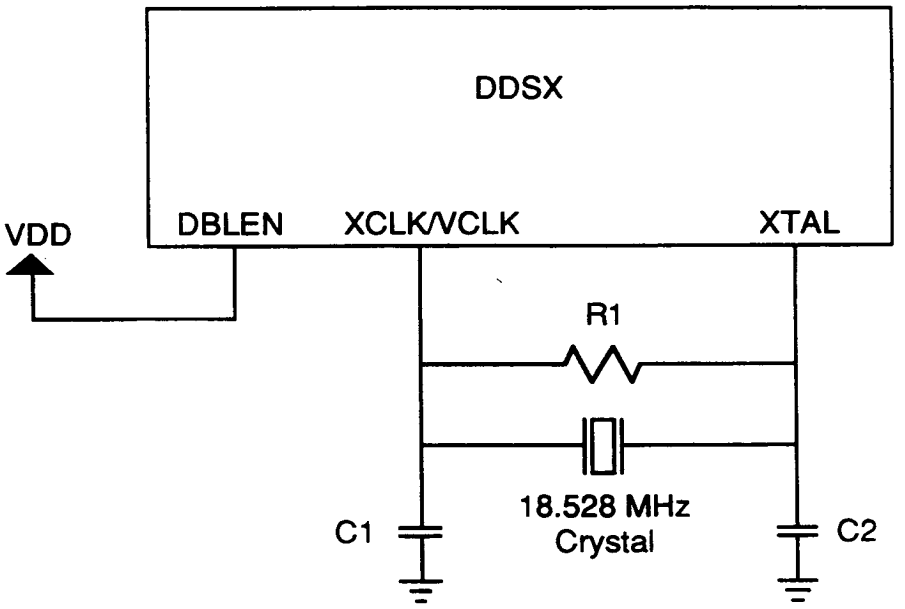


Figure 7 shows a typical circuit using an external 18.528 MHz crystal for timing generation. Typically, R1 has a value of 1 MΩ or greater. The values of the two capacitors are dependent upon the specified load capacitance of the crystal. Typically, C1 and C2 each have a value of 10 pF. Both transceivers in DDSX share the same timing source. Alternatively, the DDSX may be driven by a 37.056 MHz clock source connected to XCLK/VCLK. XTAL should be left unconnected, and the internal frequency doubler should be disabled by connecting pin DBLEN to ground.

Alarms and Diagnostics

The Alarms and Diagnostics Block controls the propagation of interrupts generated by the other blocks in the DDSX to the INTB pin. Interrupts can be masked and their current state can be read via accesses through the microprocessor interface.

The three loopback modes in the DDSX are controlled by the Alarm and Diagnostics Block. In the first mode, received data, after clock and data recovery, is retransmitted with jitter attenuated. The two remaining modes loop transmit data back towards the receive side. The loopback data is taken from the output of DJAT in mode two, and from the performance monitor outputs of XPLS in mode three.

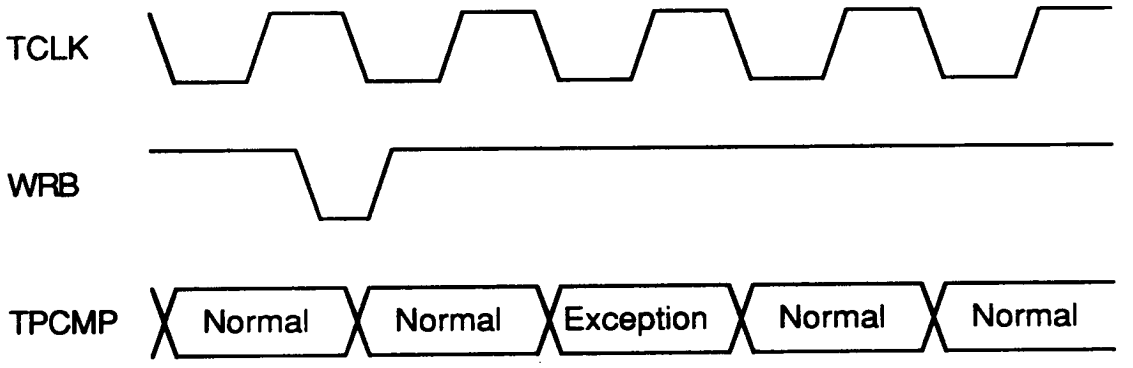
When the DDSX transmitter is in single rail mode, setting the TPCMN/TEXP pin causes a transmission exception. The effect of the exception is controlled by the TBE and TRP bits in the Transmit Control Register. If TBE is set to logic 1, a bit error is generated. If the current bit is a mark, and TRP is set to logic 1, the bit is

transmitted with reversed polarity. If the bit is a space, the next available mark bit is transmitted with reversed polarity. If both bits are set to logic 1, TRE is applied first, followed by TBV. The table below shows the effects of the TBE and TRP bits for TPCMP being mark and space.

TPCMP	TRP	TBE	Effects
Space	0	0	Bit unchanged
Space	0	1	Current bit changed to mark
Space	1	0	Next mark bit transmitted with reversed polarity
Space	1	1	Current bit changed to mark and transmitted with reversed polarity
Mark	0	0	Bit unchanged
Mark	0	1	Current bit changed to space
Mark	1	0	Current bit transmitted with reversed polarity
Mark	1	1	Current bit changed to space Next Mark bit transmitted with reversed polarity

A transmission exception can be triggered in software by setting the TEXP bit in the Transmit Control Register. For each access, the DDSX behaves as though the TEXP pin is set to logic 1 for the bit period after next (See fig. 9). In B8ZS mode, a transmit exception with TRP set will reverse the polarity of one of the pulses in the B8ZS signature.

Fig. 9 Software Induced TEXP Timing



Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the DDSX to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and

monitor the DDSX while the test mode registers are used to enhance the testability of the DDSX.

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the DDSX. Normal mode registers (as opposed to test mode registers) are selected when TRSB (CBI[13]) is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TSB to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect TSB operation unless otherwise noted.

Register Map

DSX-1	DSX-2	REGISTER DESCRIPTION
00H	20H	MASTER CONFIGURATION
01H	21H	MASTER INTERRUPT ENABLE
02H	22H	MASTER INTERRUPT STATUS
03H	23H	MASTER RESET AND IDENTITY
04H	24H	TRANSMIT CONTROL
05H	25H	Reserved for test
06H	26H	LINE CODE VIOLATION COUNT (LSB)
07H	27H	LINE CODE VIOLATION COUNT (MSB)
08H	28H	CDRC CONFIGURATION
09H	29H	CDRC INTERRUPT ENABLE/STATUS
0AH	2AH	CDRC STATUS
0BH	2BH	Reserved for test
0CH	2CH	DJAT INTERRUPT STATUS
0DH	2DH	DJAT REFERENCE CLOCK DIVISOR (N1)
0EH	2EH	DJAT OUTPUT CLOCK DIVISOR (N2)
0FH	2FH	DJAT CONFIGURATION
10H	30H	IBCD CONFIGURATION
11H	31H	IBCD INTERRUPT ENABLE/STATUS
12H	32H	IBCD ACTIVATE CODE
13H	33H	IBCD DEACTIVATE CODE
14H	34H	Reserved for test
15H	35H	Reserved for test
16H	36H	Reserved for test
17H	37H	RSLC INTERRUPT ENABLE/STATUS
18H	38H	XIBC CONFIGURATION
19H	39H	XIBC INBAND CODE
1AH-1BH	3AH-3BH	Reserved for test
1CH	3CH	XPLS CONFIGURATION
1DH	3DH	XPLS CONTROL, INTERRUPT ENABLE/STATUS
1EH-1FH	3EH-3FH	Reserved for test

Note: All register bits are cleared to zero upon activation of DDSX reset unless otherwise noted. Reading and writing to reserved registers may produce unexpected results.

DDSX Internal Registers

Register 00H, 20H: Master Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	RRZ
Bit 4	R/W	RDUAL
Bit 3	R/W	TXLBEN
Bit 2	R/W	SELPM
Bit 1	R/W	RXLBEN
Bit 0	R/W	IBCLBEN

Each master configuration register allows software to configure the associated DSX-1 line interface in the DDSX. Register 00H controls interface SX-1 and register 20H controls SX-2.

The IBCLBEN bit allows loopback from the receiver to the transmitter to be controllable by inband loopback codes on the receive data stream. If IBCLBEN is set to logic 1 and the IBCD Block detects an inband loopback activate command, the output of CDRC is directed to the input of DJAT. The receive data is looped back and returned on the transmit data stream. Loopback is deactivated when the IBCD block detects a deactivate command or when IBCLBEN is negated.

When set to logic 1, the RXLBEN bit forces the received data stream to be looped back on the transmit stream. CDRC outputs RPCMP, RPCMN and RCLK are connected to DJAT. In this mode, all bipolar violations received by the receiver are replicated by the transmitter, including those forming B8ZS signatures.

The transmit data stream can be looped back to the receiver by setting the TXLBEN bit to logic 1. The source of loopback data is selectable by the SELPM bit. If SELPM is set to logic 1, CDRC takes its inputs from the sliced outputs of the performance monitor in XPLS. If SELPM is negated, CDRC is connected to DJAT.

The receive portion of each line interface can be placed in dual rail mode by setting the RDUAL bit to logic 1. The RPCMP and RPCMN pins carry the recovered positive and negative PCM pulse, respectively. A single rail interface can be selected by

negating RDUAL. In this state, RPCMP carries DS-1 data that is selectable between AMI and B8ZS decoding, and RPCMN carries data assuming AMI decoding only.

When the DDSX receiver is in dual rail mode (RDUAL set to logic 1) the RRZ bit forces the RPCMP and RPCMN outputs to be return-to-zero signals. The outputs are gated with RCLK so that they are active only when RCLK is logic 1. The RRZ bit has no effect when RDUAL is negated.

Register 01H, 21H:
Master Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	XPLSE
Bit 3	R/W	RSLCE
Bit 2	R/W	IBCDE
Bit 1	R/W	DJATE
Bit 0	R/W	CDRCE

This register provides an interrupt enable bit for each of the blocks comprising one line interface in the DDSX. Interrupts may still be masked at the source block level. Interrupts enabled at the block level but masked by this register are reported in the Master Interrupt Status Register. Interrupts disabled at the block level are not reported by the Master Interrupt Status Register.

Register 02H, 22H: Master Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	XPLSI
Bit 3	R	RSLCI
Bit 2	R	IBCDI
Bit 1	R	DJATI
Bit 0	R	CDRCI

This register identifies the block that is the source of a pending interrupt. After identifying the block generating the interrupt, it may be necessary to read the interrupt status register of that block to determine the actual event that generated the interrupt. This register is provided as a convenience to the user since the source block of an interrupt can be determined by polling the interrupt status registers of every block in the DDSX. Unlike the interrupt status registers associated with each block, this register only reports interrupt sources capable of generating a hardware interrupt. That is, interrupts masked at the block interrupt enable register level are not reported by this register.

Register 03H, 23H: Master Reset and Identity

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	ID[6]
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

This register allows software to asynchronously reset the associated line interface (address 03H for DSX-1 and address 23H for DSX-2) in the DDSX package. The software reset is equivalent to setting the RSTB input pin to low, except that only one line interface is affected. Setting the RESET bit to logic 1 causes the associated DSX to be reset; clearing the RESET bit to logic 0 disables the reset mode. In reset mode, all bits in all DSX registers are reset, except for the RESET bit itself. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register. The DDSX RSTB pin resets both line interfaces in the DDSX package and clears the RESET bit in this register to logic 0, disabling the software reset mode.

The version identification bits, ID[6:0], are set to a fixed value representing the version number of the DDSX. The identification bits can be used to determine the DDSX version via software. The identification bits of both line interfaces are identical.

Register 04H, 24H:
Transmit Control

Bit	Type	Function
Bit 7	R/W	TCT
Bit 6	R/W	TFBT
Bit 5	R/W	TSF
Bit 4	R/W	TRP
Bit 3	R/W	TBE
Bit 2	W	TEXP
Bit 1	R/W	TAMI
Bit 0	R/W	TDUAL

This register enables software to configure the transmit portion of the line interfaces in the DDSX. When set to logic 1, the TDUAL bit configures the transmitter to expect dual rail data on the TPCMP and TPCMN pins. Polarity coding for AMI, B8ZS, etc. rests with upstream circuitry. When TDUAL is set to logic 0, the DDSX expects single rail DS-1 signals on TPCMP. The output at pins TXTIP and TXRING will be AMI encoded if the TAMI bit is set to logic 1 and B8ZS (bipolar 8 zero substitution) encoded if TAMI is set to logic 0.

The TSF bit controls the sampling of transmit data TPCMP and TPCMN. When TSF is asserted (HI), transmit data inputs are sampled on the falling edge of TCLK. Otherwise, the data is sampled on the rising edge of TCLK.

The TPCMN pin can be used to effect transmission exceptions when TDUAL is set to logic 0, and TFBT and TCT are set to logic 0. The bits TBE and TRP control the nature of the exception. If TBE is set to logic 1, the logic of the signal on TPCMP is negated. If TRP is asserted, the first available mark pulse will be transmitted with the opposite polarity. The mark pulse may have as its source a logic 1 bit on TPCMP or a part of the B8ZS pattern. Software can cause a transmission exception by writing a logic 1 to the TEXP bit. The effect is identical to that of sending a single logic 1 pulse on TPCMN. The behaviour of the DDSX under various combinations of TPCMP, TBE and TRP is listed in the table in the section on alarms and diagnostics.

The TFBT bit enables framing bit transparency when the DDSX expects single rail DS-1 signals on TPCMP, i.e. when TDUAL and TCT are set to logic 0. The EN and IF bits in the XIBC configuration register must also be set to logic one to enable framing bit transparency. When TFBT, EN, and IF bits are set to logic 1, then a logic 1 pulse on TPCMN will inhibit the overwriting of the bit received on TPCMP when transmitting an inband loopback code. This mode is provided so that the framing bits generated by an upstream transmitter are not overwritten when transmitting an inband loopback code, thus creating a framed inband loopback code where the inband code is effectively overwritten by the framing bit. For proper operation, a logic 1 pulse must be provided on TPCMN every 193 bit periods, marking the framing bit position on TPCMP. When TFBT, EN, and IF bits are set to logic 1 transmit exceptions can only be activated by writing a logic 1 to the TEXP bit .

The TCT bit enables transmitter cut-through mode where the positive and negative pulses recovered by the receiver on the opposite side of the DDSX are transmitted by the enabled side of the DDSX. In this mode, all bipolar violations received by the receiver are replicated by the transmitter, including those forming B8ZS signatures. When TCT is set to logic 1, the TPCMP and TPCMN inputs are ignored. Note that the transmitter cut through function overrides all other transmit control functions programmed in this register. This mode intended to allow application of the DDSX as a duplex jitter attenuating repeater while the receive sections of each half of the DDSX are configured for single rail operation, thus allowing external DS1 framers to be attached for path performance monitoring purposes.

Register 06H, 26H:
Line Code Violation Count (LSB)

Bit	Type	Function
Bit 7	R	LCV[7]
Bit 6	R	LCV[6]
Bit 5	R	LCV[5]
Bit 4	R	LCV[4]
Bit 3	R	LCV[3]
Bit 2	R	LCV[2]
Bit 1	R	LCV[1]
Bit 0	R	LCV[0]

Register 07H, 27H:
Line Code Violation Count (MSB)

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	LCV[11]
Bit 2	R	LCV[10]
Bit 1	R	LCV[9]
Bit 0	R	LCV[8]

Registers 6 and 7 are the holding registers for the line code violation counter. They indicate the number of line code violations occurring in the previous accumulation period, which are delineated by writes to either of the two registers. The less significant byte of the count resides in register 6, and the more significant byte in register 7. Writing to either of the two registers transfers the current LCV count to the holding registers. The counter is then cleared such that a line code violation occurring contemporaneously with the write is not lost.

CDRC Registers

Register 08H, 28H: CDRC Configuration

Bit	Type	Function
Bit 7	R/W	AMI
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

The AMI bit selects the line code of the incoming DS1 line. A logic 1 selects AMI (alternate mark inversion) line code; a logic 0 selects B8ZS line code.

Register 09H, 29H: CDRC Interrupt Enable/Status

Bit	Type	Function
Bit 7	R/W	BPVE
Bit 6	R/W	LOSE
Bit 5	R/W	B8ZSE
Bit 4	R/W	Z8DE
Bit 3	R	BPVI
Bit 2	R	LOSI
Bit 1	R	B8ZSI
Bit 0	R	Z8DI

The bit positions BPVE, LOSE, B8ZSE and Z8DE (bits 7 to 4) of this register select which of the status events (bipolar line code violation, loss of signal, B8ZS signature or 8 zeros, respectively), either singly or in combination, will generate an interrupt when it is detected. A logic 1 bit in a bit position enables the detection of the corresponding signal to generate an interrupt; a logic 0 bit in a bit position disables the corresponding signal from generating an interrupt. Status events, line code violations, B8ZS signature detection and 8 zeros detection all generate an interrupt

only on a rising edge of the signal (that is only when the event is detected). The loss of signal event generates an interrupt whenever the LOS output changes state. When the DDSX is reset, BPVE, LOSE, B8ZSE and Z8DE are all reset to logic 0; therefore, interrupt generation is disabled.

The bit positions BPVI, LOSI, B8ZSI and Z8DI (bits 3 to 0) of this register indicate which of the status events generated an interrupt. A logic 1 in a bit position indicates that the corresponding event was detected and generated an interrupt; a logic 0 in a bit position indicates that no corresponding event was detected. The bit positions BPVI, B8ZSI and Z8DI are set on the rising edge of the corresponding output signal (i.e., upon declaration of the event). LOSI is set on any state transition of the LOS output. Bits BPVI, LOSI, B8ZSI and Z8DI are cleared to logic 0 by reading this register. Regardless of whether interrupts are enabled or disabled, the BPVI, LOSI, B8ZSI and Z8DI bits retain their event capture function.

Register 0AH, 2AH:
CDRC Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R	RLOS

The current state of the RLOS output is reported in bit 0 of this register.

DJAT Registers

Register 0CH, 2CH: DJAT Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	OVRR
Bit 0	R	UNDR

The OVRR and UNDR bits reflect the status of the FIFO in DJAT. When OVRR is set to logic 1, an overrun has occurred. When UNDR is set to logic 1, an underrun has occurred. Reading this register will reset the bits to logic 0 and clear the interrupt flag, which is caused by either of the OVRR or UNDR bits changing from logic 0 to logic 1.

Register 0DH, 2DH: DJAT Reference Clock Divisor (N1)

Bit	Type	Function
Bit 7	R/W	N1[7]
Bit 6	R/W	N1[6]
Bit 5	R/W	N1[5]
Bit 4	R/W	N1[4]
Bit 3	R/W	N1[3]
Bit 2	R/W	N1[2]
Bit 1	R/W	N1[1]
Bit 0	R/W	N1[0]

This is the reference clock divisor register used in DJAT. The reference clock frequency is divided by (N1+1) is to be at the same frequency as the output clock divided by (N2+1), for phase comparison purposes. Upon hardware or software reset, the register defaults to decimal 47, such that (N1+1) equals the depth of the

FIFO in DJAT. Writing to this register is unnecessary in normal operation and will cause a reset of the PLL and FIFO in the DJAT Block.

Register 0EH, 2EH:
DJAT Output Clock Divisor (N2)

Bit	Type	Function
Bit 7	R/W	N2[7]
Bit 6	R/W	N2[6]
Bit 5	R/W	N2[5]
Bit 4	R/W	N2[4]
Bit 3	R/W	N2[3]
Bit 2	R/W	N2[2]
Bit 1	R/W	N2[1]
Bit 0	R/W	N2[0]

This is the output clock divisor register used in DJAT. It divides the output clock frequency to a common subrate as the reference clock for phase discrimination purposes. It is reset to decimal 47 by both the hardware and software resets. Writing to this register is unnecessary in normal operation and will cause a reset of the PLL and FIFO in the DJAT Block.

Register 0FH, 2FH:
DJAT Configuration Register

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	CENT
Bit 3	R/W	UNDE
Bit 2	R/W	OVRE
Bit 1	R/W	SYNC
Bit 0	R/W	LIMIT

This register configures the DJAT Block. The bits UNDE and OVRE control the enabling of underrun and overrun interrupts, respectively. The associated interrupt is disabled when the bit is set to logic 0. The remaining bits: CENT, SYNC, and

LIMIT, configure the DJAT Block for various applications. In the DDSX, CENT should be logic 0, and SYNC and LIMIT should both be logic 1. These are the default values after reset.

IBCD Registers

Register 10H, 30H: IBCD Configuration

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R/W	DSEL[1]
Bit 2	R/W	DSEL[0]
Bit 1	R/W	ASEL[1]
Bit 0	R/W	ASEL[0]

The Configuration Register allows for the selection of a loopback code length from three bits to eight bits long as follows:

MODE	DEACTIVATE		ACTIVATE	
CODE LENGTH	DSEL[1]	DSEL[0]	ASEL[1]	ASEL[0]
5 BITS	0	0	0	0
6(or 3*) BITS	0	1	0	1
7 BITS	1	0	1	0
8(or 4*) BITS	1	1	1	1

*Note: Three and four bit code sequences can be accommodated by configuring the IBCD for length of six or eight bits and by programming the code register with two repeating three or four bit patterns.

The ACCEL bit is used to enable the accelerated timing for production test purposes. For proper operation, the ACCEL bit must be set to logic 0.

Register 11H, 31H: IBCD Interrupt Enable and Status

Bit	Type	Function
Bit 7	R	LBACP
Bit 6	R	LBDCP
Bit 5	R/W	LBAE
Bit 4	R/W	LBDE
Bit 3	R	LBAI
Bit 2	R	LBDI
Bit 1	R	LBAS
Bit 0	R	LBDS

The enable bit positions (LBAE and LBDE) of this register are interrupt enable bits to select which of the inband loopback activate (LBA) or inband loopback deactivate (LBD) signals, either singly or in combination, are enabled to generate an interrupt when their state changes. A logic 1 in the LBAE or LBDE bit position enables any state change on the corresponding output to generate an interrupt; a logic 0 in the corresponding mask position disables that signal from generating an interrupt. When the TSB is reset, LBAE and LBDE are set to logic 0, disabling any interrupt generation.

The interrupt status bit positions (LBAI and LBDI) of this register indicate which of the two loopback outputs generated an interrupt when their state changed. A logic 1 in either of these bit positions indicates that a state change has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred. After the Enable/Status Register has been read, the LBAI and LBDI bits are set to logic 0 along with the interrupt output.

The current status bit positions (LBAS and LBDS) indicate the current state of the respective loopback code outputs.

The code present bit positions (LBACP and LBDCP) indicate when the respective loopback code is present. These status indications are updated at 39.8 ms intervals.

Register 12H, 32H: IBCD Activate Code

Bit	Type	Function
Bit 7	R/W	ACT[7]
Bit 6	R/W	ACT[6]
Bit 5	R/W	ACT[5]
Bit 4	R/W	ACT[4]
Bit 3	R/W	ACT[3]
Bit 2	R/W	ACT[2]
Bit 1	R/W	ACT[1]
Bit 0	R/W	ACT[0]

This 8-bit register allows selection of the activate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill this register. For example, if the code sequence is '00001', the first 8 bits of '0000100001...' are '00001000'). Note that bit 7 is the first code bit received.

Register 13H, 33H: IBCD Deactivate Code

Bit	Type	Function
Bit 7	R/W	DACT[7]
Bit 6	R/W	DACT[6]
Bit 5	R/W	DACT[5]
Bit 4	R/W	DACT[4]
Bit 3	R/W	DACT[3]
Bit 2	R/W	DACT[2]
Bit 1	R/W	DACT[1]
Bit 0	R/W	DACT[0]

This 8-bit register allows selection of the deactivate code sequence that is to be detected. If the code is less than 8 bits long, the first 8 bits of the repeated sequence must be used to fill this register. For example, if the code sequence is '10011', the first 8 bits of '1001110011...' are '10011100'). Note that bit 7 is the first code bit received.

RSLC Registers

Register 17H, 37H: RSLC Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R	LV
Bit 4	R	SQ
Bit 3	R	LVI
Bit 2	R	SQI
Bit 1	R/W	LVE
Bit 0	R/W	SQE

This register indicates the current state of the alarm outputs, selects which alarms can generate interrupts and identifies the source of the pending interrupt. The LV and SQ bits reflect the current state of the the low level alarm and the squelch alarm. The LVE bit and the SQE bit are interrupt enables for the low level signal alarm and squelch alarm, respectively. The LVI and SQI bits indicate whether the low level alarm or the squelch alarm generated the interrupt. These bits and the interrupt are cleared when this register is read. Regardless of whether interrupts are enabled or disabled, the LVI and SQI bits retain their event capture function.

XIBC Registers

Register 18H, 38H: XIBC Configuration

Bit	Type	Function
Bit 7	R/W	EN
Bit 6	R/W	IF
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	CL[1]
Bit 0	R/W	CL[0]

All of the bits in this register go to logic 0 when the TSB is reset.

The EN bit in the XIBC configuration register controls the transmission of inband codes. When it is set to logic 1, the input to DJAT is replaced by the code stored in the XIBC inband code register. This code sequence will be transmitted repetitiously until EN is negated.

The IF bit in the XIBC configuration register controls the insertion of framing bits into the inband code when the TFBT bit is set to logic 1 in the DDSX transmit control register. When IF is set to logic 0, an unframed inband code is transmitted. When IF is set to logic 1, a framed inband code is transmitted, provided that the TFBT bit is set to logic 1 in the DDSX transmit control register and assuming that an upstream device is providing framing to the DDSX on the TPCMP input and marking the framing bits with a positive pulse on the TPCMN input.

Bits 1 and 0 (CL1[1:0]) of this register indicate the length of the inband loopback code sequence, as follows:

CL[1]	CL[0]	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of three or four bits in length may be accommodated by treating them as half of a double-sized code.

Register 19H, 39H:
XIBC Inband Code

Bit	Type	Function
Bit 7	R/W	IBC[7]
Bit 6	R/W	IBC[6]
Bit 5	R/W	IBC[5]
Bit 4	R/W	IBC[4]
Bit 3	R/W	IBC[3]
Bit 2	R/W	IBC[2]
Bit 1	R/W	IBC[1]
Bit 0	R/W	IBC[0]

Bits IBC[7:0] contain the inband loopback code pattern to be transmitted. Since IBC[7] is the first bit transmitted, followed by IBC[6], the code should always be aligned with the MSB in the bit 7 position (for example, a 5-bit code would occupy positions bit 7 through bit 2). Note that 3 or 4-bit patterns must be paired to form a double-sized code (for example, the 3-bit code '011' would be entered as the 6-bit code '011011').

XPLS Registers

Register 1CH, 3CH:
XPLS Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	SM
Bit 5	R	LS[2]
Bit 4	R	LS[1]
Bit 3	R	LS[0]
Bit 2	R/W	ILS[2]
Bit 1	R/W	ILS[1]
Bit 0	R/W	ILS[0]

The XPLS Configuration Register contains signals related to the choice of analog waveform templates used to drive the TXTIP and TXRING pins. Bits 5 to 0 contain waveform select signals ILS[2:0] and LS[2:0]. These bits program the XPLS for the length of cable it is required to drive. Eight waveform templates are available. The LS bits reflect the value of the LS pins associated with the local copy of the line interface in the DDSX. The ILS bits facilitate template selection in software. The values on the LS[2:0] bits of this register are in effect if the SM bit is set to logic 0. Otherwise, the ILS pin values are in effect.

The eight available templates and the values of LS[2:0] or ILS[2:0] used to select them are listed is the table below:

ILS[2:0] / LS[2:0]	Length (ft.)
000	0-110
001	110-220
011	220-330
010	330-440
110	440-550
111	550-660
101	>655
100	square

The >655 setting is used when driving very long lines. The square pulse allows the use of external LBO networks with the TSB.

Register 1DH, 3DH: XPLS Control, Interrupt Enable and Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	PDNDAC
Bit 3	R/W	TAIS
Bit 2	R	DPMV
Bit 1	R	DPMI
Bit 0	R/W	DPME

The driver performance monitor interrupt can be enabled by asserting (HI) and disable by negating (LO) the DPME bit. Reading the DPME bit returns the current state of the interrupt mask. The bit DPMI is asserted (HI) when the internal driver performance monitor in XPLS changes states and is negated when this register is read. The monitor enters the alarm state when the PMTIP and PMRING pins have not pulsed alternately for 63 bit periods. It will return to normal state upon receiving the first alternating pulse. The DPMV bit is asserted (HI) when the driver performance monitor is in the alarm state, and negated in the normal state.

The bit TAIS is OR'ed with the external TAIS pin to enable AIS transmission. Reading this bit returns the value.written.

The PDNDAC bit disables the internal DAC bias current generator when asserted (HI) to reduce power consumption. This bit must be negated if the DDSX is driving the TXTIP and TXRING pins.

TEST FEATURES DESCRIPTION

The DDSX provides a test feature for simplification of in-circuit test. When CSB, WRB, and RDB are simultaneously brought low (normally an illegal combination of input states) all outputs and bidirectionals are forced to a high impedance state.

The DDSX provides test features that allow direct testing of its constituent TSBs. When the SILVERB input is low, some of the address inputs are redefined to allow evaluation modes to be selected as follows.

A[4]	A[3]	A[2]	Evaluation Mode
0	X	X	DJAT Evaluation
1	0	0	XPLS Evaluation
1	0	1	Reserved
1	0	1	RSLC Evaluation
1	1	1	CDRC Evaluation

In all evaluation modes, SILVERB must be low. When a particular TSB is under evaluation, most signals associated with the TSB are individually accessible in both TSBs on each side of the DDSX. However, some input signals are common between the TSBs in each side of the DDSX due to the limited number of pins available.

When the SILVERB input is low, some DDSX inputs and outputs are redefined in accordance with the selected evaluation mode as shown in the following table. In the evaluation modes, the signal names correspond to the signal names used on the TSB under evaluation. The only exception is SIDE, which is the signal (A[5]) selecting between TSBs associated with each side of the DDSX. The INTB1 and INTB2 pins remain as open drain pins in evaluations mode. They are, therefore, active low. The sense of the TSB INT signals is complemented in evaluation mode.

The clock doubler glue logic is also evaluated in the RSLC evaluation mode. The XCLK/VCLK and DBLEN pins retain their normal mode functions as source clock and clock doubling enable signals, respectively. The RCLK1 and RCLK2 pins are remapped to DCLK, output clock of the clock doubler logic. When DBLEN is set to logic 1, the doubler is active. A pulse of logic 1 is generated at each transition of XCLK. If DBLEN is set to logic 0, DCLK follows XCLK.

Connector Name	Type	Pin No.	DJAT Eval	XPLS Eval	RSLC Eval	CDRC Eval
XCLK/VCLK	Input	50	CX24	SCLK1	XCLK	SCLK1
DBLEN	Input	79	FCLK	SCLK2	DBLEN	SCLK2
TCLK[1]	I/O	32	ICLK1	TCLK1	Not Used	*PCM1*
TCLK[2]	I/O	12	ICLK2	TCLK2	Not Used	*PCM2*
TPCMP[1]	Input	30	AIN1	TP1	Not Used	RP1
TPCMP[2]	Input	14	AIN2	TP2	Not Used	RP2
TPCMN[1]	Input	31	BIN1	TN1	Not Used	RN1
TPCMN[2]	Input	13	BIN2	TN2	Not Used	RN2
TAIS[1]	I/O	48	OCLK1	AIS1	Not Used	*DPCM1*
TAIS[2]	I/O	80	OCLK2	AIS2	Not Used	*DPCM2*
RCLK[1]	Output	38	SCO1	Low	DCLK	PCLK1
RCLK[2]	Output	6	SCO2	Low	DCLK	PCLK2
RPCMP[1]	Output	39	AOUT1	OUTP1	OUTP1	PCMP1
RPCMP[2]	Output	5	AOUT2	OUTP2	OUTP2	PCMP2
RPCMN[1]	Output	42	BOUT1	OUTN1	OUTN1	PCMN1
RPCMN[2]	Output	2	BOUT2	OUTN2	OUTN2	PCMN2
RLOS[1]	Output	43	SCX8O1	DPM1	SQLCH1	LOS1
RLOS[2]	Output	1	SCX8O2	DPM2	SQLCH2	LOS2
RLCV[1]	Output	44	OVRR1+ UDRR1	Low	LEVL1	LCV1
RLCV[2]	Output	84	OVRR2+ UDRR2	Low	LEVL2	LCV2
LS0[1]	I/O	45	*FULL1*	LS01	Not Used	*B8ZS1*
LS0[2]	I/O	83	*FULL2*	LS02	Not Used	*B8ZS2*
LS1[1]	I/O	46	*EMPTY1*	LS11	Not Used	*Z8D1*
LS1[2]	I/O	82	*EMPTY2*	LS12	Not Used	*Z8D2*
LS2[1]	I/O	47	*CX8O1*	LS21	Not Used	*Z16D1*
LS2[2]	I/O	81	*CX8O2*	LS22	Not Used	*Z16D2*

INTB[1]	Output	37	INT1	INT1	INT1	INT1
INTB[2]	Output	7	INT2	INT2	INT2	INT2
A[2]	Input	20	REF1	Low	High	High
A[3]	Input	23	REF2	Low	Low	High
A[4]	Input	24	Low	High	High	High
A[5]	Input	25	SIDE	SIDE	SIDE	SIDE
SILVERB	Input	15	Low	Low	Low	Low

The *italic* style text is used to indicate output signal names where the connector type is I/O.

Test mode registers are used to apply test vectors during production testing of the DDSX. Test mode registers (as opposed to normal mode registers) are selected when TRSB (CBI[13]) is low.

Test mode 0 provides access to the values of the TSB's primary inputs and control of the primary output values, allowing rapid verification of inter-TSB connectivity. Test modes other than test mode 0 are reserved for production testing.

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 01H, 21H: Test Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	W	PTEST
Bit 3	W	DBCTRL
Bit 2	W	IOTEST
Bit 1	W	HIZDATA
Bit 0	W	HIZIO

The Test Configuration Register is provided at DDSX address 01H and 21H when TRSB, and CSB are low. Either address will access the same register. This register controls the actions of the DDSX under testing conditions. All bits, except PTEST, are reset to logic 0 by a hardware reset of the DDSX, while a software reset to either line interface has no effect.

The PTEST bit is used to place the DDSX in production test mode. When PTEST is set to logic 1, all blocks are held in test mode. Production test vectors used to verify manufacture are executed with PTEST set high. PTEST is reset when the CSB input is set high.

The IOTEST bit is used to allow normal microprocessor access to the test registers in each block in the DDSX. When IOTEST is set to logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate its outputs and consequently the chip's outputs (refer to the section "Test Mode 0" for details).

The HIZIO and HIZDATA bits control the tri-state modes of the DDSX. While the HIZIO bit is set to logic 1, all output pins in the DDSX are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is set to logic 1, the data bus is held in a high-impedance state inhibiting microprocessor read cycles. Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin in test mode. When the DBCTRL bit is set to logic 1 and the IOTEST bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is asserted, holding the CSB pin high causes the DDSX to drive the data bus, and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the

HIZDATA bit. The DBCTRL bit is used in tests that measure the drive capability of the data bus driver pads.

Test Mode 0

In test mode 0, the DDSX allows the logic levels on the device inputs to be read, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the TRSB pin must be set to logic 0, the IOTEST bit in the Test Configuration register must be set to logic 1, the IOTEST or PTEST bits in the Test Configuration Register must be set to logic 1, and the test mode select registers in each constituent TSB must be written with 00H. The test mode select registers are at addresses 09H, 0DH, 11H, 15H, 19H, 1DH, 29H, 2DH, 31H, 35H, 39H, and 3DH.

Reading the following address locations with TDUAL in the Master Transmit Control Register set to logic 1 returns the values for the indicated inputs in the table below. The TAIS pin is synchronized external to the XPLS TSB. Therefore, it can only be sensed at the TSB after two TCLK cycles.

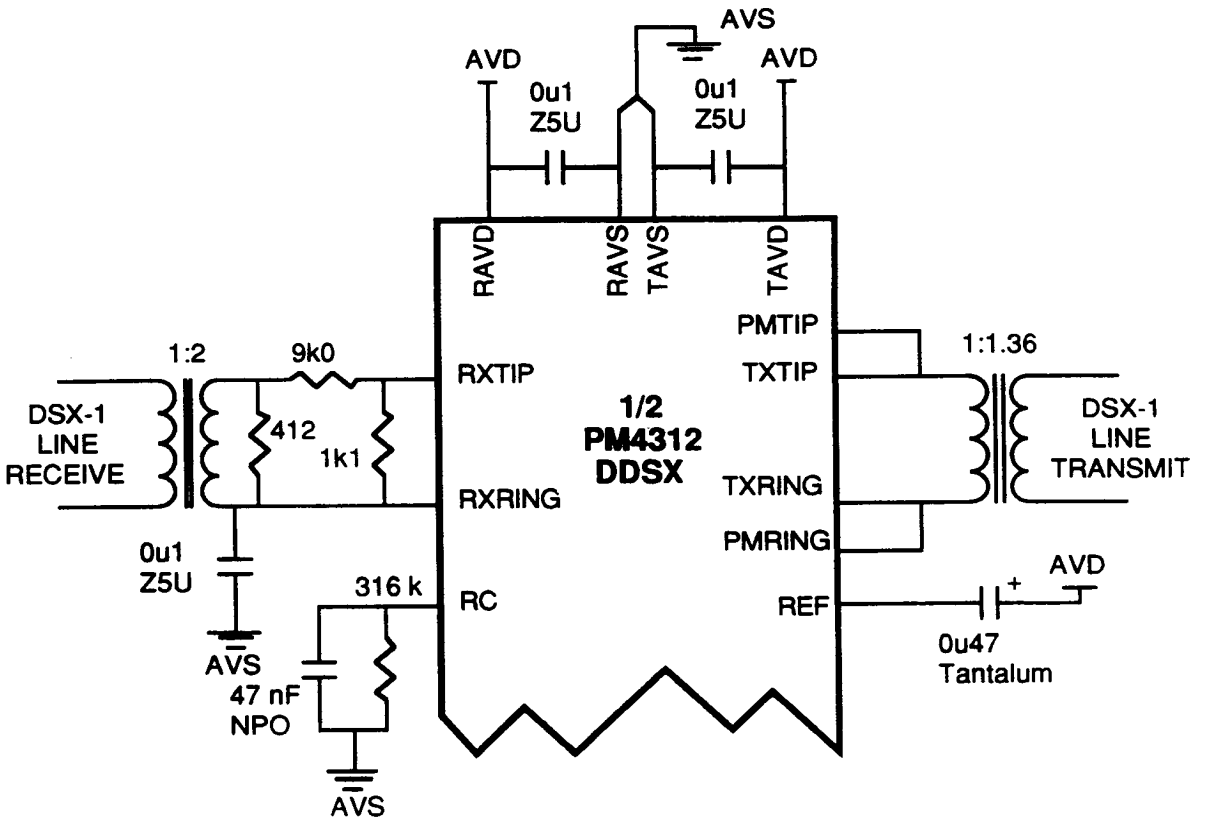
DSX0	DSX1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0CH	2CH			TCLK				TPCMN	TPCMP
1CH	3CH				TAIS				

Writing the following address locations forces the outputs to the value in the corresponding bit position:

DSX0	DSX1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08H	28H	RPCMP	CDRCI†			RLOS	RLCV	RPCMN	RCLK
0CH	2CH	DJATI							
10H	30H						IBCDI		
1CH	3CH								XPLSI

†Note: The active high block interrupt lines (CDRCI, DJATI, IBCDI, and XPLSI) may be masked in the Master Interrupt Enable Register at the originating block and therefore may not be able to assert the active low INTB output. The interrupt signals of any of the unmasked blocks' can assert the INTB output.

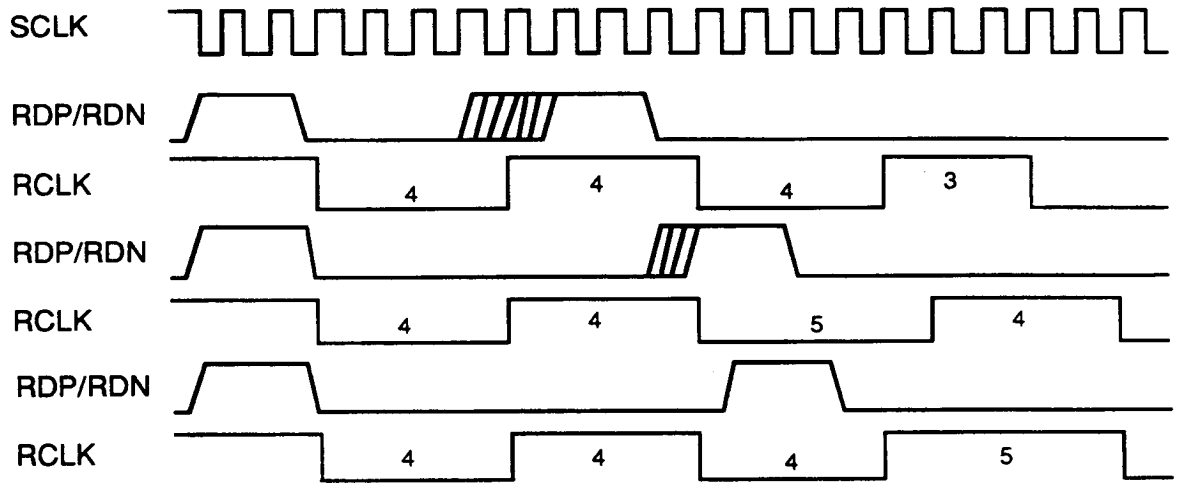
APPLICATION EXAMPLES



FUNCTIONAL TIMING

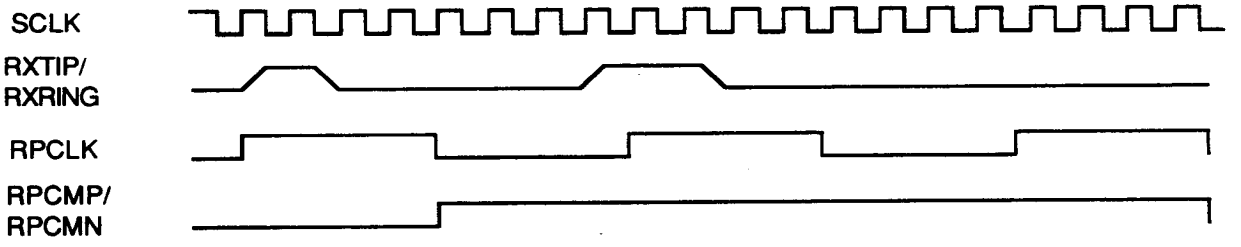
Clock and Data Recovery

Fig. 10 Clock Recovery



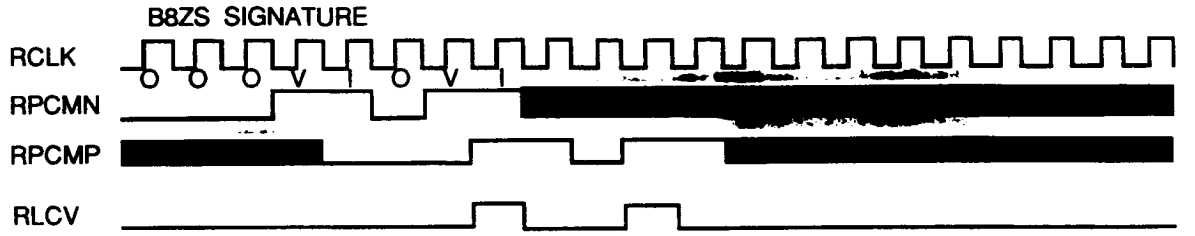
The diagram above shows the recovery of the PCM clock, RCLK, by the CDRC Block. The nominal period of RCLK is 8 SCLK cycles but the period may be from 7 to 9 SCLK cycles. The early arrival of a positive or negative input pulse (RDP/RDN) causes the instantaneous frequency of RCLK to increase, as shown in the first PCLK trace. (Note that RPCLK may be high for three SCLK cycles, but it may not be low for three SCLK cycles). The late arrival of a RDP/RDN pulse causes the instantaneous frequency of RCLK to decrease, as shown in the second and third RCLK traces. (Note that RCLK may be either high or low for five SCLK cycles).

Fig. 11 Data Recovery



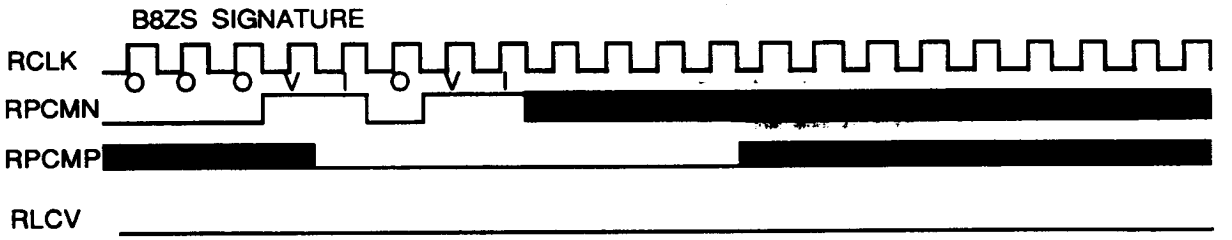
The diagram above shows the conversion of RZ data to NRZ data function of the CDRC block. A pulse on RXTIP/RXRING of length of one SCLK cycle or greater will be latched through on the falling edge of RPCLK. When the receiver is in the dual rail mode (RDUAL asserted), the RPCMP and RPCMN pins reflect the values on RXTIP and RXRING, respectively, in NRZ format.

Fig. 12 AMI Line Code Timing



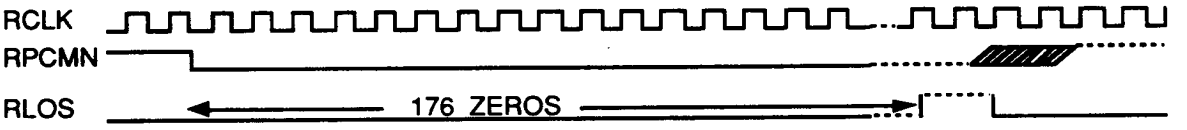
The above timing diagram shows the processing of B8ZS signature while AMI line code is selected. The bipolar violations in the B8ZS pattern are identified. When the receiver is in single rail mode (RDUAL negated), RPCMP reports the AMI decoded PCM signal, while RPCMN reports the recovered PCM signal.

Fig. 13 B8ZS Line Code Timing



The processing of B8ZS signature with B8ZS line code selected is shown in the above diagram. Eight (8) zeros are substituted for the signature and reporting of the line code violations are suppressed. When the receiver is in single rail mode, RPCMP reports the B8ZS decoded PCM signal, while RPCMN reports the recovered PCM signal.

Fig. 14 Loss of Signal (LOS) Timing



The above diagram shows the detection of loss of signal after 176 consecutive zeros.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-40°C to +125°C
Voltage on V_{DD} with Respect to GND	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to +6.0V
Static Discharge Voltage	2000 V
Latch-Up Current (T_a = 0°C to +85°C)	400 mA

D.C. CHARACTERISTICS

(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}, A_{VD}	Power Supply	4.5	5.5	Volts	
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0	V_{DD}	Volts	Guaranteed Input HIGH Voltage
V_{RAS}	Analog Input Voltage	A_{VS} -0.6	A_{VD} -0.6	Volts	
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, **Note 3**
V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, **Note 3**
V_T	Reset Input High Voltage	2.3	2.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage	0.5	1.2	Volts	
I_{ILPU}	Input Low Current	-26	-110	µA	V_{IL} ≤ 1.65 V, **Notes 1, 3**
I_{IHPU}	Input High Current	-48	-110	µA	V_{IH} ≥ 3.85 V, **Notes 1, 3**
I_{IL}	Input Low Current	-10	0	µA	V_{IL} ≤ 1.65 V, **Notes 2, 3**
I_{IH}	Input High Current	-10	0	µA	V_{IH} ≥ 3.85 V, **Notes 2, 3**
I_{DDOP}	Operating Current		118	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 37.056 MHz TCLK = 1.544MHz, **Note 4**
I_{DDSB}	Standby Current		68	mA	V_{DD} = 5.5 V, A_{VD} = 0 V, Outputs Unloaded, **Note 5**

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. I_{DDOP} is the sum of all power supply currents when transmitting all ones from both DDSX halves, producing 2.7 volt pulses across a 54 ohm load. The I_{DDOP} will increase by 1 mA with an external crystal and with D.C.loading.

5. I_{DDSB} is the sum of all power supply currents when no pulses are transmitted from either DDSX half. The XPLS PDNDAC bit is set to logic one in the standby mode. The I_{DDSB} will increase by 1 mA with an external crystal and with D.C.loading.

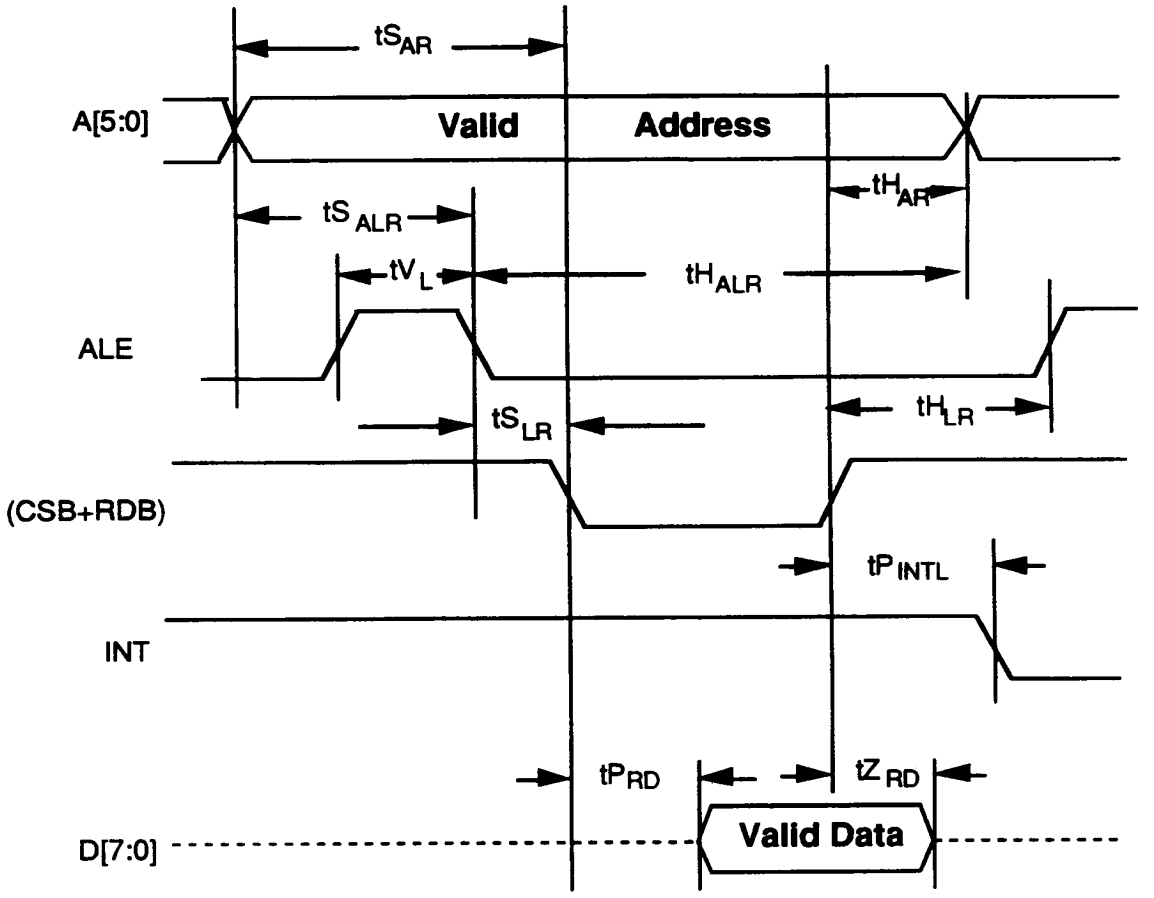
MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

Microprocessor Interface Read Access (Fig. 15)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	20		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		20	ns
tP_{INTL}	Valid Read Deasserted to INT Low		50	ns

Fig. 15 Microprocessor Interface Read Access Timing



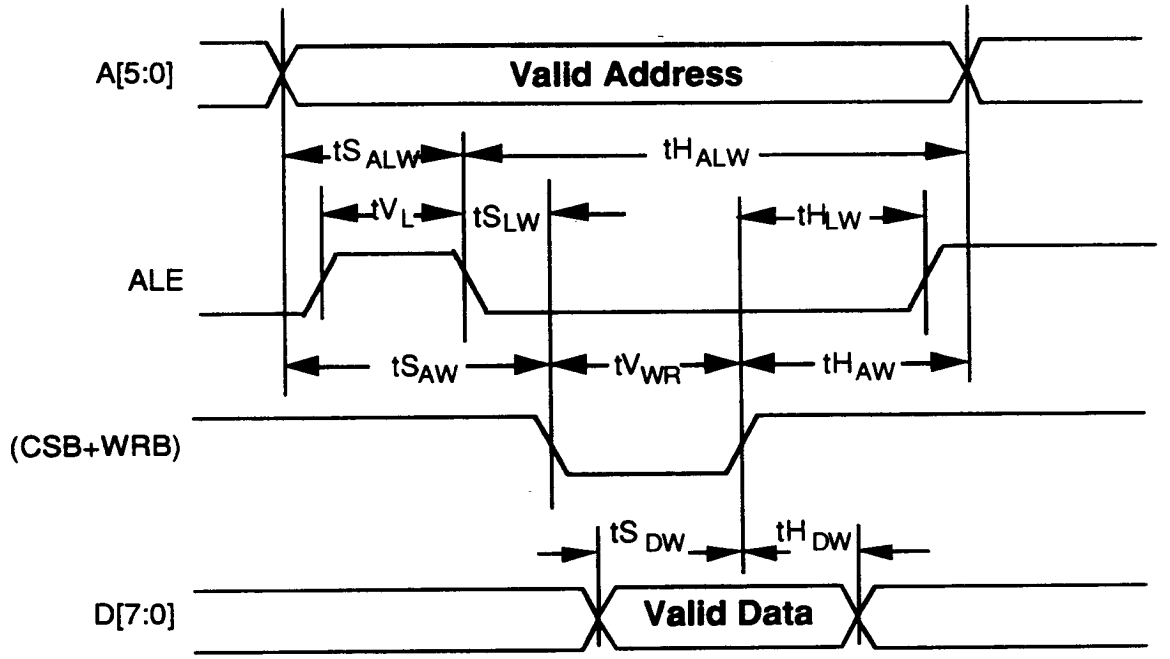
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.
5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
6. Parameter tH_{AR} is not applicable is address latching is used.

Microprocessor Interface Write Access (Fig. 16)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	20		ns
tV_{L}	Vaild Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 16 Microprocessor Interface Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.
4. Parameter tH_{AW} is not applicable is address latching is used.

DDSX TIMING CHARACTERISTICS

(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

PCM Interface Input Timing (Fig. 17, 18 and 19)

Symbol	Description	Min	Max	Units
tP_{AIN}	RXTIP/RXRING analog input pulse width	300	405	ns
tP_{PIN}	PMTIP/PMRING analog input pulse width	300	405	ns
tS_{TPCM}	TPCMP/TPCMN set-up time before TCLK rise	30		ns
tH_{TPCM}	TPCMP/TPCMN hold time after TCLK rise	30		ns

Fig. 17 Receiver Analog Input Timing

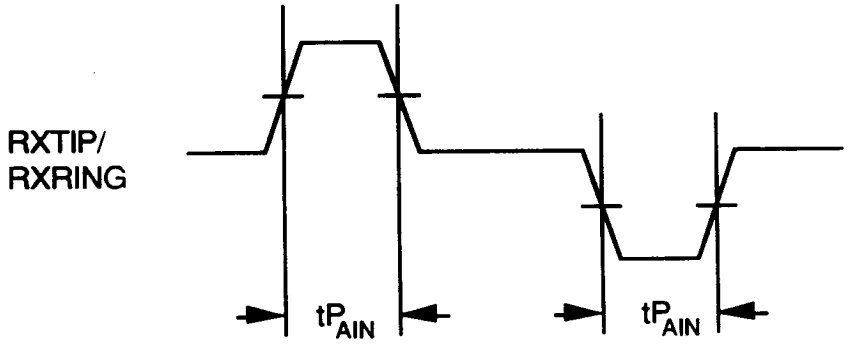


Fig. 18 Driver Performance Monitor Analog Input Timing

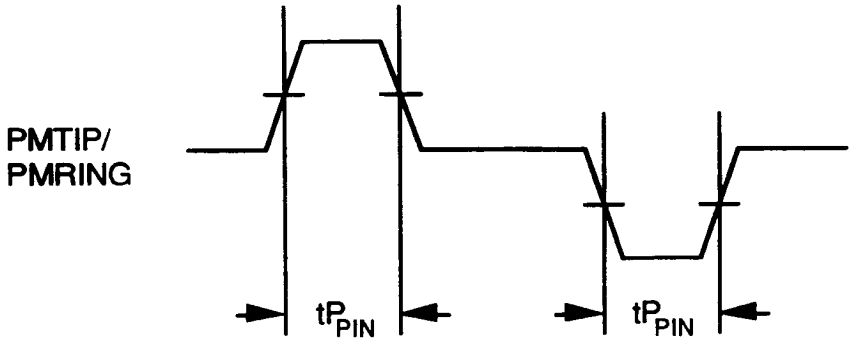
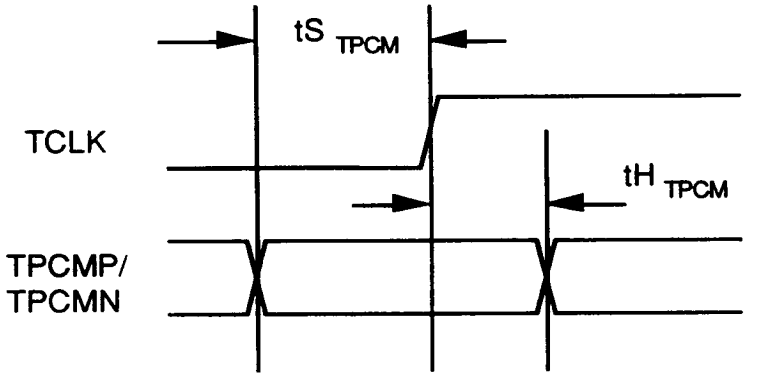


Fig. 19 Transmitter Input Data Timing



Notes on PCM Interface Input Timing:

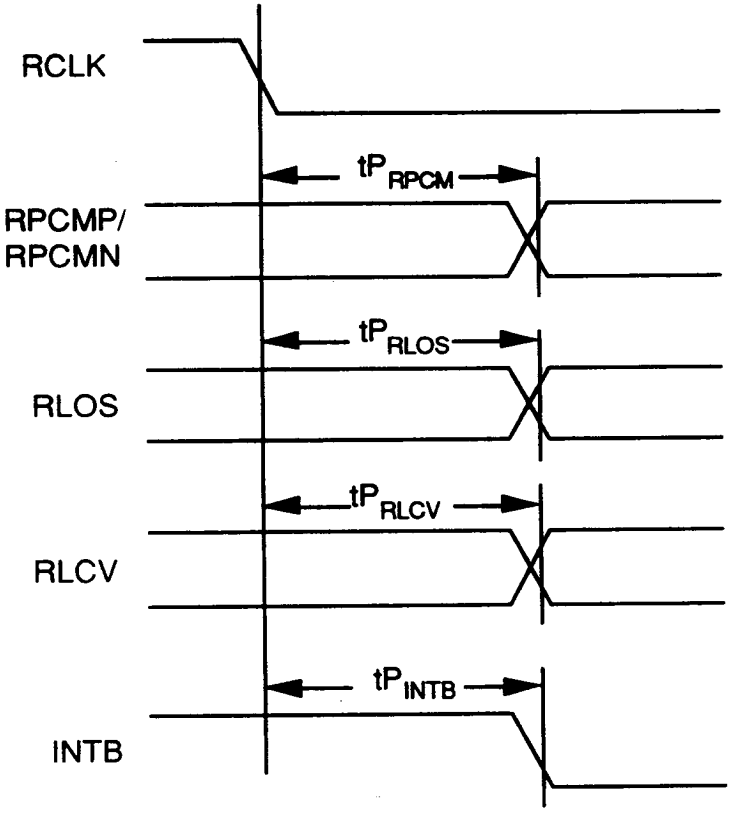
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

PCM Interface Output Timing (Fig. 20)

Symbol	Description	Min	Max	Units
tP_{RCLK}	RCLK propagation delay		60	ns
tPR_{PCM}	RPCMP/RPCMN propagation delay		35	ns
tP_{RLOS}	RLOS propagation delay		35	ns
tP_{RLCV}	RLCV propagation delay		35	ns
tP_{INTB}	INTB propagation delay		100	ns

Fig. 20 Receiver Output Timing



Notes on PCM Interface Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

NOTES

901014P2 ref 900516P7 Issue date: October, 1991.

Printed in Canada

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