Semiconductor Corporation

CS3112

High Speed Precision Track and Hold

Features

- Completely Self-Contained On-Chip Hold Capacitor Microprocessor Interface
- Fast Acquisition: 800ns to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset, Including Hold Pedestal: 1.8 mV
- Low Droop Rate: 0.001uV/us
- Self-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 130 mW

General Description

The CS3112 is a high speed track and hold with 12-bit linearity. It is completely self-contained, including hold capacitor, output buffer, and calibration circuitry.

Aperture jitter of 100ps and acquisition time of 800ns to 0.01% provide excellent dynamic performance. An on-chip hold capacitor limits droop to 0.001 uV/us, and first order leakage compensation minimizes droop over the full operating temperature range.

Advanced CMOS fabrication insures low power consumption and increased reliability.

The CS3112 can be controlled and monitored through its microprocessor interface, or can operate independently.

ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS3112-KD2	2.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-KD1	1.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-BD1	1.0 µs	-40 to +85 °C	14-pin CerDIP
CS3112-TD1	1.0 µs	-55 to +125 °C	14-pin CerDIP

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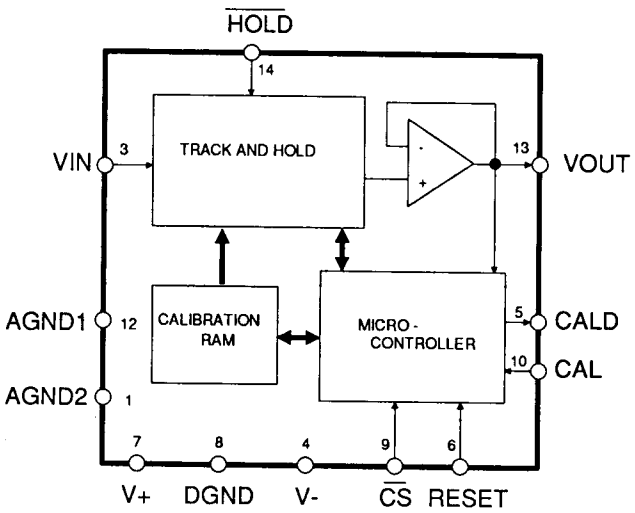


ANALOG CHARACTERISTICS (T_A = 25°C, V+ = +5.0V, V- = -5.0V, R_L = 10KΩ, C_L = 50pF, Analog Source Impedance = 40Ω, unless otherwise specified)

Parameter*	CS3112-K min	CS3112-K typ	CS3112-K max	CS3112-B min	CS3112-B typ	CS3112-B max	CS3112-T min	CS3112-T typ	CS3112-T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Total Offset (Note 1) 25°C		−1.8	± 3.0		−1.8	± 3.0		−1.8	± 3.0	mV
T_{min} to T_{max}			± 3.5			± 3.5			± 3.5	mV
Offset Drift (Note 2) T_{min} to T_{max}		± 0.020			± 0.025			± 0.030		mV/°C
Tracking Offset			± 55			± 55			± 55	mV
Nonlinearity 25°C			± 0.7			± 0.7			± 0.7	mV
(Note 3) T_{min} to T_{max}		± 0.5			± 0.5			± 0.5		mV
Gain Error T_{min} to T_{max}		± 0.01			± 0.01			± 0.01		% FS
Dynamic Characteristics										
Acquisition Time -1		0.8	1.0		0.8	1.0		0.8	1.0	us
(6V step to 0.01%) -2		1.6	2.0							us
-1		0.6			0.6			0.6		us
(6V step to 0.1%) -2		1.2								us
Track to Hold Settling to 0.01%		0.5	0.8		0.5	0.8		0.5	0.8	us
Aperture Time		20			20			20		ns
Aperture Time Matching (Note 4)		2			2			2		ns
Aperture Jitter		100			100			100		ps
Droop Rate 25°C		± 0.001	± 0.1		± 0.001	± 0.1		± 0.001	± 0.1	uV/us
T_{min} to T_{max}			± 0.6			± 1.0			± 5.0	uV/us
Analog Input/Output										
Large Signal Bandwidth (6V p-p Input)		2.0			2.0			2.0		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		5			5			5		pF
Input Bias Current		100			100			100		pA
Output Impedance at dc (Note 3)		0.1			0.1			0.1		Ω
Output Slew Rate		10			10			10		V/us
Noise (Note 5) Track Mode		50			50			50		uV_{rms}
Hold Mode		33			33			33		uV_{rms}
Power Supplies										
Supply Currents Positive		13	20		13	20		13	20	mA
Negative		−13	−20		−13	−20		−13	20	mA
Power Supply Rejection Ratio										
Positive (Note 6)		75			75			75		dB
Negative (Note 7)		60			60			60		dB

*Refer to Error Definitions at the end of this data sheet.

Specifications are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 8).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	- 4.5	−5.0	−5.5	V
Analog Input Voltage:	V_{IN}	- 3.0	-	3.0	V

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5V±10%; V- = -5V±10%)

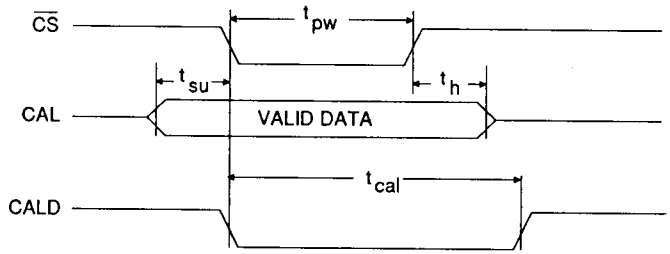
All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	1.7	-	V
Low-Level Input Voltage	V_{IL}	-	1.6	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	(V+) - 1.0V	-	-	V
Low-Level Output Voltage, Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA

SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
CAL to $\overline{CS}$ Setup Time	t_{su}	20	5	-	ns
$\overline{CS}$ to CAL Hold Time	t_h	20	5	-	ns
$\overline{CS}$ Pulse Width	t_{pw}	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	t_{cal}	-	500	-	ms

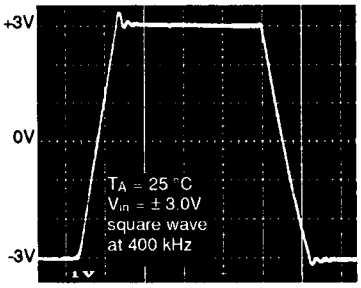
Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Applies over specified temperature range without recalibration since calibration at 25°C.
3. Applies over the input voltage range of -3.0V to +3.0V.
4. Part to part.
5. Total noise from dc to 1MHz.
6. With 300 mV_{p-p}, 1kHz ripple applied to V+.
7. With 300 mV_{p-p}, 1 kHz ripple applied to V-.
8. All voltages with respect to ground.
9. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = +2.4V @ I_{out} = -40µA).



CS3112 Timing Diagram

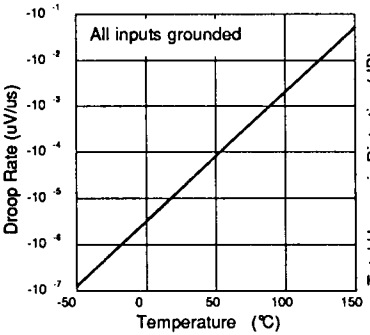
TYPICAL PERFORMANCE CHARACTERISTICS

(V+ = +5.0V, V- = -5.0V)

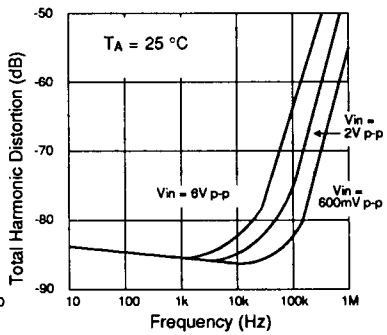


500 ns/div.

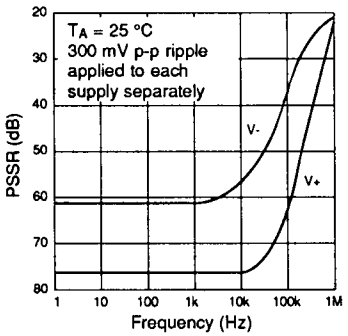
Full Scale Acquisition



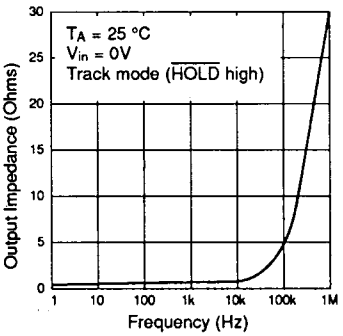
Droop Rate vs. Temperature



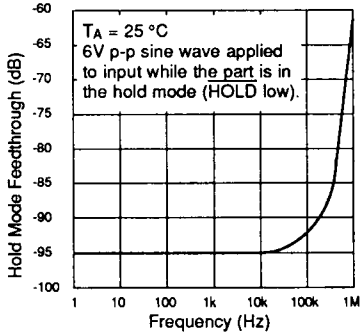
Distortion vs. Frequency



PSSR vs. Frequency



Output Impedance vs. Frequency



Hold Mode Feedthrough vs. Frequency

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V+	−0.3	6.0	V
Negative	V-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 10)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	V- - 0.3	V+ + 0.3	V
Digital Input Voltage	V_{IND}	-0.3	V+ + 0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 10. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is ±100 mA.

GENERAL DESCRIPTION

The CS3112 consists of a complete track-and-hold amplifier with on-chip hold capacitor, an output buffer, and calibration circuitry. Use of an on-chip buffer isolates the track-and-hold amplifier from load conditions for optimal performance, and the calibration circuitry nulls out error sources. The CS3112 requires no external components or manual trims of any kind to achieve 12-bit performance.

The CS3112 can be controlled through its on-board microprocessor interface, or can be operated independently. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output.

Calibration

In the calibration mode, an internal microcontroller and special nulling circuitry reduce all errors at the VOUT pin. The controller disconnects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. This voltage is captured on the internal hold capacitor, and a DAC is adjusted to remove any error. Thus, all internal errors, including dc offset and dynamic errors due to charge injection (hold pedestal), are trimmed. During tracking, there may be up to ±55mV of offset.

At power-up, the user must calibrate the device. Calibration is achieved by bringing the CAL input high with $\overline{CS}$ low. (In the stand-alone mode, $\overline{CS}$ is grounded, so only the CAL pin needs to be pulsed.) Calibration can be similarly initiated during operation at any time, thus insuring accuracy under any conditions.

During the calibration cycle (which takes about 500ms to complete) the CALD pin remains low. During this period, any load on VOUT must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS3112 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

Digital Interface

The CS3112 includes a digital interface designed for maximum flexibility. In a microprocessor-controlled application, the $\overline{CS}$ control input is usually derived from a decoded address as well as write and strobe signals from the control bus (see Figure 1a). Calibration initiation thereby involves writing to the CS3112's address using a data bit to control CAL. For microprocessor-independent operation, $\overline{CS}$ is tied low and the digital inputs are controlled by externally-latched signals (see Figure 1b).

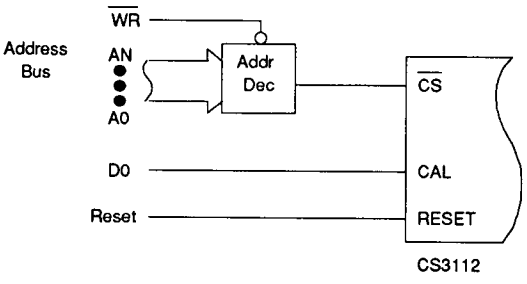


Figure 1a. CPU-Control

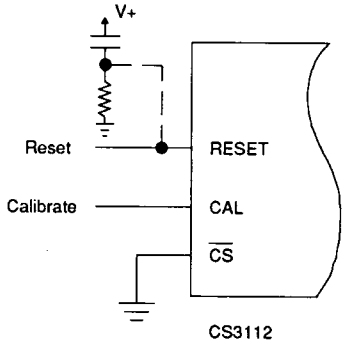


Figure 1b. Independent Control

The CS3112's CALD output can be used to generate an interrupt indicating that calibration has been completed. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a three-state buffer.

Reset

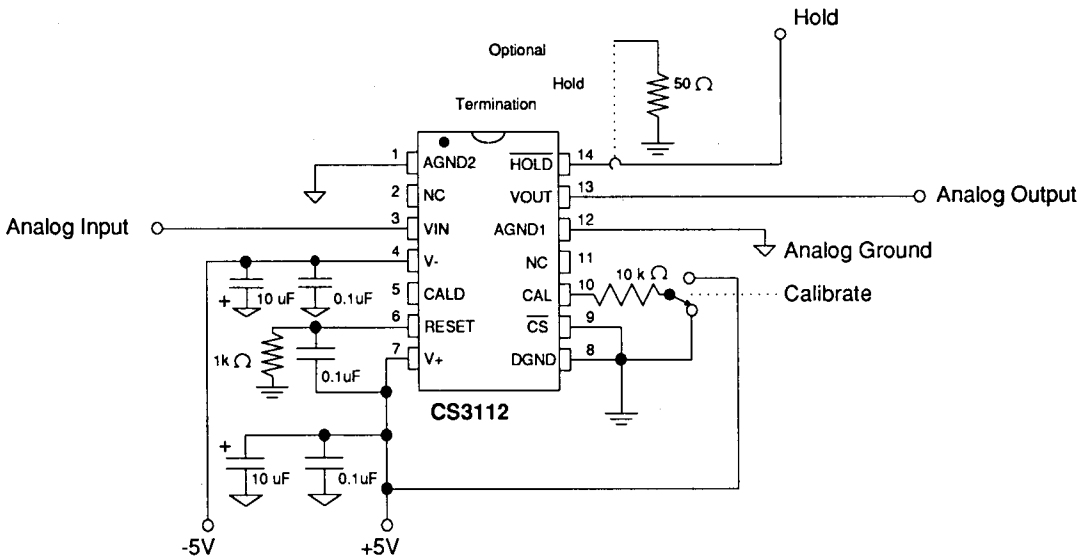
The CS3112 must be reset after power up to ensure correct operation. The CS3112 is reset when the RESET pin is high for at least 1µs. An RC network attached to the RESET pin will reset the part (See Figure 1b).

Power Supplies and Input Connections

The CS3112 uses the analog ground voltage (AGND1) only as a reference voltage. No signal or dc power currents flow through the AGND1 connection, and it is completely independent of DGND. Both the analog input and output are referenced to to the AGND1 pin internally, and this pin needs to be at the same potential as the entire system's analog ground plane to minimize offset errors induced by noise between the AGND1 pin and the system analog ground.

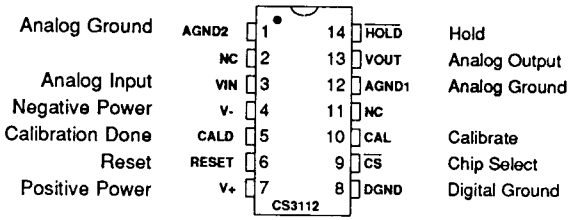
Decoupling should be performed between the V+, V- pins and AGND1 using 0.1µF ceramic capacitors. If significant low frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors. *The decoupling capacitors should be placed as close to the CS3112's power supply pins as possible.*

The signal source impedances which drive the input of the CS3112 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pin to picking up capacitively-coupled energy from logic level transitions, such as $\overline{\text{HOLD}}$ going low.



Simple Test Connections - Independent Operation

PIN DESCRIPTION



Analog Input and Output

VIN - Analog Input, PIN 3
Analog input to the track-and-hold amplifier.

VOUT - Analog Output , PIN 13
Buffered output from the track-and-hold.

Power Supplies

V+ - Positive Power, PIN 7
Most positive supply voltage. Nominally +5 volts.

V- - Negative Power, PIN 4
Most negative supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 8
Digital ground.

AGND1, AGND2 - Analog Ground, PIN 12, PIN 1
Analog ground reference.

Digital Inputs and Outputs

$\overline{\text{HOLD}}$ - Hold, PIN 14
A falling transition on this pin switches the track-and-hold amplifier to the hold mode. When brought high, the track-and-hold is switched to the track mode, and acquires and then tracks the input signal.

CAL - Calibrate, PIN 10
When taken high with $\overline{\text{CS}}$ low, initiates a full internal calibration.

CALD - Calibration Done, PIN 5

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low, the device is calibrating.

CS - Chip Select, PIN 9

Enables the CAL digital inputs.

RESET - Reset, PIN 6

The CS3112 must be reset after power up to ensure correct operation. Reset occurs when RESET is high.

NC - No Connect, PINS 2,11

No connection should be made to these pins.

ERROR DEFINITIONS

Total Offset

The difference between the analog input voltage and the voltage at the output pin after thehold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

Nonlinearity

The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

Gain Error

Calculated as the difference between the errors resulting from a -3V and a +3V dc input signal, relative to a 6V input range. Units in percent of full scale.

Acquisition Time

The time required after the negation of the hold command ($\overline{\text{HOLD}}$ high) for the track-and-hold amplifier to reach its final value to within a specified error band (±0.01% or ±0.1%). This determines the minimum time allowed before reassertion of the hold command. Units in microseconds.

Track-to-Hold Settling

The time required after the hold command is given for the output buffer amplifier to reach its final value to within a specified error band (±0.01%). Includes switch delay (aperture) time. Units in microseconds.

Aperture Time

The delay after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Droop Rate

The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

Large Signal Bandwidth

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a full scale 6V p-p sine wave. Units in megahertz.

Small Signal Gain Bandwidth

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a 60mV p-p sine wave. Units in megahertz.