GREENWICH INSTRUMENTS LTD

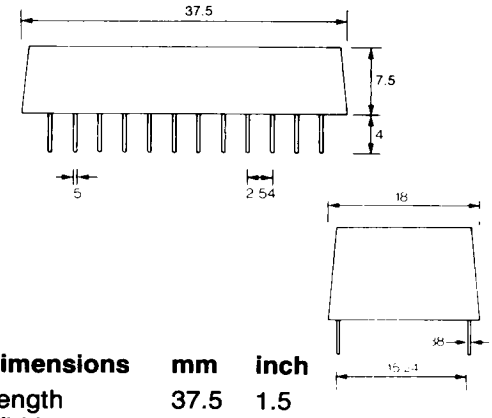
8K x 8 NON-VOLATILE RAM

NVR8

- Plug-in replacement for Static RAM chips
- Retains data for up to 10 years
- No erasure required
- Functions as Data or Proram RAM
- No limit to number of programming cycles
- Fits standard 28-pin socket
- Write Protectable

NVR8 is a 8 kilobyte non-volatile memory module which is pin-compatible with normal Static RAM chips, and offers immediate conversion to non-volatile memory of all or part of a system, able to retain data and survive power-downs for up to 10 years.

REPLACES: HM 6264 - TC 5565



Dimensions	mm	inch
Length	37.5	1.5
Width	18.0	0.7
Height	7.5	0.3

MAXIMUM RATINGS

Symbol	Min	Max	Unit
V_{dd}	−0.3	7.0	Volts
$V_{i/o}$	−0.3	V_{dd} + 0.3	Volts
Temp.	−10	+60	deg. C

OPERATING CONDITIONS

Symbol	Min	Typ	Max	Unit
V_{dd}	4.5	5.0	5.5	V
V_{in} (1)	2.2		V_{dd} + 3	V
V_{in} (0)	−.3		0.8	V
I_{in} (any pin)*	−1		+1	uA
V_{out} (1) (I_{out} = −1mA)	2.4			V
V_{out} (0) (I_{out} = −2mA)			0.4	V
I_{dd} (Active)		30		mA
I_{dd} (Standby)		5		uA
T_{cycle}			150	nS
C_{in} (any pin)		7		pF

*INH: 1 Mohm pull-up to V_{dd}

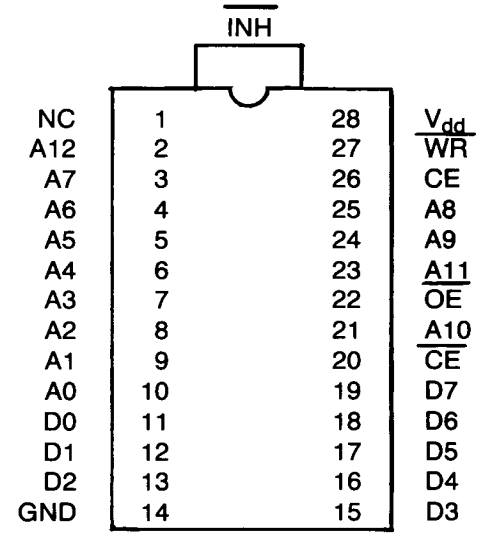
PIN DESIGNATIONS

Pin	Function
A0-A12	Address I/Ps
D0-D7	Data in/out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WR}$	Write Input
V_{dd}	+5V power
GND	Ground
$\overline{INH}$	Extra I/P

FUNCTION MODE

$\overline{INH}$	$\overline{CE}$	$\overline{OE}$	$\overline{WR}$	MODE	OUTPUT	I_{dd}
X	H	X	X	Unsel.	Hi-Z	Standby
X	L	H	H	Unsel.	Hi-Z	Active
X	L	L	H	Read	D_{out}	Active
H	L	X	L	Write	D_{in}	Active
L	L	X	L	WRITE INHIBIT		Active

PIN CONNECTIONS



REPRESENTATIVE/IMPORTER

LMS ELECTRONICS

3401 MONROE RD. • CHARLOTTE, NC 28205
(704) 376-7805, TELEX 358 905

TIMING DIAGRAMS (units — nano-seconds)

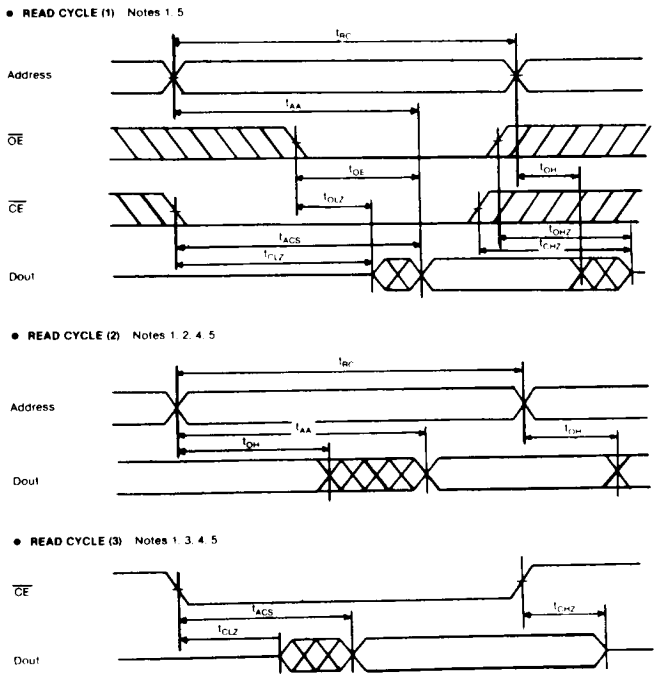
READ CYCLE

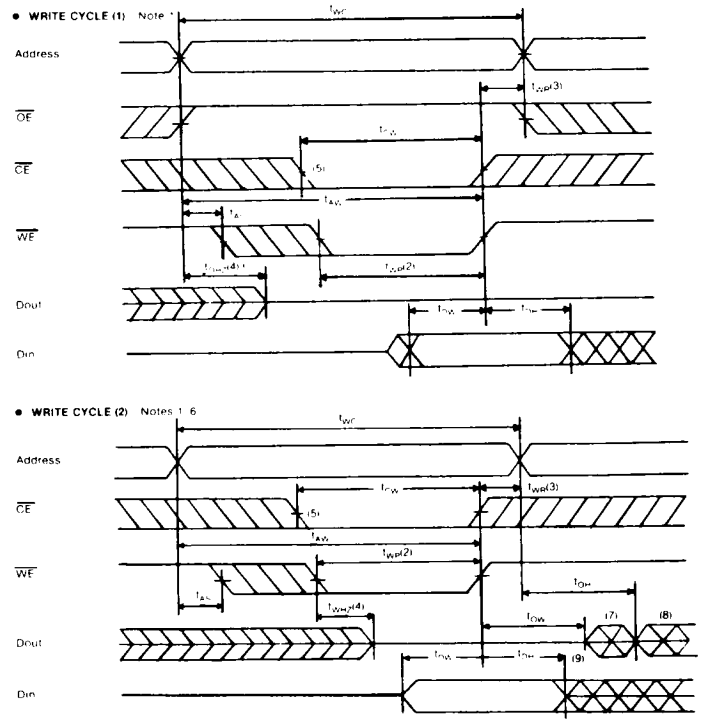
Characteristic	Label	Min	Max
Read cycle time	T_{rc}	200	
Address to O/P valid	T_{aa}		200
$\overline{CE}$ to O/P valid	T_{acs}		200
$\overline{OE}$ to O/P valid	T_{oe}		100
Output hold time	T_{oh}	20	
$\overline{CE}$ to O/P enable	T_{clz}	10	
$\overline{OE}$ to O/P enable	T_{olz}	10	
$\overline{CE}$ to O/P disable	T_{chz}	100	
$\overline{OE}$ to O/P disable	T_{ohz}	100	

(EOW = End of Write)

WRITE CYCLE

Characteristic	Label	Min	Max
Write cycle time	T_{wc}	200	
$\overline{CE}$ to EOW	T_{cw}	170	
Addr valid to EOW	T_{aw}	170	
Addr set-up time	T_{as}	0	
Write pulse width	T_{wp}	170	
$\overline{WR}$ recovery time	T_{wr}	0	
Data valid to EOW	T_{dw}	100	
Data hold time	T_{dh}	0	
$\overline{WR}$ to O/P disable	T_{whz}		100
$\overline{OE}$ from EOW	T_{ow}	20	
$\overline{OE}$ to O/P disable	T_{ohz}	0	





NOTES — READ CYCLE

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CE}$ = V_{il}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{il}.
5. When $\overline{CE}$ is low, address inputs must not be in the high impedace state.

NOTES — WRITE CYCLE

1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. T_{wr} measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to end of write cycle.
4. During this period, I/O pins are in the O/P state.
5. If a $\overline{CE}$ low transition occurs simultaneously with or after a $\overline{WE}$ transition, O/Ps remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{il}).
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CE}$ is low during this period, I/O pins are in the output state.

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