National Semiconductor

microCMOS

NSC830 ROM-I/O; NSC831 I/O Only

General Description

The NSC830 is a ROM-I/O device contained in a standard 40-pin, dual-in-line package. The chip, which is fabricated using microCMOS silicon gate technology, functions as a memory, and an input/output peripheral interface device. The memory is comprised of 16,384 bits of ROM organized as 2048 x 8. The I/O portion consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written to or read from in bytes. Several types of strobed mode operations are available through Port A.

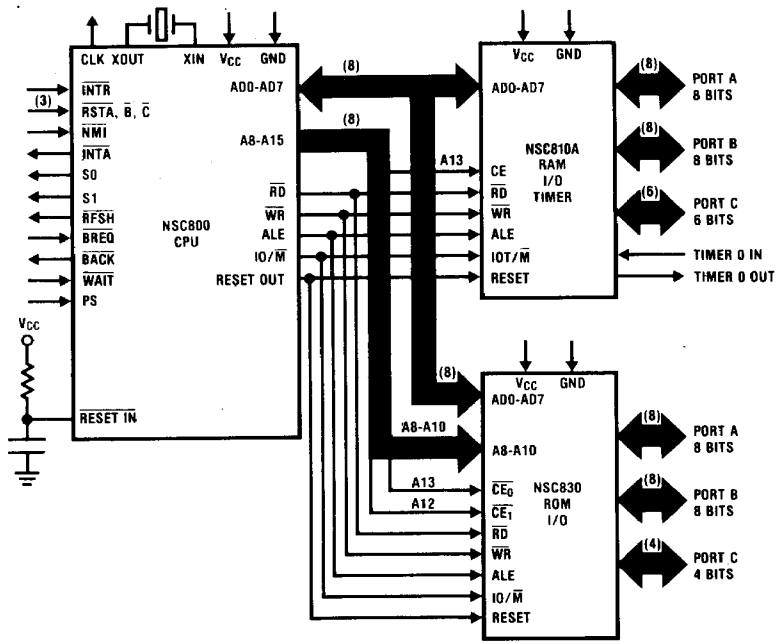
The NSC831 I/O Only is similar to the NSC830 except it has no ROM. The NSC831 is useful for prototyping work prior to ordering the NSC830, and when on-chip ROM is not required.

For military applications the NSC831 is available with class B screening in accordance with methods 5004 of MIL-STD-883.

Features

- 2K x 8 read only memory
- Three programmable I/O ports
- Single 5V Power Supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Directly compatible with NSC800 family
- Strobed modes available on Port A

Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W

Note: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Operating Range V_{CC} = 5V ± 10%

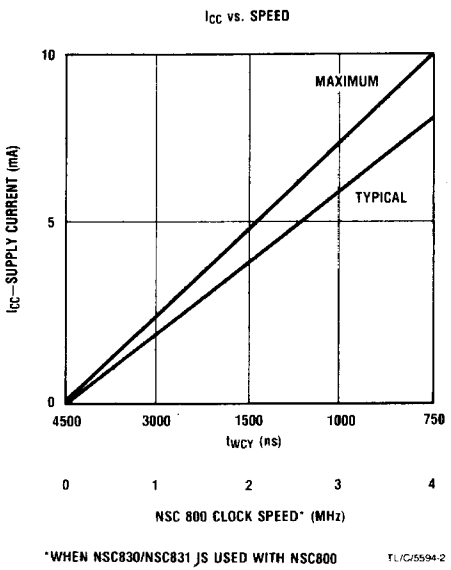
Ambient Temperature	
Military	−55°C to +125
Industrial	−40°C to +85
Commercial	0°C to +70

DC Electrical Characteristics T_A = −55°C to +125°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specif

Symbol	Parameter	Test Conditions	Min	Typ	Max	Uni
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA	2.4			V
		I_{OUT} = −10 μA	V_{CC} − 0.5			V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
		I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, t_{WCY} = 750 ns		8	10	mA
I_Q	Quiescent Current	No Input Switching, T_A = 25°C		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage		2.4	5	6	V

Low Voltage Operation Preliminary

Voltage	NSC831-1	NSC831	NSC831-4	Units
2.4	—	500	500	kHz
3.0	—	1	1	MHz



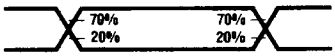
AC Electrical Characteristics

$V_{CC} = 5V \pm 10\%$, GND = 0V
Valid for the following temperature and speed:

NSC830-1, NSC831-1: 0°C to +70°C
−40°C to +85°C
NSC830, NSC831: 0°C to +70°C
−40°C to +85°C
−55°C to +125°C
NSC830-4, NSC831-4: 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

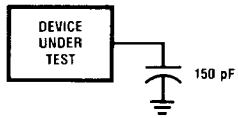
Symbol	Parameter	Test Conditions	NSC830-1 NSC831-1		NSC830 NSC831		NSC830-4 NSC831-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		300	ns
t_{AH}	AD0–AD7, CE, IOT/$\overline{M}$ Hold time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		125		75		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0–AD7, CE, IOT/$\overline{M}$ Set-Up Time		100		75		40		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		310		300	ns
t_{DS}	Data Set-Up Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Set-Up Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Output			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		220		ns
t_{RDD}	Data Bus Disable		0	100	0	100	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		75		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold With Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to INTR Output			300		300		300	ns
t_{SS}	Peripheral Data Set-Up With Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		340		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

AC Testing Input/Output Waveform



TL/C/5517-3

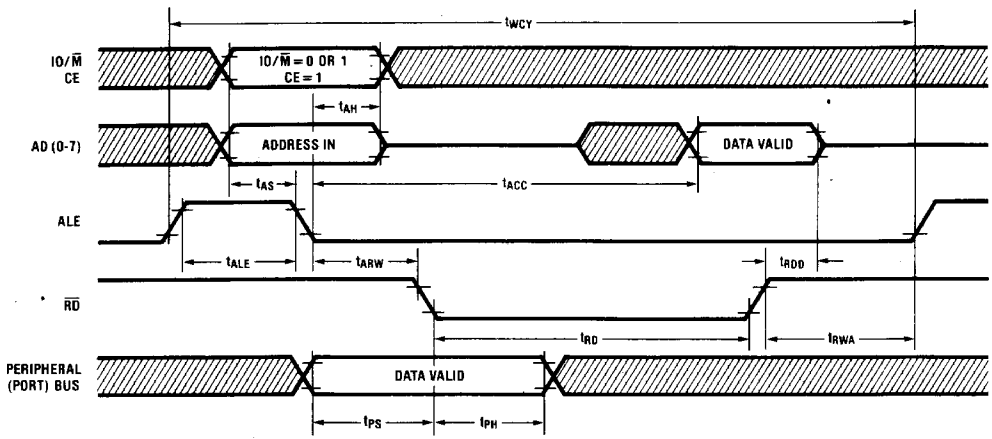
AC Testing Load Circuit



TL/C/5517-4

General Timing Waveforms

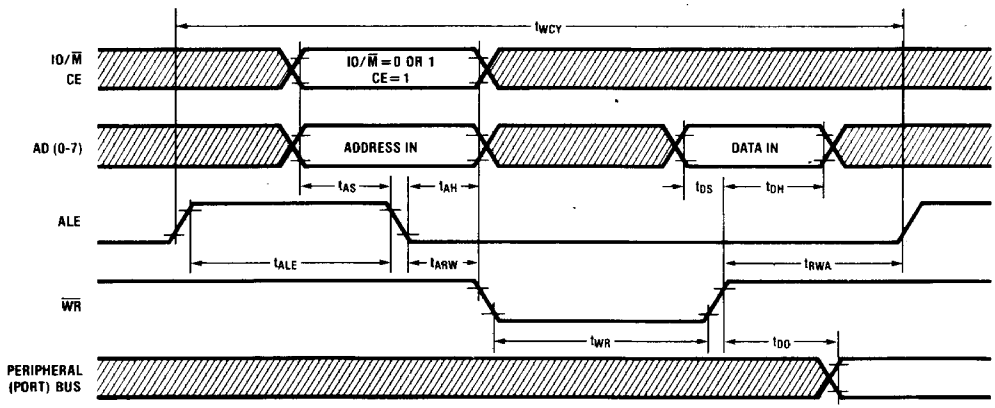
Read Cycle (Read from ROM or Port)



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-11

Write Cycle (Write to Port)

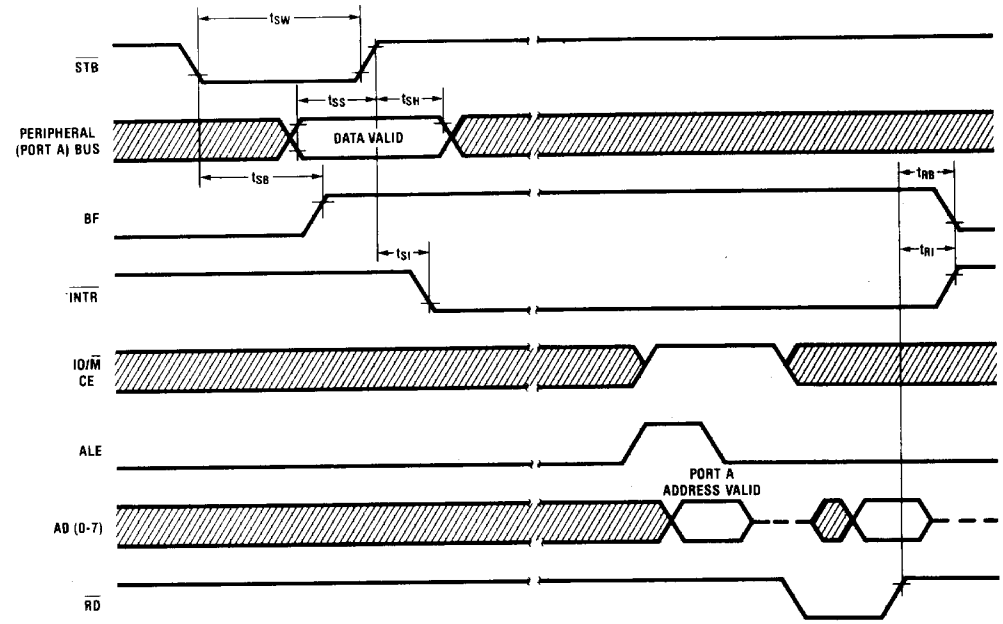


Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-12

Handshake Timing

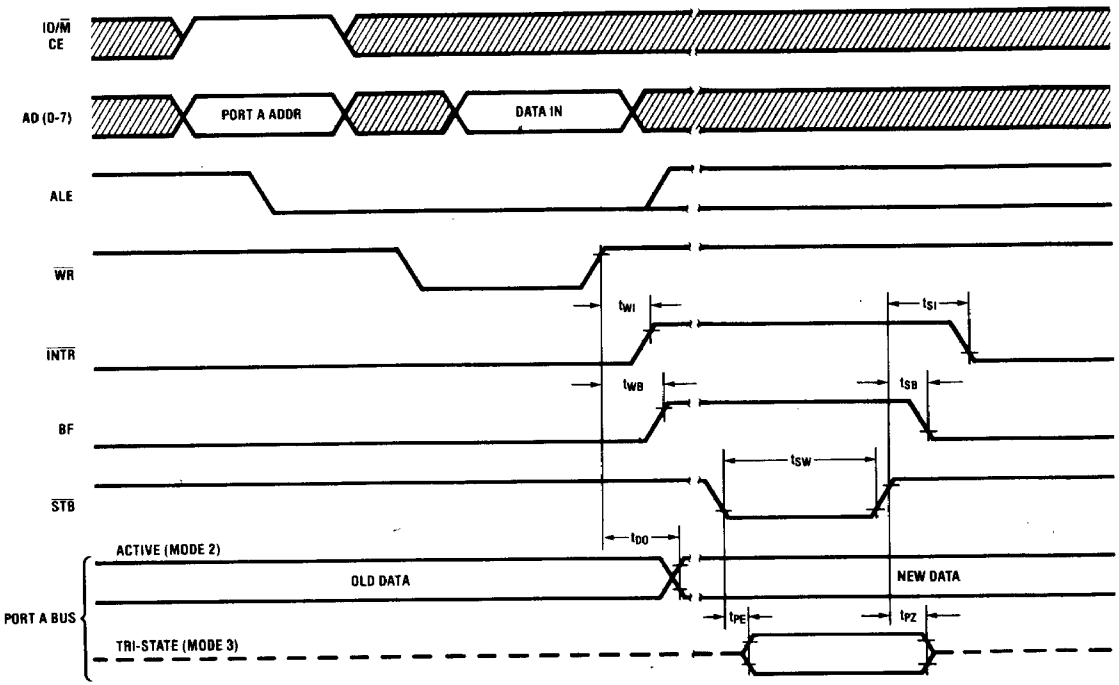
Strobed Mode Output



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-13

Strobed Mode Input



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-14

NSC830 Functional Pin Description

The following describes the function of all NSC830 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Master Reset (RESET): An active-high input on the RESET pin initializes the chip causing the three I/O ports (A, B and C) to revert to the input mode. The three ports, the three data direction registers and the mode definition register are reset to low (0).

Input/Output/Memory Select (IO/$\overline{M}$): The IO/$\overline{M}$ pin is a latched, select input line. A high (1) input selects the I/O portion of the chip; a low (0) input selects the ROM portion of the chip. The select input is latched by the trailing edge (high to low transition) of the ALE signal.

Chip Enable ($CE_0/\overline{CE_0}$, $\overline{IOR}/CE_1/\overline{CE_1}$): The chip enable inputs are mask programmable at the factory. The CE inputs permit the use of multiple NSC830s in a system without using a chip select decoder. The CE inputs must be active at the falling edge of ALE. At ALE time, the CE inputs are latched to provide access to the NSC830. The $\overline{IOR}$ input performs the same function as the combination of IO/$\overline{M}$ input high and the $\overline{RD}$ input low.

Read ($\overline{RD}$): When the $\overline{RD}$ (or the $\overline{IOR}$, when mask programmed) input is an active low, data is read from the AD0–AD7 bus. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD0–AD7 bus is in the high impedance state.

Write ($\overline{WR}$): When the CE inputs are active, and the IO/$\overline{M}$ input is high, an active low $\overline{WR}$ input causes the selected output port to be written with the data from the AD0–AD7 bus.

Address Latch Enable (ALE): The trailing edge (high to low transition) of the ALE input signal latches the address/data present on the AD0–AD7 bus, A8–A10 bus, plus the input control signals on IO/$\overline{M}$, $CE_0/\overline{CE_0}$, and $CE_1/\overline{CE_1}$.

Address Bus A8–A10: The high-order bits of the ROM address are input on this 3-bit bus and are latched by the high-to-low transition of the ALE input. These bits do not affect the I/O operations.

Power (V_{CC}): 5V power supply.

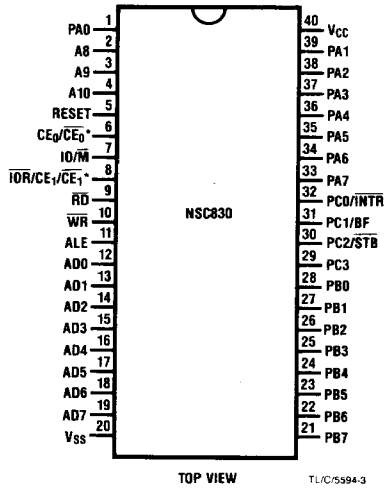
Ground (V_{SS}): Ground reference.

INPUT/OUTPUT SIGNALS

Bidirectional Address/Data Bus AD0–AD7: The lower 8 bits of the ROM or I/O address are applied to these pins, and latched by the trailing edge of ALE. During read operations, 8 bits are present on these pins, and are read when $\overline{RD}$ or $\overline{IOR}$ is low. During an I/O write cycle, Port A, B, or C is written with the data present on this bus at the trailing edge of the $\overline{WR}$ strobe.

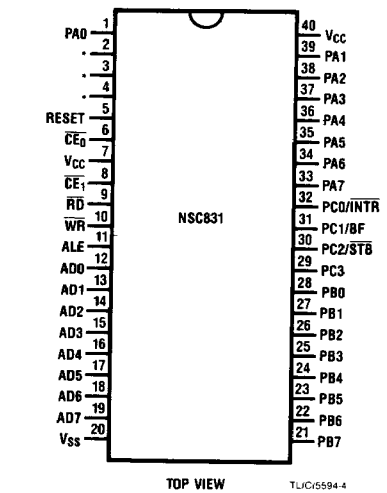
Ports A, B, C (PA0–PA7, PB0–PB7, PC0–PC3): These are general purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDRs).

Connection Diagrams



TOP VIEW TL/C/5594-3

*Pin 6 is mask programmable as CE_0 or $\overline{CE_0}$.
Pin 8 is mask programmable as $\overline{IOR}$, CE_1, or $\overline{CE_1}$.

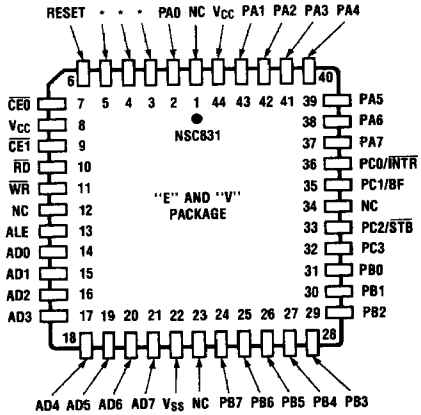


TOP VIEW TL/C/5594-4

*Tie pins 2, 3, and 4 to either V_{CC} or V_{SS}.

See NS Package D40C, J40A or N40A

Connection Diagrams (Continued)



NC = NO CONNECT

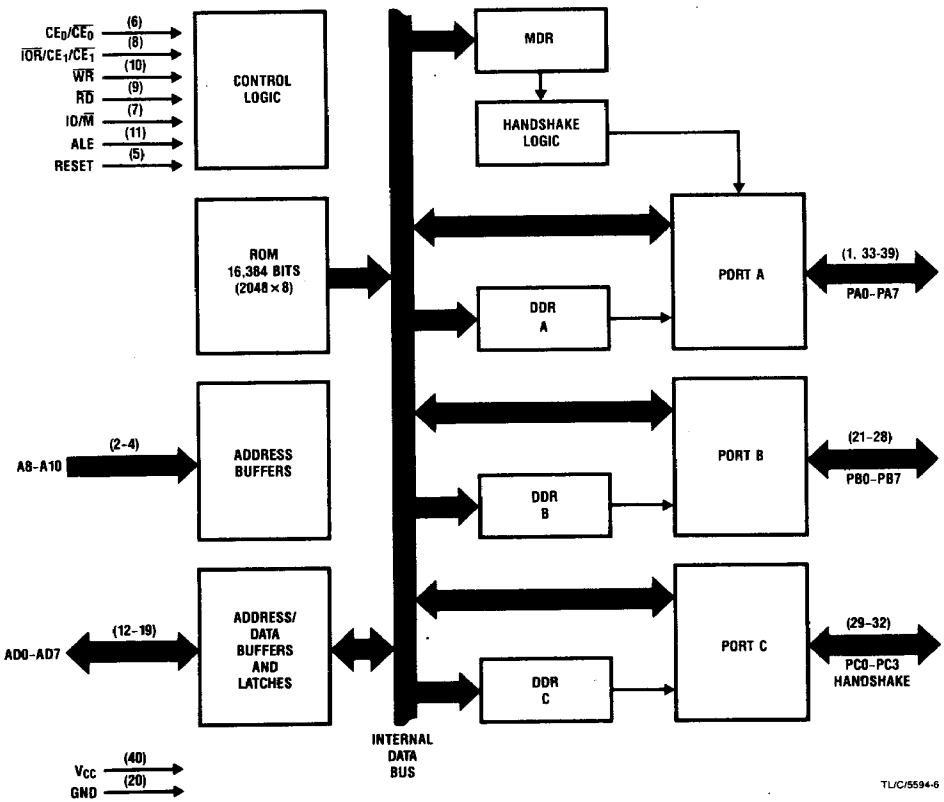
See NS Package ED44A or V44

NSC830 Functional Description

Refer to *Figure 1* for a detailed block diagram of the NSC830, while reading the following paragraphs.

Read Only Memory (ROM): The memory portion of the ROM-I/O is accessed by an 11-bit address input to pins AD0–AD7 and A8–A10. The IO/$\overline{M}$ input must be low (ROM select) and the chip enable pins in the active programmed state at the falling edge of ALE to address the ROM. Timing for ROM read and write operations is shown in the timing diagrams.

Input/Output (I/O): The I/O portion of the NSC830 contains three sets of I/O called Ports. There are two ports (A and B) which contain 8 bits each and one port (Port C) which has 4 bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (4 bits for Port C). When reading Port C, bits 4–7 will be read as ones. All ports share common functions of Read, Write, Bit-Set and Bit-Clear. Additionally, Port A is programmable for strobed (handshake) mode input or output. Port C has a programmable second function for each bit associated with strobed modes. *Table 1* defines the address location of the ports and control registers.



Note: Applicable pinout for 40-pin dual-in-line package within parentheses.

FIGURE 1. NSC830 Block Diagram

Table 1. I/O and Address Designations

8-Bit Address Field Bits 7	6	5	4	3	2	1	0	Designation I/O Port, etc.	R (Read) W (Write)
X	X	X	X	0	0	0	0	Port A (byte)	R/W
X	X	X	X	0	0	0	1	Port B (byte)	R/W
X	X	X	X	0	0	1	0	Port C (byte)	R/W
X	X	X	X	0	0	1	1	Not Used	—
X	X	X	X	0	1	0	0	DDR — Port A	W
X	X	X	X	0	1	0	1	DDR — Port B	W
X	X	X	X	0	1	1	0	DDR — Port C	W
X	X	X	X	0	1	1	1	Mode Definition Register	W
X	X	X	X	1	0	0	0	Port A — Bit Clear	W
X	X	X	X	1	0	0	1	Port B — Bit Clear	W
X	X	X	X	1	0	1	0	Port C — Bit Clear	W
X	X	X	X	1	0	1	1	Not Used	—
X	X	X	X	1	1	0	0	Port A — Bit Set	W
X	X	X	X	1	1	0	1	Port B — Bit Set	W
X	X	X	X	1	1	1	0	Port C — Bit Set	W
X	X	X	X	1	1	1	1	Not Used	—

Note: X = don't care

MODE DEFINITION REGISTER (MDR)

The Mode Definition Register (MDR) defines the operating mode for Port A. While Ports B and C are always in the basic I/O mode, there are four operating modes for Port A:

Mode 0 — Basic I/O (Input or Output)

Mode 1 — Strobed Mode Input

Mode 2 — Strobed Mode Output
- Active Peripheral Bus

Mode 3 — Strobed Mode Output
- TRI-STATE (high impedance) Peripheral Bus

The MDR has the I/O address assignment XXX00111. The bit configuration for the mode selection is illustrated below:

Mode	Bit 7	6	5	4	3	2	1	0
0	X	X	X	X	X	X	X	0
1	X	X	X	X	X	X	0	1
2	X	X	X	X	X	0	1	1
3	X	X	X	X	X	1	1	1

Note: X = don't care

DATA DIRECTION REGISTERS (DDR)

Each port bit has a data direction register (DDR) which defines the I/O state of the bit. The bit is configured as an input if a "0" is written into its DDR, or as an output if a "1" is written. The DDR bits cannot be individually written to; the entire DDR byte is affected by a write to the DDR address. Thus all data must be consistent with the direction desired for each port.

Any write or read operations on a port contradicting the DDR will not affect the port output or input. However, a read of a port bit defined as an output will cause a read from th output latch, and a write to a port bit defined as an input wi modify the output latch.

PORT FUNCTIONS — BASIC I/O

Basic I/O is the mode of operation of Ports B and C an mode 0 of Port A (defined by the MDR). Read, write, and bi operations can be executed in the basic I/O mode. The tim ing for basic input and basic output modes is shown in th AC Characteristics tables.

When a read occurs the information is latched from th peripheral bus on the leading (falling) edge of the $\overline{RD}$ strobe. When a write occurs the port bus is modified afte the trailing (rising) edge of the $\overline{WR}$ strobe with data from th AD bus. Port output data remains valid on the output pi from one trailing edge of $\overline{WR}$ strobe to the trailing edge o the next $\overline{WR}$ strobe.

BIT OPERATIONS

The I/O features of the ROM-I/O allow modification of a sin gle bit or several bits of a port with Bit-Set and Bit-Clear (see *Figure 2)*. The address is set up to indicate that a bit set (o clear) is taking place. The incoming data on the address data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing "1s" will cause the indicated operation to be performed on the corresponding port bit. All bits of the data mask with "0s" cause the corre sponding port bits to remain unchanged. Three sample operations are given, using Port B as an example:

Operation	Set B7	Bit B2 and B0	Set B4, B3 and B1
Address	XXX01101	XXX01001	XXX01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

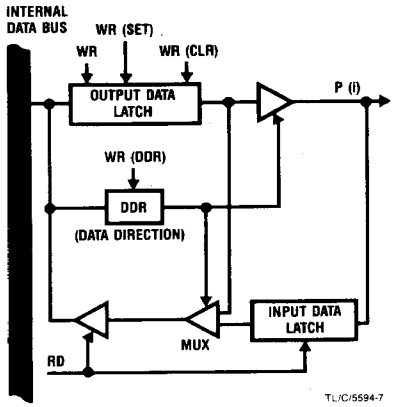


FIGURE 2. Block Diagram for Port Bit (i)

PORT A — STROBED (HANDSHAKE) MODE

Port A can be programmed (via the MDR) into one of 3 types of strobed mode for handshake communication with intelligent peripherals. When Port A is in mode 1, 2, or 3 (see description of MDR), Port C pins 0, 1, and 2 are used as signals to and from the peripheral and to the CPU, controlling handshake operations. These control signals are designated $\overline{STB}$, BF, and $\overline{INTR}$. Timing parameters and timing diagrams are detailed under AC Characteristics.

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the I/O to the CPU. In strobed input mode, the CPU reads the valid data at Port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writting to Port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving the ability to control strobed data transfer under software control. It is enabled or disabled respectively, by setting (= 1) or clearing (= 0) the output data latch of bit 2, port C. Port bit PC2 is used as the $\overline{STB}$ input. Since PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation. Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear instructions. The Port C byte write command will not alter the output data latch of the PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active-low input from the peripheral device, signaling that data transfer is about to begin. This strobe is interpreted as an "output request" if Port A is in a strobed output mode, or as a "data valid" signal if Port A is in strobed input mode.

BF (Buffer Full) is an output from the I/O to the peripheral signaling that data transfer is complete. In strobed input mode this strobe indicates that data is received into Port A and that no further data should be transmitted by the peripheral device until the port has been read (emptied). In strobed output mode the BF indicates that the request from the peripheral has been processed by the CPU and the valid data now appears in Port A.

The bits of Port C that are used for handshake control of Port A (bits C0, C1, and C2) must be direction-defined appropriately in the DDR. Also, the DDR of Port A must be consistent with the mode specified in the MDR. Register set-up configurations for the three handshake modes are illustrated in Table 2.

Table 2. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Strobed Input	XXXXXX01	00000000	XXX011	XXX1XX
Strobed Output (Active)	XXXXX011	11111111	XXX011	XXX1XX
Strobed Output (TRI-STATE)	XXXXX111	11111111	XXX011	XXX1XX

NSC831/833B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC831D and NSC831E with full class B screening per MIL-STD-883B for Military/ Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

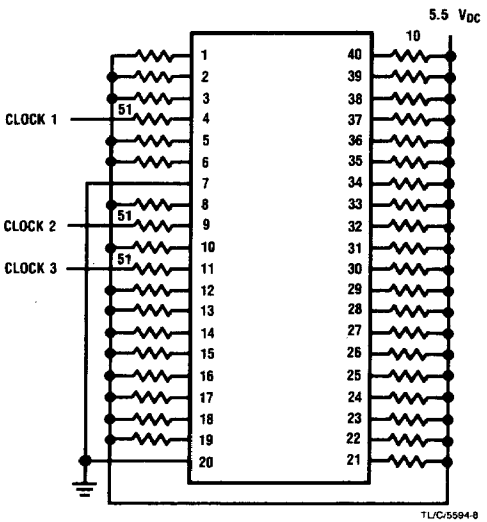
Electrical testing is performed in accordance with RET831 which tests or guarantees all of the electrical performanc characteristics of the NSC831 data sheet. A copy of the cu rent revision of RET831X is available upon request. The fo lowing table is the MIL-STD-883 flow as of the date publication.

100% SCREENING FLOW

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010B	100%
Stabilization Bake	1008C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010C 10 Cycles −65°C/+150°C	100%
Constant Acceleration	2001E 30,000 Gs, Y1 Axis	100%
Fine Leak	1014B 5×10^{-8}	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS831X	100%
PDA	10% Max	
	+125°C AC and DC per RETS831X	100%
	−55°C AC and DC per RETS831X	100%
	+25°C AC per RETS831X	100%
QA Acceptance	Group A (sample, each lot)	
Quality Conformance	Group B (sample, each inspection lot)	
	Group C (sample, every 90 days per microcircuit group)	
	Group D (sample every 6 months per package type)	
External Visual	2009	100%

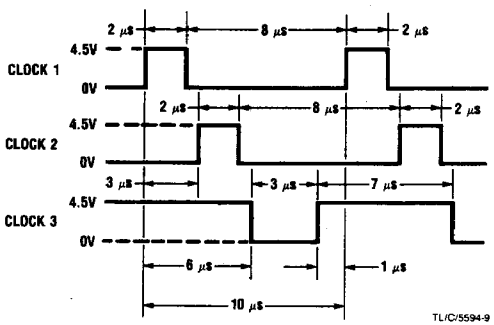
Burn-In Circuit

5243HR
NSC831D/883B (Dual In-Line)



Timing Diagram

Input Clocks



Note 1: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

Note 2: E package burn-in circuit 5556HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V

Note 5: Device to be cooled down under power after burn-in.

APPROVED FORMATS FOR CUSTOM PROGRAMMED PARTS

Input Medium:

2716 EPROM
2708 EPROM
Paper Tape

IMPORTANT — EPROM LABELING

Only one customer program may be included in a single order. The following method must be used to identify the EPROMs comprising a program.

a. The EPROMs used for storing a custom program are designated as shown:

2716:	Block A	0–2047
2708:	Block A	0–1023
	Block B	1024–2047

b. All EPROMs must be labeled (stickers, paint, etc.) with this block designation plus a customer assigned print or identification number.

Example:

1. Customer Data
   - Custom Program Length — 2K
   - Medium — Two 2708s
   - Customer Print or I.D. No. C123-45
2. EPROM Labels

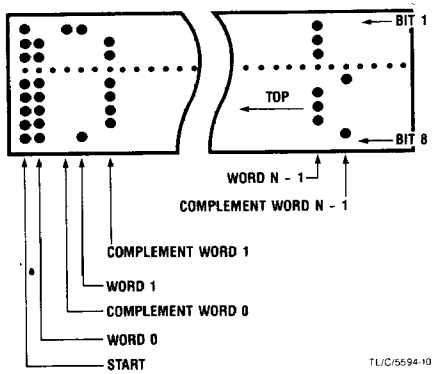
C123-45 A 0–1023	C123-45 B 1024–2047

Paper Tape

Tapes may only be submitted in binary complement format. The following information should be written on the paper tape.

Company Name
Customer Print or I.D. No.
NSC Part No.
A Punch = ("1" or "0")
This is _____ logic (POS or NEG)

BINARY COMPLEMENT FORMAT



Note 1: Tape must be blank except for the data words.

Note 2: Tape must start with a rubout character.

Note 3: Data is comprised of two words, the first being the actual data and the second being the complement of the data.

Verification

You will receive a listing of the options ordered and the input data. If you also wish to receive EPROMs for verification, please send additional blank EPROMs as necessary for this purpose. You can use software (the listing) or hardware (EPROMs) to verify the program.

You will be asked for a GO/NO GO response within one week after you receive the listing.

VERIFICATION LISTING

The verification listing has six sections:

1. A cover sheet with provision for "STOP, DO NOT PROCEED" or "VERIFICATION CERTIFIED" signatures.
2. Description of the options you have chosen.
3. A description of the log designations and assumptions used to process the data.
4. A listing of the data you have submitted.
5. An error summary.
6. A definition of the standard logic definitions for the ROM and the reduced form of the data. This list shows the output word corresponding to each address coded in binary.

ORDERING INFORMATION FOR CUSTOM PROGRAMMED PARTS

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information.

Person (Customer, Sales Representative, etc.) to whom Verification Package be sent:	NATIONAL PART NUMBER AND PACKAGE
Name	ROM Letter Code (National Use Only)
Company	Customer Name and Location
Address	Customer Print or I.D. Number for this ROM Program
City, State, and Zip Code	Purchase Order Number
Person (Customer) NS Can Contact for Technical Questions	Device Marking Instruction (Unless otherwise instructed, NS will always mark devices with Date Code, National Part No., and ROM Code. Any additional marking should be shown below.)
Telephone Number	
Sales Representative	Customer Service Representative

INPUT MEDIUM

See following page for approved formats. Please check the medium you are using.

- ☐ Paper Tape
- ☐ 2716 EPROM
- ☐ 2708 EPROM

_____Total number of EPROMs

OPTIONS FOR NSC830 ROM — I/O

Option 1 = ☐

CE_0 Select, enter: 0 for CE_0
1 for CE_0

Option 2 = ☐

CE_1/IOR Select, enter: 0 for IOR
1 for CE_1
2 for CE_1

Ordering Information

NSC830XXX X X X X

- **/A+ = A+ Reliability Screening**
- **I = Industrial Temperature (−40°C to +85°C)**
  M = Military Temperature (−55°C to = +125°C)
  No Designation = Commercial Temperature (0°C to +70°C)
- **−1 = 1 MHz Clock Output (Note 1)**
  −4 = 4 MHz Clock Output
  No Designation = 2.5 MHz Clock Output
- **D = Ceramic Package**
  J = Cerdip Package (Availability to be announced)
  N = Plastic Package
  E = Ceramic Leadless Chip Carrier (LCC)
  V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)
- **Unique ROM code (Alpha characters assigned by National)**

Note 1: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I

Examples
NSC830XXX/N
NSC830XXX/E−4/A+

Reliability Information (NSC830)

Gate Count*	2150 (min)
	2278 (max)
Transistor Count*	8500 (min)
	24,884 (max)

*Dependent on ROM program size.

Ordering Information

NSC831 X X X X

- **/A+ = A+ Reliability Screening**
  /883 = MIL-STD-883B Screening (Note 1)
- **I = Industrial Temperature (−40°C to +85°C)**
  M = Military Temperature (−55°C to = +125°C)
  No Designation = Commercial Temperature (0°C to +70°C)
- **−1 = 1 MHz Clock Output (Note 2)**
  −4 = 4 MHz Clock Output
  No Designation = 2.5 MHz Clock Output
- **D = Ceramic Package**
  J = Cerdip Package (Availability to be announced)
  N = Plastic Package
  E = Ceramic Leadless Chip Carrier (LCC)
  V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)

Note 1: Do not specify a temperature option: all parts are screened to military temperature.
Note 2: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I.

Examples
NSC831E-4/883
NSC831N
NSC831D-1I/A+

Reliability Information (NSC831)

Gate Count	1900
Transistor Count	7400