MICRON TECHNOLOGY, INC.

**MT4LDT164H(X)(L), MT8LDT264H(X)(L)**
**1 MEG, 2 MEG x 64 DRAM MODULES**

# SMALL-OUTLINE DRAM MODULE

# 1 MEG, 2 MEG x 64

8, 16 MEGABYTE, 3.3V, OPTIONAL EXTENDED REFRESH, FAST PAGE OR EDO PAGE MODE

## FEATURES

- JEDEC- and industry-standard pinout in a 144-pin, small-outline, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 24mW standby; 1,012mW active, typical (16MB)
- Refresh modes: RAS# ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN; optional Extended CBR
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode
- Serial Presence-Detect (SPD)

## OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - 144-pin Small-Outline DIMM (gold) — G
- Operating Modes
  - FAST PAGE MODE — Blank
  - EDO PAGE MODE — X
- Refresh
  - Standard/16ms — Blank
  - Extended Refresh/128ms — L

## KEY TIMING PARAMETERS

EDO Operating Mode

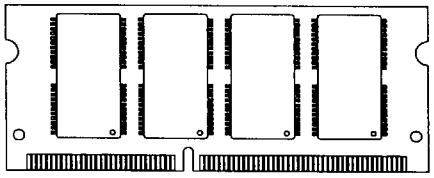
| SPEED | tRC | tRAC | tPC | tAA | tCAC | tCAS |
|---|---|---|---|---|---|---|
| -6 | 105ns | 60ns | 25ns | 30ns | 15ns | 12ns |
| -7 | 125ns | 70ns | 30ns | 35ns | 20ns | 12ns |

FPM Operating Mode

| SPEED | tRC | tRAC | tPC | tAA | tCAC | tRP |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |
| -7 | 130ns | 70ns | 40ns | 35ns | 20ns | 50ns |

## PIN ASSIGNMENT (Front View)

### 144-Pin Small-Outline DIMM



| PIN # | FRONT | PIN # | BACK | PIN # | FRONT | PIN # | BACK |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 2 | Vss | 73 | OE# | 74 | RFU |
| 3 | DQ0 | 4 | DQ32 | 75 | Vss | 76 | Vss |
| 5 | DQ1 | 6 | DQ33 | 77 | RSVD | 78 | RSVD |
| 7 | DQ2 | 8 | DQ34 | 79 | RSVD | 80 | RSVD |
| 9 | DQ3 | 10 | DQ35 | 81 | Vcc | 82 | Vcc |
| 11 | Vcc | 12 | Vcc | 83 | DQ16 | 84 | DQ48 |
| 13 | DQ4 | 14 | DQ36 | 85 | DQ17 | 86 | DQ49 |
| 15 | DQ5 | 16 | DQ37 | 87 | DQ18 | 88 | DQ50 |
| 17 | DQ6 | 18 | DQ38 | 89 | DQ19 | 90 | DQ51 |
| 19 | DQ7 | 20 | DQ39 | 91 | Vss | 92 | Vss |
| 21 | Vss | 22 | Vss | 93 | DQ20 | 94 | DQ52 |
| 23 | CAS0# | 24 | CAS4# | 95 | DQ21 | 96 | DQ53 |
| 25 | CAS1# | 26 | CAS5# | 97 | DQ22 | 98 | DQ54 |
| 27 | Vcc | 28 | Vcc | 99 | DQ23 | 100 | DQ55 |
| 29 | A0 | 30 | A3 | 101 | Vcc | 102 | Vcc |
| 31 | A1 | 32 | A4 | 103 | A6 | 104 | A7 |
| 33 | A2 | 34 | A5 | 105 | A8 | 106 | RSVD |
| 35 | Vss | 36 | Vss | 107 | Vss | 108 | Vss |
| 37 | DQ8 | 38 | DQ40 | 109 | A9 | 110 | RSVD |
| 39 | DQ9 | 40 | DQ41 | 111 | A10 | 112 | RSVD |
| 41 | DQ10 | 42 | DQ42 | 113 | Vcc | 114 | Vcc |
| 43 | DQ11 | 44 | DQ43 | 115 | CAS2# | 116 | CAS6# |
| 45 | Vcc | 46 | Vcc | 117 | CAS3# | 118 | CAS7# |
| 47 | DQ12 | 48 | DQ44 | 119 | Vss | 120 | Vss |
| 49 | DQ13 | 50 | DQ45 | 121 | DQ24 | 122 | DQ56 |
| 51 | DQ14 | 52 | DQ46 | 123 | DQ25 | 124 | DQ57 |
| 53 | DQ15 | 54 | DQ47 | 125 | DQ26 | 126 | DQ58 |
| 55 | Vss | 56 | Vss | 127 | DQ27 | 128 | DQ59 |
| 57 | RSVD | 58 | RSVD | 129 | Vcc | 130 | Vcc |
| 59 | RSVD | 60 | RSVD | 131 | DQ28 | 132 | DQ60 |
| 61 | RFU | 62 | RFU | 133 | DQ29 | 134 | DQ61 |
| 63 | Vcc | 64 | Vcc | 135 | DQ30 | 136 | DQ62 |
| 65 | RFU | 66 | RFU | 137 | DQ31 | 138 | DQ63 |
| 67 | WE# | 68 | RFU | 139 | Vss | 140 | Vss |
| 69 | RAS0# | 70 | RFU | 141 | SDA | 142 | SCL |
| 71 | RAS1#* | 72 | RFU | 143 | Vcc | 144 | Vcc |

*16MB version only

## PART NUMBERS

EDO Operating Mode

| PART NUMBER | DESCRIPTION |
|---|---|
| MT4LDT164HG-xx X | 1 Meg x 64, EDO |
| MT4LDT164HG-xx XL | 1 Meg x 64, EDO, Extended Refresh |
| MT8LDT264HG-xx X | 2 Meg x 64, EDO |
| MT8LDT264HG-xx XL | 2 Meg x 64, EDO, Extended Refresh |

xx = speed

FPM Operating Mode

| PART NUMBER | DESCRIPTION |
|---|---|
| MT4LDT164HG-xx | 1 Meg x 64 |
| MT4LDT164HG-xx L | 1 Meg x 64, Extended Refresh |
| MT8LDT264HG-xx | 2 Meg x 64 |
| MT8LDT264HG-xx L | 2 Meg x 64, Extended Refresh |

xx = speed

## GENERAL DESCRIPTION

The MT4LDT164H(X)(L) and MT8LDT264H(X)(L) are randomly accessed 8MB and 16MB solid-state memories organized in a small outline x64 configuration. They are specially processed to operate from +3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

## FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS#, followed by a column-address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

## EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time ($^{t}$CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH (reference MT4LC1M16E5 DRAM data sheet for additional information on EDO functionality).

## REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A9) are executed at least every $^{t}$REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

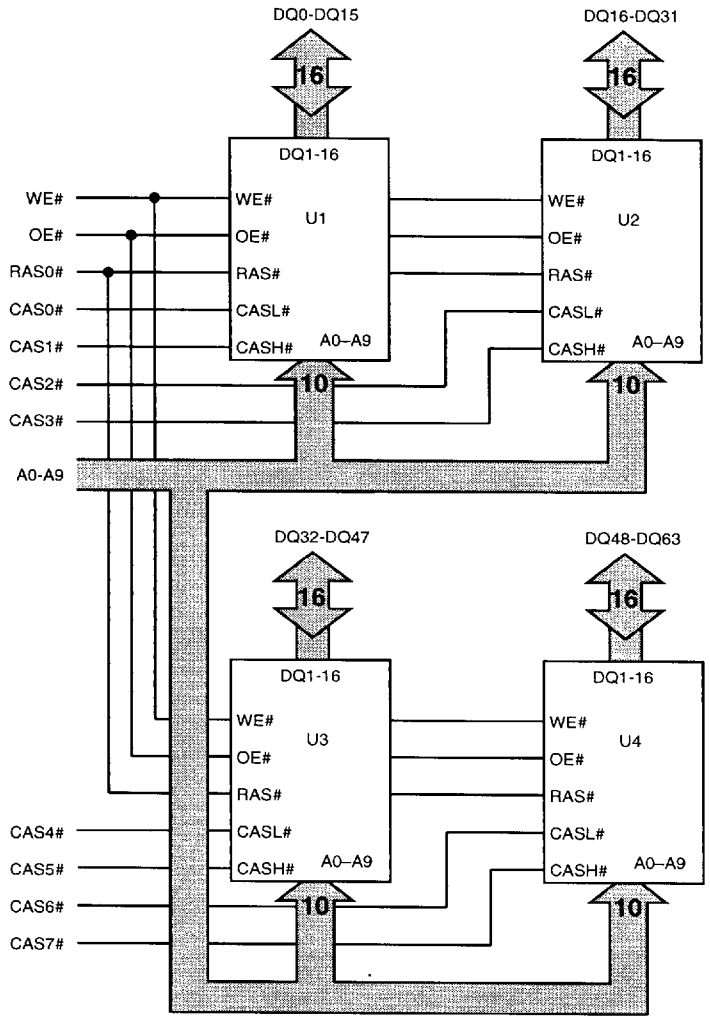
## STANDBY

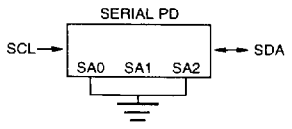
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

## SERIAL PRESENCE-DETECT EEPROM

This module incorporates Serial Presence Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains data programmed by Micron that identifies the module type and various DRAM organization and timing parameters. System READ/WRITE operations to the EEPROM device occur via a standard $I^2C$ bus using the DIMM's SCL (clock) and SDA (data) signals. The EEPROM device operates with a Vcc of 3.3V ±0.3V.

## FUNCTIONAL BLOCK DIAGRAM
## MT4LDT164H (8MB)

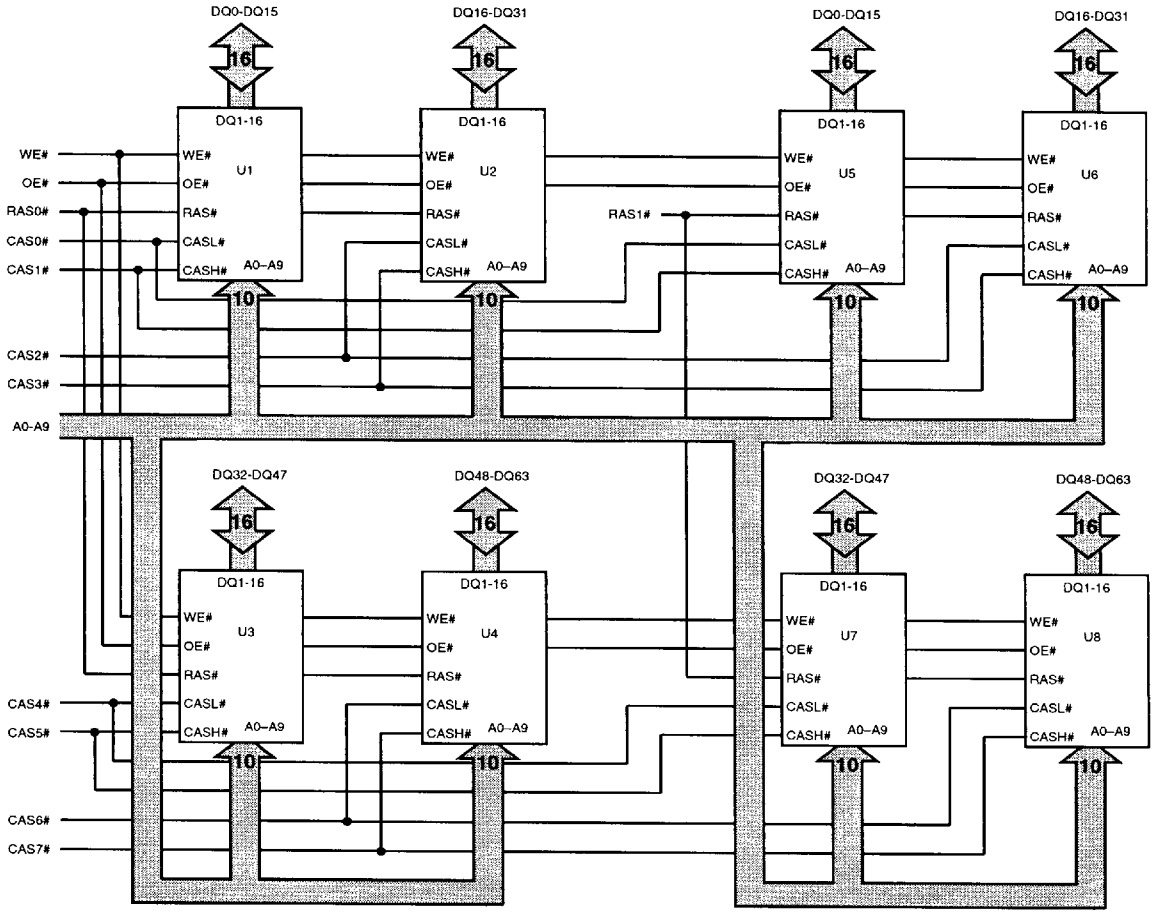


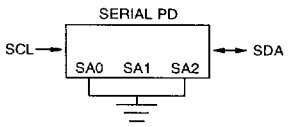




1 Meg x 64 - MT4LDT164HG(L)
U1-U4 = MT4LC1M16C3(L) FAST PAGE MODE

1 Meg x 64 - MT4LDT164HG X(L)
U1-U4 = MT4LC1M16E5(L) EDO PAGE MODE

## FUNCTIONAL BLOCK DIAGRAM
## MT8LDT264H (16MB)




2 Meg x 64 - MT8LDT264HG(L)
U1-U8 = MT4LC1M16C3(L) FAST PAGE MODE

2 Meg x 64 - MT8LDT264HG X(L)
U1-U8 = MT4LC1M16E5(L) EDO PAGE MODE

## SERIAL PRESENCE-DETECT EEPROM
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) ($V_{CC}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.6 | V | |
| Input High (Logic 1) Voltage, all inputs | $V_{IH}$ | $V_{CC} \times .7$ | $V_{CC} \times .5$ | V | |
| Input Low (Logic 0) Voltage, all inputs | $V_{IL}$ | -1.0 | $V_{CC} \times .3$ | V | |
| OUTPUT LOW VOLTAGE, $I_{OUT}$ = 3mA | $V_{OL}$ | | 0.4 | V | |
| INPUT LEAKAGE CURRENT, $V_{IN}$ = GND to $V_{CC}$ | $I_{LI}$ | | 10 | µA | |
| OUTPUT LEAKAGE CURRENT, $V_{OUT}$ = GND to $V_{CC}$ | $I_{LO}$ | | 10 | µA | |
| STANDBY CURRENT<br>SCL = SDA = $V_{CC}$ -0.3V, All other inputs = GND or $V_{CC}$ 3.3V +10% | $I_{SB}$ | | 30 | µA | |
| POWER SUPPLY CURRENT<br>SCL clock frequency = 100 KHz | $I_{CC}$ | | 2 | mA | |

## SERIAL PRESENCE-DETECT EEPROM
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
| SCL LOW to SDA data-out valid | $t_{AA}$ | 0.3 | 3.5 | µs | |
| Time the bus must be free before a new transition can start | $t_{BUF}$ | 4.7 | | µs | |
| Data-out hold time | $t_{DH}$ | 300 | | ns | |
| SDA and SCL fall time | $t_F$ | | 300 | ns | |
| Data-in hold time | $t_{HD:DAT}$ | 0 | | µs | |
| Start condition hold time | $t_{HD:STA}$ | 4 | | µs | |
| Clock HIGH period | $t_{HIGH}$ | 4 | | µs | |
| Noise suppression time constant at SCL, SDA inputs | $t_I$ | | 100 | ns | |
| Clock LOW period | $t_{LOW}$ | 4.7 | | µs | |
| SDA and SCL rise time | $t_R$ | | 1 | µs | |
| SCL clock frequency | $t_{SCL}$ | | 100 | KHz | |
| Data-in setup time | $t_{SU:DAT}$ | 250 | | ns | |
| Start condition setup time | $t_{SU:STA}$ | 4.7 | | µs | |
| Stop condition setup time | $t_{SU:STO}$ | 4.7 | | µs | |
| WRITE cycle time | $t_{WR}$ | | 10 | ms | 32 |

## SERIAL PRESENCE-DETECT MATRIX

| | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|
| **BYTE 0: NUMBER OF BYTES USED BY MICRON** | | | | | | | | |
| 128 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **BYTE 1: TOTAL NUMBER OF SPD MEMORY BYTES** | | | | | | | | |
| 256 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **BYTE 2: MEMORY TYPE** | | | | | | | | |
| FAST PAGE MODE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| EDO PAGE MODE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **BYTE 3: NUMBER OF ROW ADDRESSES** | | | | | | | | |
| 10 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| **BYTE 4: NUMBER OF COLUMN ADDRESSES** | | | | | | | | |
| 10 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| **BYTE 5: NUMBER OF BANKS** | | | | | | | | |
| 1 (1 Meg x 64) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 (2 Meg x 64) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **BYTE 6: DATA WIDTH** | | | | | | | | |
| x64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| **BYTE 7: DATA WIDTH (continued)** | | | | | | | | |
| NONE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **BYTE 8: VOLTAGE INTERFACE** | | | | | | | | |
| LVTTL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **BYTE 9: RAS# ACCESS TIME** | | | | | | | | |
| 60ns | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 70ns | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| **BYTE 10: CAS# ACCESS TIME** | | | | | | | | |
| 10ns | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 12ns | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| **BYTE 11: MODULE CONFIGURATION TYPE** | | | | | | | | |
| NON-PARITY | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **BYTE 12: REFRESH RATES** | | | | | | | | |
| NORMAL (15.625µs) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EXTENDED (8X - 125µs) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH" / "driven to LOW."

## TRUTH TABLE

| FUNCTION | | RAS# | CAS# | WE# | ADDRESSES | | DATA-IN/OUT |
|---|---|---|---|---|---|---|---|
| | | | | | $^tR$ | $^tC$ | DQ0-DQ63 |
| Standby | | H | H→X | X | X | X | High-Z |
| READ | | L | L | H | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | ROW | COL | Data-In |
| EDO/FAST-PAGE-MODE READ | 1st Cycle | L | H→L | H | ROW | COL | Data-Out |
| | 2nd Cycle | L | H→L | H | n/a | COL | Data-Out |
| EDO/FAST-PAGE-MODE WRITE | 1st Cycle | L | H→L | L | ROW | COL | Data-In |
| | 2nd Cycle | L | H→L | L | n/a | COL | Data-In |
| RAS#-ONLY REFRESH | | L | H | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | High-Z |
| Extended CBR REFRESH (L version) | | H→L | L | H | X | X | High-Z |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ supply relative to $V_{SS}$ ..... -1V to +4.6V
Voltage on Inputs or I/O pins
relative to $V_{SS}$ ..... -1V to +5.5V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation ..... 4W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) ($V_{CC}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | 3.0 | 3.6 | V | |
| Input High (Logic 1) Voltage, all inputs | | $V_{IH}$ | 2.0 | 5.5 | V | |
| Input Low (Logic 0) Voltage, all inputs | | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT | RAS0#-1# | $I_{I1}$ | -8 | 8 | µA | |
| Any input 0V ≤ $V_{IN}$ ≤ 5.5V | A0-A9,WE#,OE# | $I_{I2}$ | -16 | 16 | µA | 25 |
| (All other pins not under test = 0V) for each package input | CAS0#-CAS7# | $I_{I3}$ | -4 | 4 | µA | 25 |
| OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ $V_{OUT}$ ≤ 5.5V) for each package input | DQ0-DQ63 | $I_{OZ}$ | -20 | 20 | µA | 25 |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -2mA) | | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 2mA) | | $V_{OL}$ | | 0.4 | V | |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) (Vcc = +3.3V ±0.3V)

| | | | MAX | | | |
|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | SIZE | -6 | -7 | UNITS | NOTES |
| STANDBY CURRENT: (TTL)<br>(RAS# = CAS# = $V_{IH}$) | $I_{CC1}$ | 8MB<br>16MB | 8<br>16 | 8<br>16 | mA | |
| STANDBY CURRENT: (CMOS)<br>(RAS# = CAS# = $V_{CC}$ -0.2V) | $I_{CC2}$ | 8MB<br>16MB | 2<br>4 | 2<br>4 | mA | 28 |
| | $I_{CC2}$<br>(L only) | 8MB<br>16MB | 0.6<br>1.2 | 0.6<br>1.2 | mA | |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS#, CAS#, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | 8MB<br>16MB | 680<br>688 | 620<br>628 | mA | 3, 24 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, Address Cycling: tPC = tPC [MIN];<br>$^tCP$, $^tASC$ = 10ns) | $I_{CC4}$ | 8MB<br>16MB | 400<br>408 | 360<br>368 | mA | 3, 24 |
| OPERATING CURRENT: EDO PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, Address Cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC5}$<br>(X only) | 8MB<br>16MB | 480<br>488 | 440<br>448 | mA | 3, 24 |
| REFRESH CURRENT: RAS# ONLY<br>Average power supply current<br>(RAS# Cycling, CAS# = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | 8MB<br>16MB | 640<br>648 | 580<br>588 | mA | 3, 24 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>(RAS#, CAS#, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC7}$ | 8MB<br>16MB | 600<br>608 | 560<br>568 | mA | 3, 4 |
| REFRESH CURRENT: Extended (L-version only)<br>Average power supply current during Extended Refresh:<br>CAS# = 0.2V or CBR cycling; RAS# = $^tRAS$ (MIN);<br>WE# = Vcc -0.2V; A0-A9 and $D_{IN}$ = Vcc -0.2V or 0.2V ($D_{IN}$ may be left open); $^tRC$ = 125µs (1024 rows at 125µs = 128ms) | $I_{CC8}$<br>(L only) | 8MB<br>16MB | 1.2<br>2.4 | 1.2<br>2.4 | mA | 3, 4 |

## CAPACITANCE

| PARAMETER | SYMBOL | 8MB | 16MB | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A9 | $C_{I1}$ | 24 | 46 | pF | 2 |
| Input Capacitance: WE#, OE# | $C_{I2}$ | 32 | 62 | pF | 2 |
| Input Capacitance: RAS0# - RAS1# | $C_{I3}$ | 32 | 32 | pF | 2 |
| Input Capacitance: CAS0# - CAS7# | $C_{I4}$ | 10 | 20 | pF | 2 |
| Input/Output Capacitance: DQ0-DQ63 | $C_{IO1}$ | 10 | 18 | pF | 2 |
| Input/Output Capacitance: SDA, SCL | $C_{IO2}$ | 10 | 10 | pF | |

## FAST PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS - FAST PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column-address | $^tAA$ | | 30 | | 35 | ns | |
| Column-address hold time (referenced to RAS#) | $^tAR$ | 50 | | 55 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | ns | |
| Row-address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Column-address to WE# delay time | $^tAWD$ | 55 | | 60 | | ns | 20 |
| Access time from CAS# | $^tCAC$ | | 15 | | 20 | ns | 14 |
| Column-address hold time | $^tCAH$ | 10 | | 15 | | ns | |
| CAS# pulse width | $^tCAS$ | 15 | 10,000 | 20 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | $^tCHR$ | 15 | | 15 | | ns | 4 |
| Last CAS# going LOW to first CAS# to return HIGH | $^tCLCH$ | 10 | | 10 | | ns | 33 |
| CAS# to output in Low-Z | $^tCLZ$ | 3 | | 3 | | ns | 23 |
| CAS# precharge time | $^tCP$ | 10 | | 10 | | ns | 15 |
| Access time from CAS# precharge | $^tCPA$ | | 35 | | 40 | ns | |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | 5 | | ns | |
| CAS# hold time | $^tCSH$ | 60 | | 70 | | ns | |
| CAS# setup time (CBR REFRESH) | $^tCSR$ | 5 | | 5 | | ns | 4 |
| CAS# to WE# delay time | $^tCWD$ | 40 | | 45 | | ns | 20, 29 |
| Write command to CAS# lead time | $^tCWL$ | 15 | | 20 | | ns | |
| Data-in hold time | $^tDH$ | 10 | | 15 | | ns | 20 |
| Data-in hold time (referenced to RAS#) | $^tDHR$ | 45 | | 55 | | ns | |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 20 |
| Output disable | $^tOD$ | 3 | 15 | 3 | 20 | ns | 27, 28, 39 |
| Output enable | $^tOE$ | | 15 | | 20 | ns | 32 |
| OE# hold time from WE# during READ-MODIFY-WRITE cycle | $^tOEH$ | 15 | | 20 | | ns | 27 |
| Output buffer turn-off delay | $^tOFF$ | 3 | 15 | 3 | 20 | ns | 19, 23 |
| OE# setup prior to RAS# during HIDDEN REFRESH cycle | $^tORD$ | 0 | | 0 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 35 | | 40 | | ns | |
| Access time from RAS# | $^tRAC$ | | 60 | | 70 | ns | 13 |
| RAS# to column-address delay time | $^tRAD$ | 15 | 30 | 15 | 35 | ns | 17 |
| Row-address hold time | $^tRAH$ | 10 | | 10 | | ns | |
| Column-address to RAS# lead time | $^tRAL$ | 30 | | 35 | | ns | |

## FAST PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

| AC CHARACTERISTICS - FAST PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| RAS# pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | ns | |
| RAS# pulse width (FAST PAGE MODE) | tRASP | 60 | 100,000 | 70 | 100,000 | ns | |
| Random READ or WRITE cycle time | tRC | 110 | | 130 | | ns | |
| RAS# to CAS# delay time | tRCD | 20 | 45 | 20 | 50 | ns | 16 |
| Read command hold time (referenced to CAS#) | tRCH | 0 | | 0 | | ns | 18 |
| Read command setup time | tRCS | 0 | | 0 | | ns | |
| Refresh period (1,024 cycles) | tREF | | 16 | | 16 | ms | |
| Refresh period (1,024 cycles) L version | tREF | | 128 | | 128 | ms | |
| RAS# precharge time | tRP | 40 | | 50 | | ns | |
| RAS# to CAS# precharge time | tRPC | 0 | | 0 | | ns | |
| Read command hold time (referenced to RAS#) | tRRH | 0 | | 0 | | ns | 18 |
| RAS# hold time | tRSH | 15 | | 20 | | ns | |
| READ WRITE cycle time | tRWC | 150 | | 180 | | ns | |
| RAS# to WE# delay time | tRWD | 85 | | 95 | | ns | 20 |
| Write command to RAS# lead time | tRWL | 15 | | 20 | | ns | |
| Transition time (rise or fall) | tT | 3 | 50 | 3 | 50 | ns | |
| Write command hold time | tWCH | 10 | | 15 | | ns | |
| Write command hold time (referenced to RAS#) | tWCR | 45 | | 55 | | ns | |
| WE# command setup time | tWCS | 0 | | 0 | | ns | |
| Write command pulse width | tWP | 10 | | 15 | | ns | |
| WE# hold time (CBR REFRESH) | tWRH | 10 | | 10 | | ns | |
| WE# setup time (CBR REFRESH) | tWRP | 10 | | 10 | | ns | |

## EDO PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

| AC CHARACTERISTICS - EDO PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column-address | tAA | | 30 | | 35 | ns | |
| Column-address setup to CAS# precharge during WRITE | tACH | 15 | | 15 | | ns | |
| Column-address hold time (referenced to RAS#) | tAR | 45 | | 55 | | ns | |
| Column-address setup time | tASC | 0 | | 0 | | ns | |
| Row-address setup time | tASR | 0 | | 0 | | ns | |
| Column-address to WE# delay time | tAWD | 55 | | 60 | | ns | 13 |
| Access time from CAS# | tCAC | | 15 | | 20 | ns | 14 |
| Column-address hold time | tCAH | 10 | | 12 | | ns | |
| CAS# pulse width | tCAS | 10 | 10,000 | 12 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | tCHR | 10 | | 12 | | ns | 4 |
| Last CAS# going LOW to first CAS# to return HIGH | tCLCH | 10 | | 10 | | ns | 29 |
| CAS# to output in Low-Z | tCLZ | 0 | | 0 | | ns | |
| Data output hold after next CAS# LOW | tCOH | 3 | | 3 | | ns | |
| CAS# precharge time | tCP | 10 | | 10 | | ns | 15 |
| Access time from CAS# precharge | tCPA | | 35 | | 40 | ns | |
| CAS# to RAS# precharge time | tCRP | 5 | | 5 | | ns | |
| CAS# hold time | tCSH | 50 | | 55 | | ns | |
| CAS# setup time (CBR REFRESH) | tCSR | 5 | | 5 | | ns | 4 |
| CAS# to WE# delay time | tCWD | 35 | | 40 | | ns | 13, 25 |
| Write command to CAS# lead time | tCWL | 15 | | 15 | | ns | |
| Data-in hold time | tDH | 10 | | 12 | | ns | 20 |
| Data-in hold time (referenced to RAS#) | tDHR | 45 | | 55 | | ns | |
| Data-in setup time | tDS | 0 | | 0 | | ns | 20 |
| Output disable | tOD | 0 | 15 | 0 | 15 | ns | |
| Output Enable | tOE | | 15 | | 20 | ns | 19, 23 |
| OE# hold time from WE# during READ-MODIFY-WRITE cycle | tOEH | 12 | | 12 | | ns | 18 |
| OE# HIGH hold from CAS# HIGH | tOEHC | 10 | | 10 | | ns | 18 |
| OE# HIGH pulse width | tOEP | 10 | | 10 | | ns | |
| OE# LOW to CAS# HIGH setup time | tOES | 5 | | 5 | | ns | |
| Output buffer turn-off delay | tOFF | 3 | 15 | 3 | 15 | ns | 19, 23 |
| OE# setup prior to RAS# during HIDDEN REFRESH cycle | tORD | 0 | | 0 | | ns | |
| EDO-PAGE-MODE READ or WRITE cycle time | tPC | 25 | | 30 | | ns | |
| EDO-PAGE-MODE READ-WRITE cycle time | tPRWC | 75 | | 85 | | ns | 31 |
| Access time from RAS# | tRAC | | 60 | | 70 | ns | 13 |
| RAS# to column-address delay time | tRAD | 12 | 30 | 12 | 35 | ns | 17 |
| Row-address hold time | tRAH | 10 | | 10 | | ns | |
| Column-address to RAS# lead time | tRAL | 30 | | 35 | | ns | |
| RAS# pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | ns | |
| RAS# pulse width (EDO PAGE MODE) | tRASP | 60 | 125,000 | 70 | 125,000 | ns | |
| Random READ or WRITE cycle time | tRC | 110 | | 130 | | ns | |
| RAS# to CAS# delay time | tRCD | 14 | 45 | 14 | 50 | ns | 16 |
| Read command hold time (referenced to CAS#) | tRCH | 0 | | 0 | | ns | 18 |
| Read command setup time | tRCS | 0 | | 0 | | ns | |

## EDO PAGE MODE
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

| AC CHARACTERISTICS - EDO PAGE MODE OPTION | | -6 | | -7 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Refresh period (1,024 cycles) | tREF | | 16 | | 16 | ms | |
| Refresh period (1,024 cycles) L version | tREF | | 128 | | 128 | ms | |
| RAS# precharge time | tRP | 40 | | 50 | | ns | |
| RAS# to CAS# precharge time | tRPC | 0 | | 0 | | ns | |
| Read command hold time (referenced to RAS#) | tRRH | 0 | | 0 | | ns | 18 |
| RAS# hold time | tRSH | 10 | | 12 | | ns | |
| READ WRITE cycle time | tRWC | 145 | | 170 | | ns | |
| RAS# to WE# delay time | tRWD | 80 | | 90 | | ns | 13 |
| Write command to RAS# lead time | tRWL | 15 | | 15 | | ns | |
| Transition time (rise or fall) | tT | 2 | 50 | 2 | 50 | ns | |
| Write command hold time | tWCH | 10 | | 12 | | ns | |
| Write command hold time (referenced to RAS#) | tWCR | 45 | | 55 | | ns | |
| WE# command setup time | tWCS | 0 | | 0 | | ns | |
| Output disable delay from WE# (CAS# HIGH) | tWHZ | 0 | 13 | 0 | 15 | ns | |
| Write command pulse width | tWP | 10 | | 12 | | ns | |
| WE# pulse width for output disable when CAS# HIGH | tWPZ | 10 | | 12 | | ns | |
| WE# hold time (CBR REFRESH) | tWRH | 10 | | 10 | | ns | |
| WE# setup time (CBR REFRESH) | tWRP | 10 | | 10 | | ns | |

## NOTES

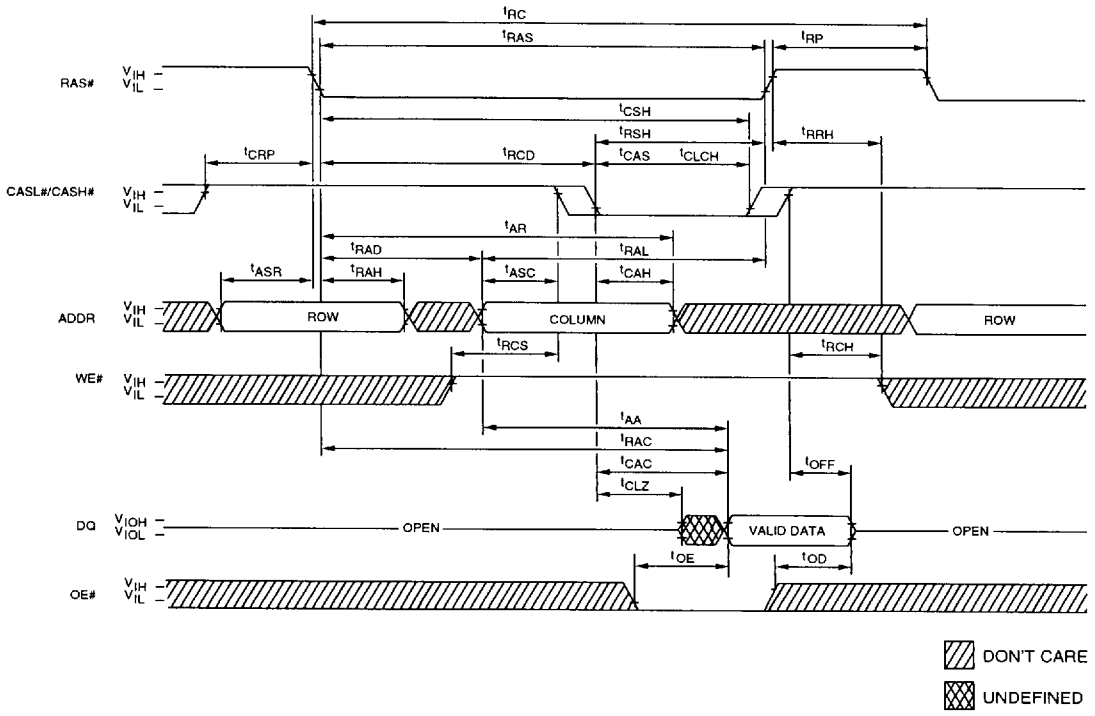
1. All voltages referenced to Vss.
2. This parameter is sampled. $V_{CC}$ = +3.3V ±0.3V; f = 1 MHz.
3. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS# ONLY or CBR with WE# HIGH) before proper device operation is assured. The eight RAS# cycle wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 5ns for FAST PAGE MODE and $^{t}$T = 2.5ns for EDO PAGE MODE.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If CAS# = $V_{IH}$, data output is High-Z.
11. If CAS# = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V.
13. Assumes that $^{t}$RCD < $^{t}$RCD (MAX). If $^{t}$RCD is greater than the maximum recommended value shown in this table, $^{t}$RAC will increase by the amount that $^{t}$RCD exceeds the value shown.
14. Assumes that $^{t}$RCD ≥ $^{t}$RCD (MAX).
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for $^{t}$CP.
16. Operation within the $^{t}$RCD (MAX) limit ensures that $^{t}$RAC (MAX) can be met. $^{t}$RCD (MAX) is specified as a reference point only; if $^{t}$RCD is greater than the specified $^{t}$RCD (MAX) limit, then access time is controlled exclusively by $^{t}$CAC, provided $^{t}$RAD is not exceeded.
17. Operation within the $^{t}$RAD (MAX) limit ensures that $^{t}$RAC (MIN) and $^{t}$CAC (MIN) can be met. $^{t}$RAD (MAX) is specified as a reference point only; if $^{t}$RAD is greater than the specified $^{t}$RAD (MAX) limit, then access time is controlled exclusively by $^{t}$AA, provided $^{t}$RCD is not exceeded.
18. Either $^{t}$RCH or $^{t}$RRH must be satisfied for a READ cycle.
19. $^{t}$OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$. It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
20. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
21. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
23. The 3ns minimum is a parameter guaranteed by design.
24. Column-address changed once each cycle.
25. 8MB module values will be half of those shown.
26. For FAST PAGE MODE option, $^{t}$OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, $^{t}$OFF on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
27. Applies to both EDO and FAST PAGE MODE operating modes.
28. All other inputs at 0.2V or $V_{CC}$ -0.2V.
29. L version only.
30. $^{t}$WCS, $^{t}$RWD, $^{t}$AWD and $^{t}$CWD are not restrictive operating parameters. $^{t}$WCS applies to EARLY WRITE cycles. $^{t}$RWD, $^{t}$AWD and $^{t}$CWD apply to READ-MODIFY-WRITE cycles. If $^{t}$WCS ≥ $^{t}$WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}$WCS < $^{t}$WCS (MIN) and $^{t}$RWD ≥ $^{t}$RWD (MIN), $^{t}$AWD ≥ $^{t}$AWD (MIN) and $^{t}$CWD ≥ $^{t}$CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. $^{t}$WCS, $^{t}$RWD, $^{t}$CWD and $^{t}$AWD are not applicable in a LATE WRITE cycle.

## NOTES (continued)

31. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^{t}$OD and $^{t}$OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after $^{t}$OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.

32. The SPD EEPROM WRITE cycle time ($^{t}$WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

## READ CYCLE
(FAST PAGE MODE Module)

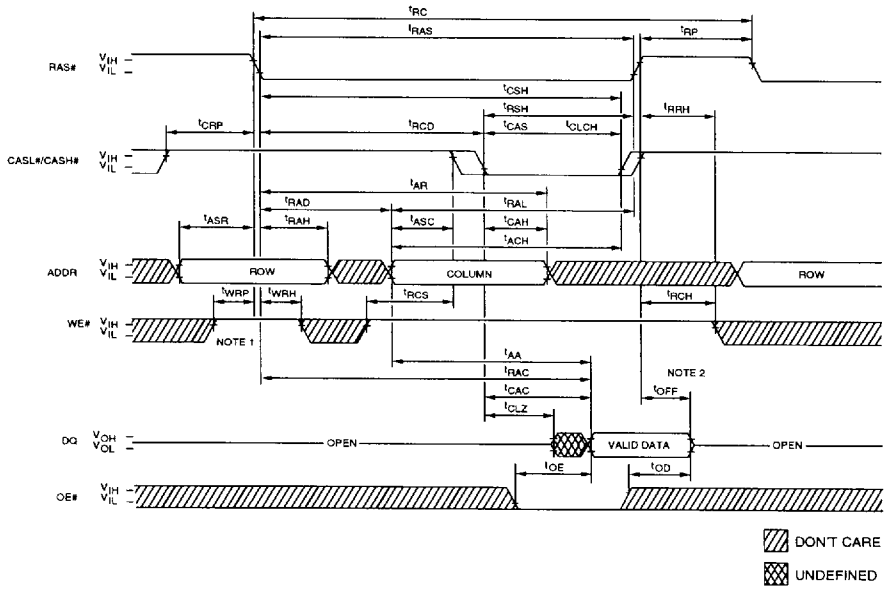



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tAR | 50 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 15 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOFF | 3 | 15 | 3 | 20 | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | 30 | 15 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 110 | | 130 | | ns |
| tRCD | 20 | 45 | 20 | 50 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 15 | | 20 | | ns |

## READ CYCLE
(EDO PAGE MODE Module)



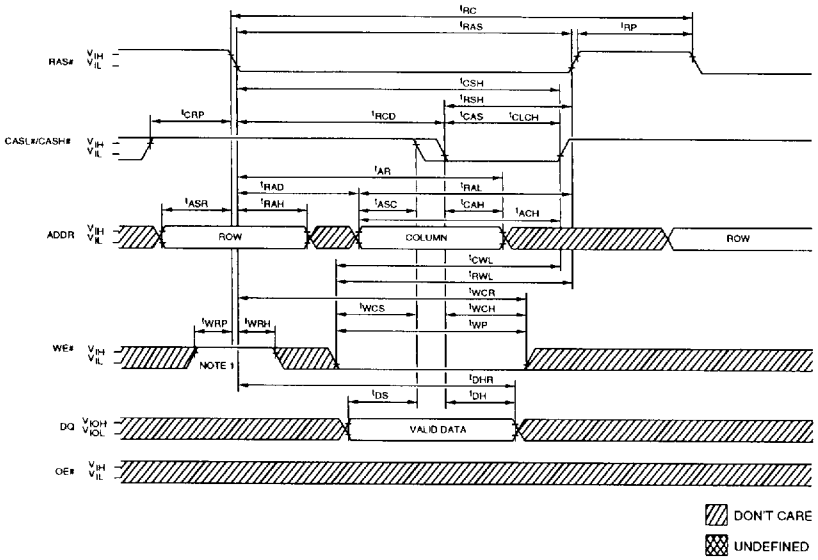

**NOTE:**
1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |
| tOE | | 15 | | 15 | ns |
| tOFF | 3 | 15 | 3 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAC | | 60 | | 70 | ns |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 105 | | 125 | | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## EARLY WRITE CYCLE [27]

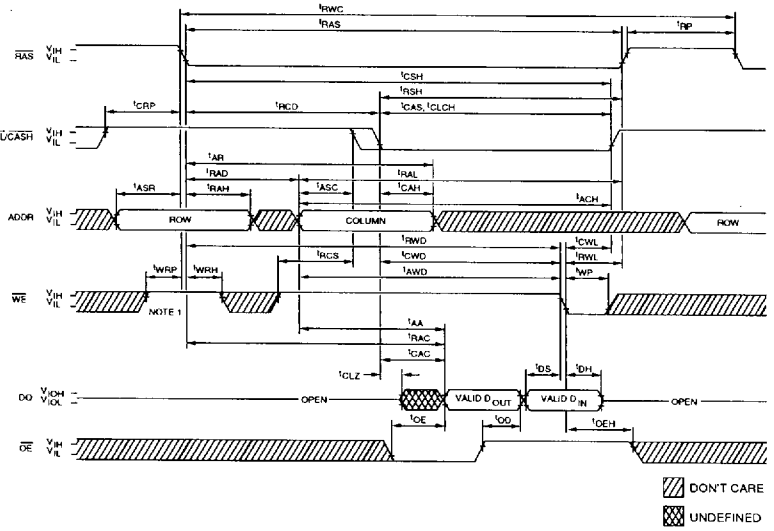



## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tACH (EDO) | 15 | | 15 | | ns |
| tAR (FPM) | 50 | | 55 | | ns |
| tAR (EDO) | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH (FPM) | 10 | | 15 | | ns |
| tCAH (EDO) | 10 | | 12 | | ns |
| tCAS (FPM) | 15 | 10,000 | 20 | 10,000 | ns |
| tCAS (EDO) | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH (FPM) | 60 | | 70 | | ns |
| tCSH (EDO) | 50 | | 55 | | ns |
| tCWL (FPM) | 15 | | 20 | | ns |
| tCWL (EDO) | 15 | | 15 | | ns |
| tDH (FPM) | 10 | | 15 | | ns |
| tDH (EDO) | 10 | | 12 | | ns |
| tDHR | 45 | | 55 | | ns |
| tDS | 0 | | 0 | | ns |
| tRAD (FPM) | 15 | 30 | 15 | 35 | ns |
| tRAD (EDO) | 12 | 30 | 12 | 35 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC (FPM) | 110 | | 130 | | ns |
| tRC (EDO) | 105 | | 125 | | ns |
| tRCD (FPM) | 20 | 45 | 20 | 50 | ns |
| tRCD (EDO) | 14 | 45 | 14 | 50 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH (FPM) | 15 | | 20 | | ns |
| tRSH (EDO) | 13 | | 15 | | ns |
| tRWL (FPM) | 15 | | 20 | | ns |
| tRWL (EDO) | 15 | | 15 | | ns |
| tWCH (FPM) | 10 | | 15 | | ns |
| tWCH (EDO) | 10 | | 12 | | ns |
| tWCR | 45 | | 55 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP (FPM) | 10 | | 15 | | ns |
| tWP (EDO) | 10 | | 12 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



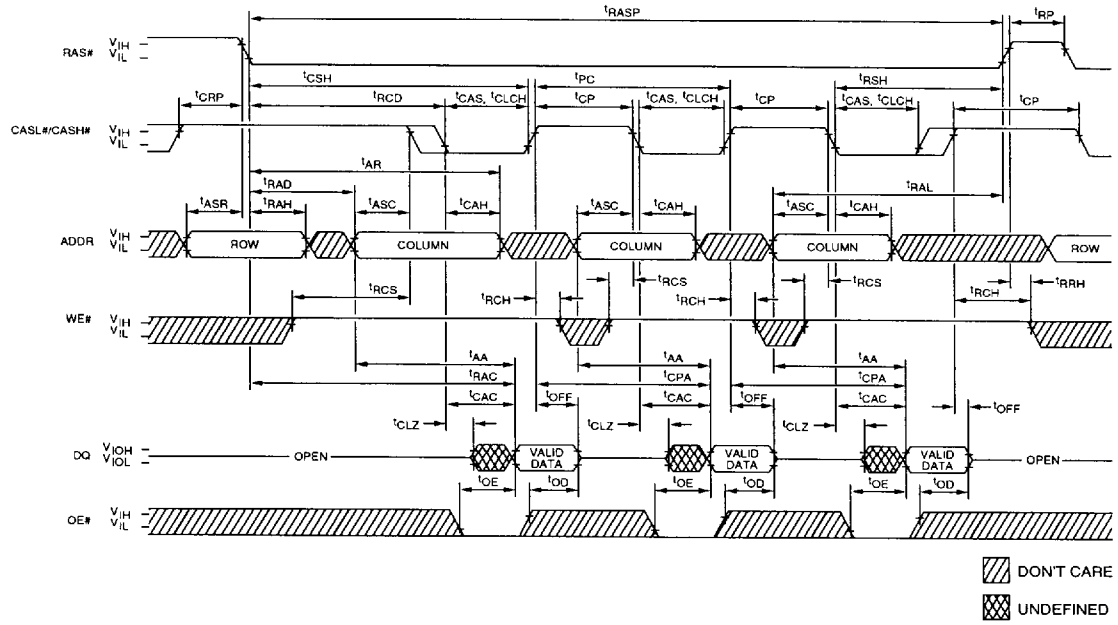

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 55 | | 60 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tCWD | 35 | | 40 | | ns |
| tCWL | 15 | | 15 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 12 | | 12 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWC | 145 | | 170 | | ns |
| tRWD | 80 | | 90 | | ns |
| tRWL | 15 | | 15 | | ns |
| tWP | 10 | | 12 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## FAST-PAGE-MODE READ CYCLE

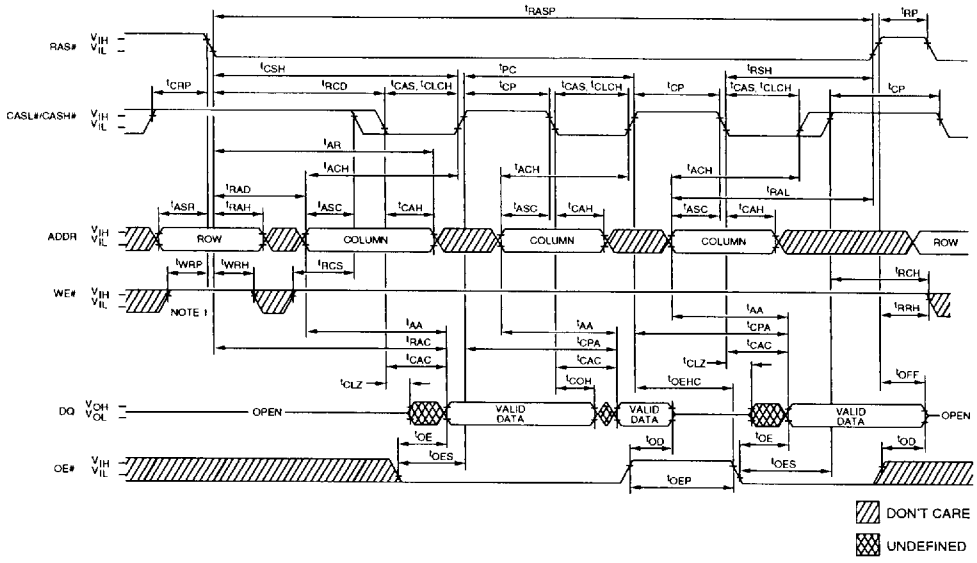



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tAR | 50 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 15 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOFF | 3 | 15 | 3 | 20 | ns |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | 30 | 15 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 20 | 45 | 20 | 50 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 15 | | 20 | | ns |

## EDO-PAGE-MODE READ CYCLE



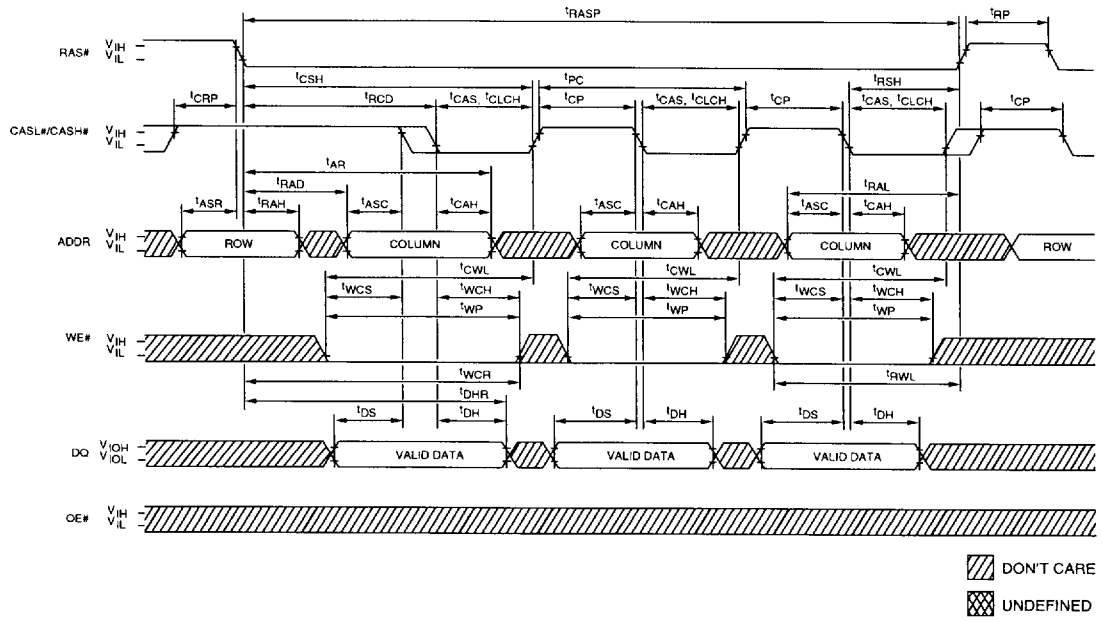

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |
| tOE | | 15 | | 20 | ns |
| tOEHC | 10 | | 10 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOEP | 10 | | 10 | | ns |
| tOES | 5 | | 5 | | ns |
| tOFF | 3 | 15 | 3 | 15 | ns |
| tPC | 25 | | 30 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## FAST-PAGE-MODE EARLY-WRITE CYCLE

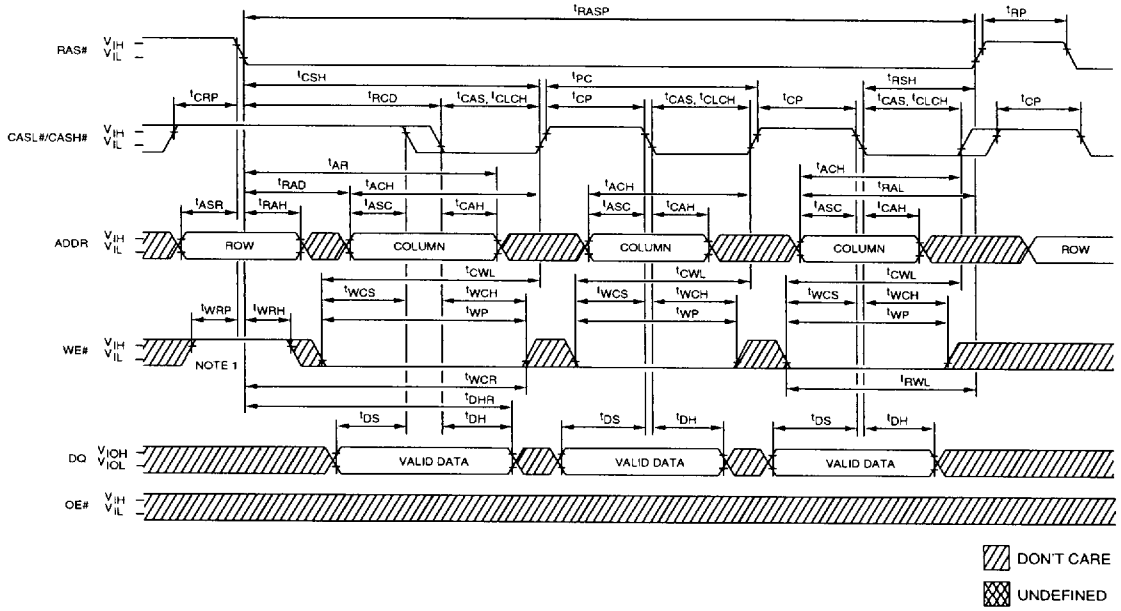



## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAR | 50 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 10 | | 15 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 15 | | ns |
| tDHR | 45 | | 55 | | ns |
| tDS | 0 | | 0 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tPC | 35 | | 40 | | ns |
| tRAD | 15 | 30 | 15 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 20 | 45 | 20 | 50 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWCH | 10 | | 15 | | ns |
| tWCR | 45 | | 55 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 15 | | ns |

## EDO-PAGE-MODE EARLY-WRITE CYCLE



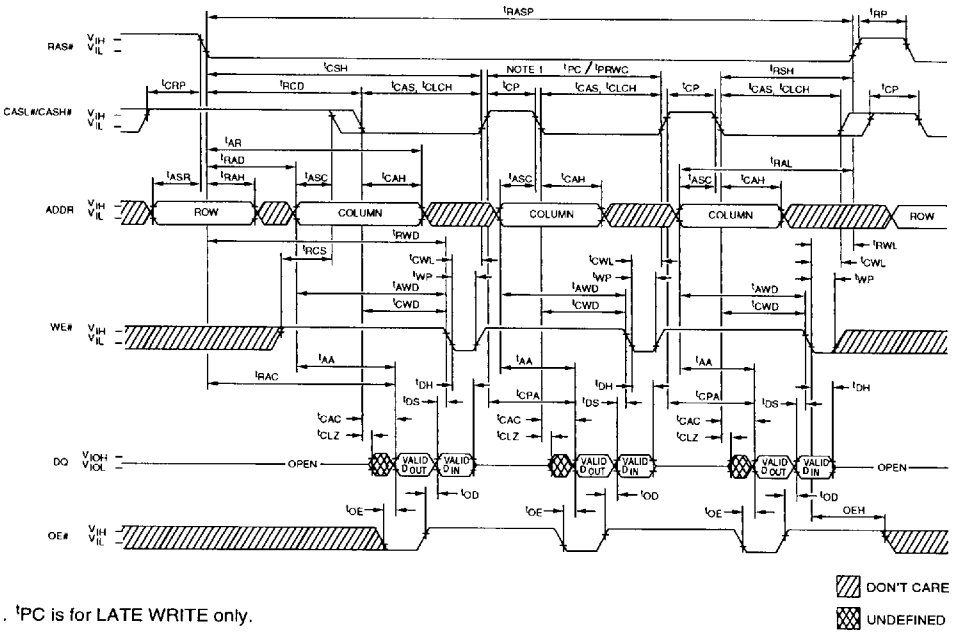

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tACH | 15 | | 15 | | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tCWL | 15 | | 15 | | ns |
| tDH | 10 | | 12 | | ns |
| tDHR | 45 | | 55 | | ns |
| tDS | 0 | | 0 | | ns |
| tPC | 25 | | 30 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 15 | | 15 | | ns |
| tWCH | 10 | | 12 | | ns |
| tWCR | 45 | | 55 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 12 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



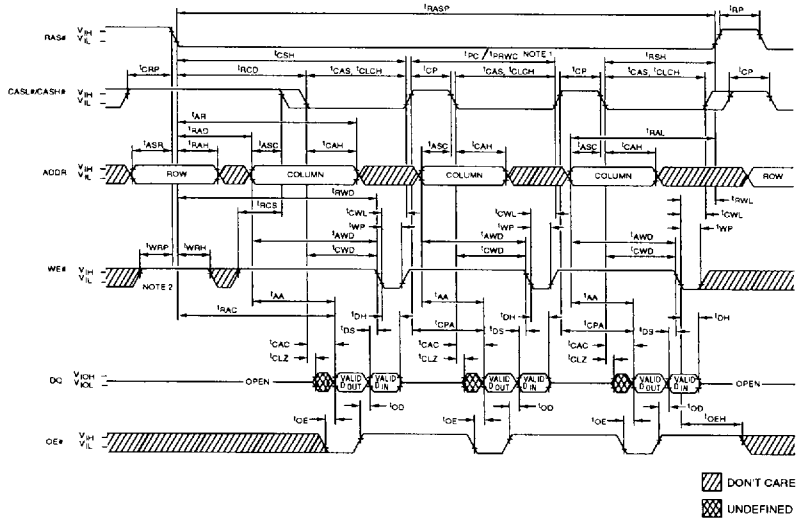

**NOTE:** 1. tPC is for LATE WRITE only.

## TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tAR | 50 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 55 | | 60 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 15 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWD | 40 | | 45 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 15 | | ns |
| tDS | 0 | | 0 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |
| tOEH | 15 | | 20 | | ns |
| tPC | 35 | | 40 | | ns |
| tPRWC | 85 | | 95 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | 30 | 15 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 20 | 45 | 20 | 50 | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWD | 85 | | 95 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWP | 10 | | 15 | | ns |

## EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



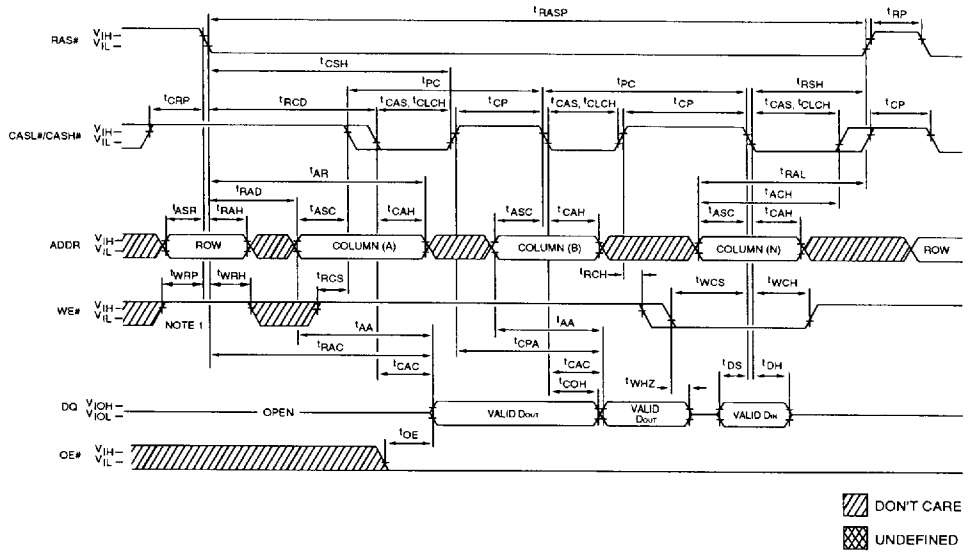

**NOTE:**
1. tPC is for LATE WRITE cycles only.
2. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 55 | | 60 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tCWD | 35 | | 40 | | ns |
| tCWL | 15 | | 15 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |
| tOD | 0 | 15 | 0 | 15 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOE | | 15 | | 20 | ns |
| tOEH | 12 | | 12 | | ns |
| tPC | 25 | | 30 | | ns |
| tPRWC | 75 | | 85 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWD | 80 | | 90 | | ns |
| tRWL | 15 | | 15 | | ns |
| tWP | 10 | | 12 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



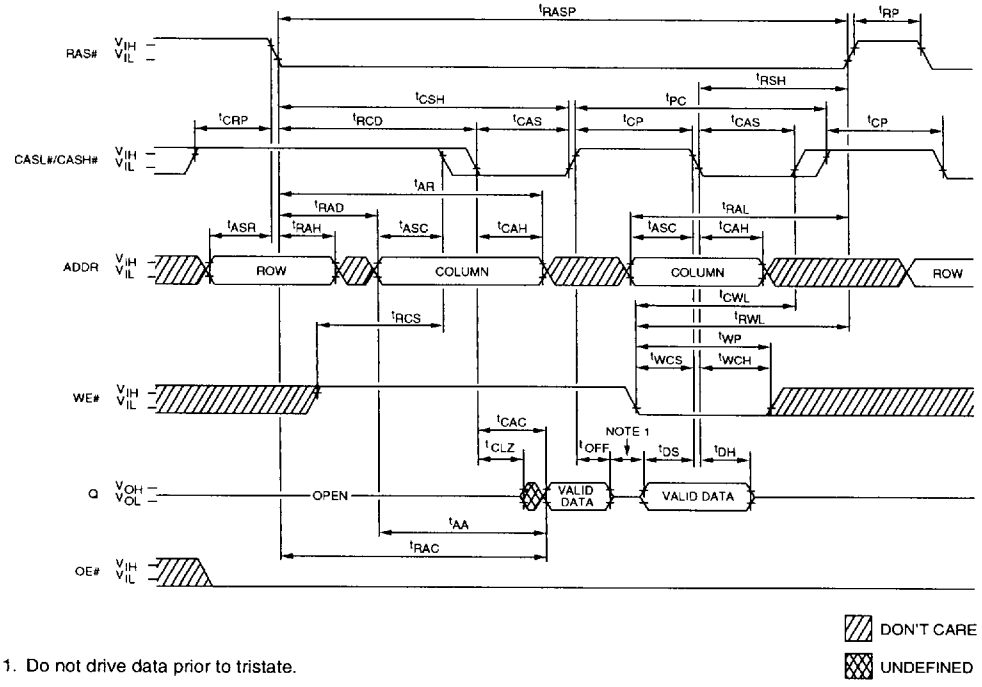

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tACH | 15 | | 15 | | ns |
| tAR | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 12 | 10,000 | 13 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 50 | | 55 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |
| tOE | | 15 | | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tPC | 25 | | 30 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 14 | 45 | 14 | 50 | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWCH | 10 | | 12 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWHZ | 0 | 13 | 0 | 15 | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



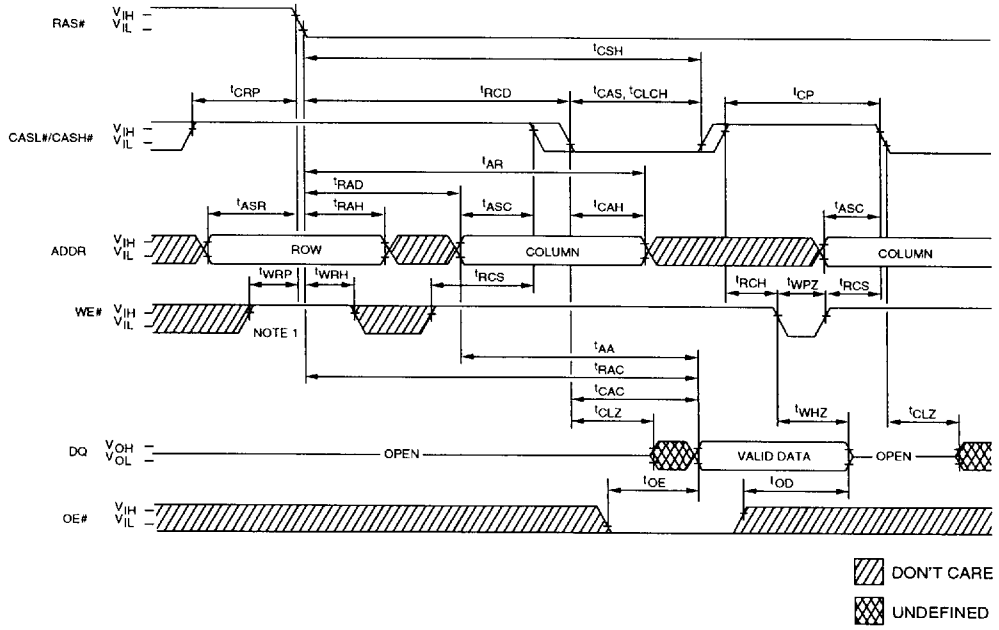

**NOTE:** 1. Do not drive data prior to tristate.

## FAST PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tAA | | 30 | | 35 | ns |
| tAR | 50 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 15 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 15 | | ns |
| tDS | 0 | | 0 | | ns |
| tOFF | 3 | 15 | 3 | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | 30 | 15 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRASP | 60 | 100,000 | 70 | 100,000 | ns |
| tRCD | 20 | 45 | 20 | 50 | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWCH | 10 | | 15 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 15 | | ns |

## EDO READ CYCLE
(with WE#-controlled disable)



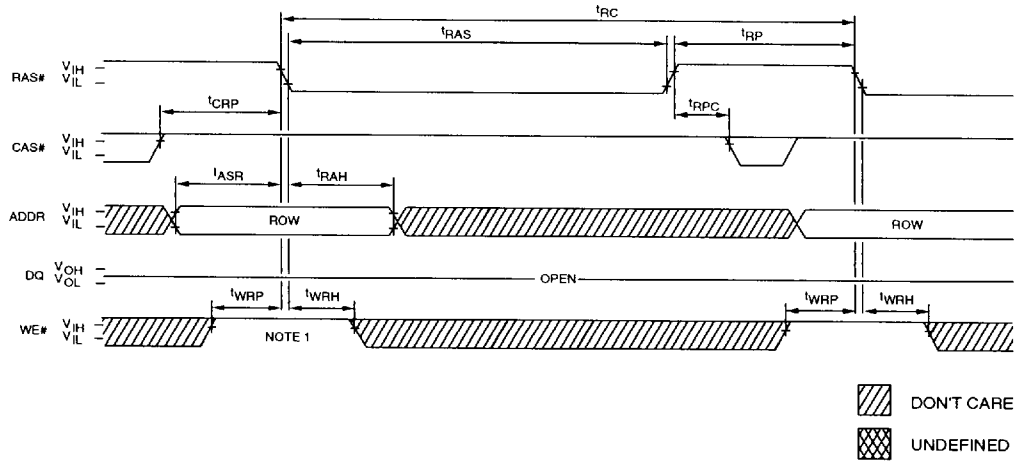

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for $^{t}$WRP and $^{t}$WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$AA | | 30 | | 35 | ns |
| $^{t}$AR | 45 | | 50 | | ns |
| $^{t}$ASC | 0 | | 0 | | ns |
| $^{t}$ASR | 0 | | 0 | | ns |
| $^{t}$CAC | | 15 | | 20 | ns |
| $^{t}$CAH | 10 | | 12 | | ns |
| $^{t}$CAS | 12 | 10,000 | 13 | 10,000 | ns |
| $^{t}$CLCH | 10 | | 10 | | ns |
| $^{t}$CLZ | 0 | | 0 | | ns |
| $^{t}$CP | 10 | | 10 | | ns |
| $^{t}$CRP | 5 | | 5 | | ns |
| $^{t}$CSH | 50 | | 55 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$OD | 0 | 15 | 0 | 15 | ns |
| $^{t}$OE | | 15 | | 20 | ns |
| $^{t}$RAC | | 60 | | 70 | ns |
| $^{t}$RAD | 12 | 30 | 12 | 35 | ns |
| $^{t}$RAH | 10 | | 10 | | ns |
| $^{t}$RCD | 14 | 45 | 14 | 50 | ns |
| $^{t}$RCH | 0 | | 0 | | ns |
| $^{t}$RCS | 0 | | 0 | | ns |
| $^{t}$WHZ | 0 | 13 | 0 | 15 | ns |
| $^{t}$WPZ | 10 | | 12 | | ns |
| $^{t}$WRH | 10 | | 10 | | ns |
| $^{t}$WRP | 10 | | 10 | | ns |

## RAS#-ONLY REFRESH CYCLE [27]



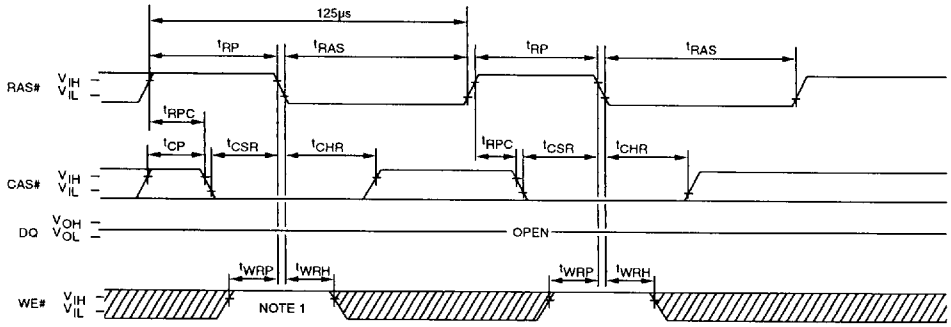

**NOTE:** 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for $^{t}$WRP and $^{t}$WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

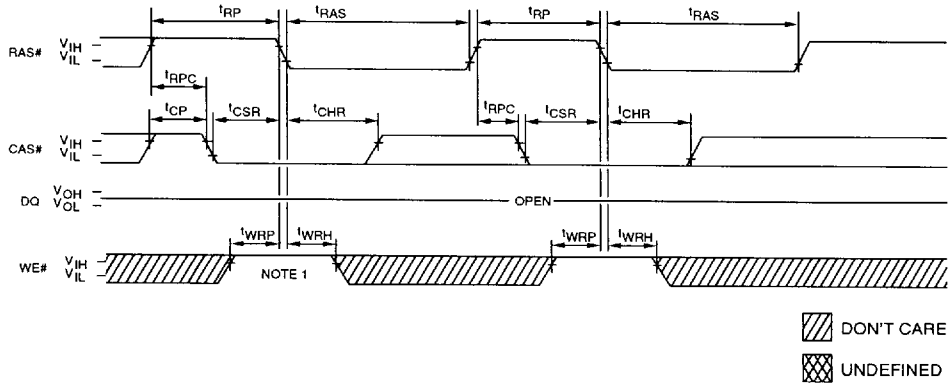
| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$ASR | 0 | | 0 | | ns |
| $^{t}$CRP | 5 | | 5 | | ns |
| $^{t}$RAH | 10 | | 10 | | ns |
| $^{t}$RAS | 60 | 10,000 | 70 | 10,000 | ns |
| $^{t}$RC | 110 | | 130 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$RP | 40 | | 50 | | ns |
| $^{t}$RPC (FPM) | 0 | | 0 | | ns |
| $^{t}$RPC (EDO) | 5 | | 5 | | ns |
| $^{t}$WRH | 10 | | 10 | | ns |
| $^{t}$WRP | 10 | | 10 | | ns |

## EXTENDED CBR REFRESH CYCLE [27, 29]
(Addresses = DON'T CARE)




## CBR REFRESH CYCLE [27]
(Addresses = DON'T CARE)



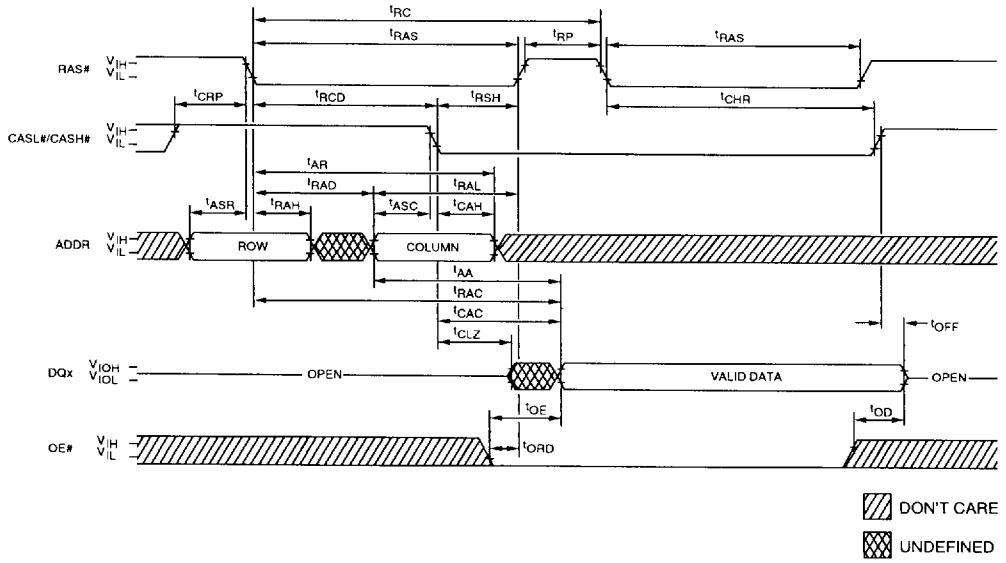

**NOTE:** 1. $^{t}$WRP and $^{t}$WRH are for system design reference only. The WE# signal is actually a "don't care" at RAS# time during a CBR REFRESH. However, WE# should be held HIGH at RAS# time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE# HIGH at RAS# time during a CBR REFRESH.

## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$CHR | 15 | | 15 | | ns |
| $^{t}$CP | 10 | | 10 | | ns |
| $^{t}$CSR | 5 | | 5 | | ns |
| $^{t}$RAS | 60 | 10,000 | 70 | 10,000 | ns |
| $^{t}$RP | 40 | | 50 | | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| $^{t}$RPC (FPM) | 0 | | 0 | | ns |
| $^{t}$RPC (EDO) | 5 | | 5 | | ns |
| $^{t}$WRH | 10 | | 10 | | ns |
| $^{t}$WRP | 10 | | 10 | | ns |

## HIDDEN REFRESH CYCLE [22, 27]
(WE# = HIGH)

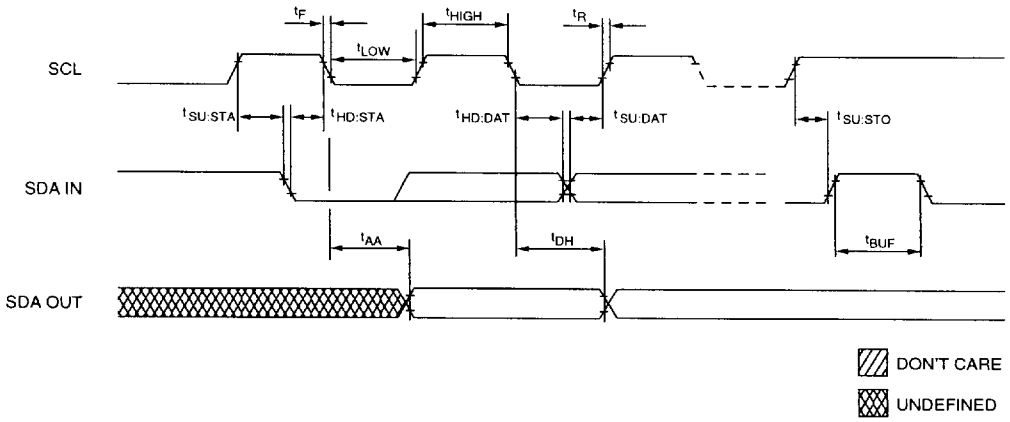



## FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 30 | | 35 | ns |
| tAR (FPM) | 50 | | 55 | | ns |
| tAR (EDO) | 45 | | 50 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH (FPM) | 10 | | 15 | | ns |
| tCAH (EDO) | 10 | | 12 | | ns |
| tCHR (FPM) | 15 | | 15 | | ns |
| tCHR (EDO) | 10 | | 12 | | ns |
| tCLZ (FPM) | 3 | | 3 | | ns |
| tCLZ (EDO) | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |
| tOFF (FPM) | 3 | 15 | 3 | 20 | ns |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYM | MIN | MAX | MIN | MAX | UNITS |
| tOFF (EDO) | 3 | 15 | 3 | 15 | ns |
| tORD | 0 | | 0 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD (FPM) | 15 | 30 | 15 | 35 | ns |
| tRAD (EDO) | 12 | 30 | 12 | 35 | ns |
| tRAH | 10 | | 10 | | ns |
| tRAL | 30 | | 35 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC (FPM) | 110 | | 130 | | ns |
| tRC (EDO) | 105 | | 125 | | ns |
| tRCD (FPM) | 20 | 45 | 20 | 50 | ns |
| tRCD (EDO) | 14 | 45 | 14 | 50 | ns |
| tRP | 40 | | 50 | | ns |
| tRSH (FPM) | 15 | | 20 | | ns |
| tRSH (EDO) | 10 | | 12 | | ns |

## SPD EEPROM

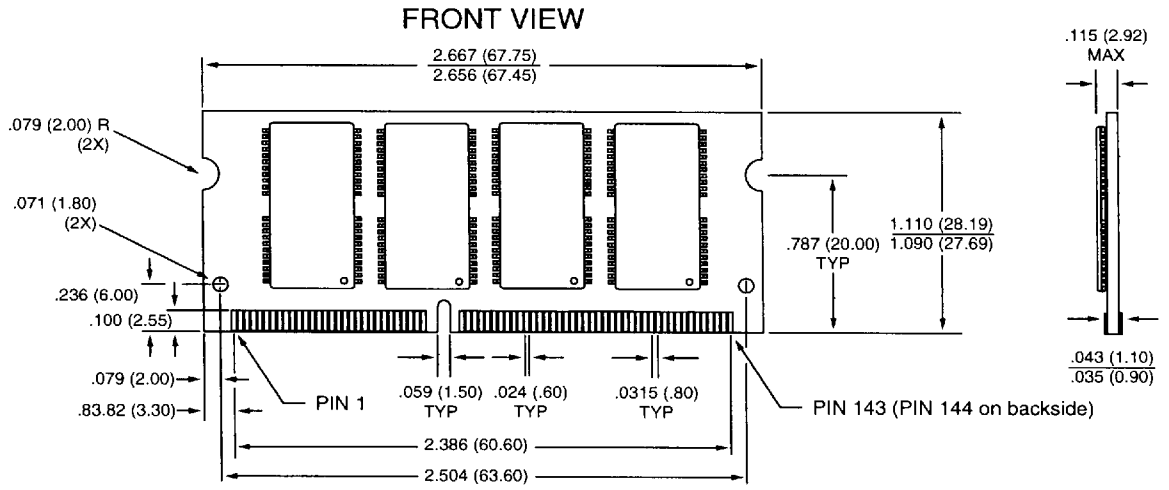



## SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

| SYM | MIN | MAX | UNITS |
|---|---|---|---|
| tAA | 0.3 | 3.5 | µs |
| tBUF | 4.7 | | µs |
| tDH | 300 | | ns |
| tF | | 300 | ns |
| tHD:DAT | 0 | | µs |
| tHD:STA | 4 | | µs |
| tHIGH | 4 | | µs |
| tI | | 100 | ns |

| SYM | MIN | MAX | UNITS |
|---|---|---|---|
| tLOW | 4.7 | | µs |
| tR | | 1 | µs |
| tSCL | | 100 | KHz |
| tSU:DAT | 250 | | ns |
| tSU:STA | 4.7 | | µs |
| tSU:STO | 4.7 | | µs |
| tWR | | 10 | ms |

## 144-Pin SO DIMM
(8 MB)




## 144-Pin SO DIMM
(16 MB)