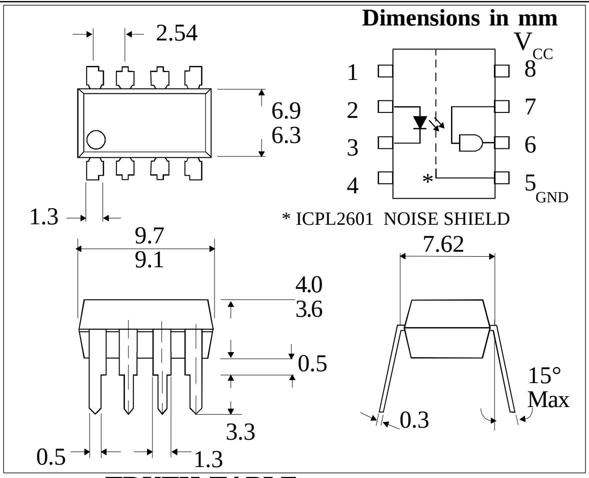
6N137
ICPL2601

HIGH CMR, VERY HIGH SPEED OPTICALLY COUPLED ISOLATOR LOGIC GATE OUTPUT



APPROVALS

- UL recognised, File No. E91231

DESCRIPTION

The 6N137 / ICPL2601 optocouplers consist of a GaAsP light emitting diode and a high gain integrated photo detector to provide 2500Volts $_{RMS}$ electrical isolation between input and output. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The ICPL2601 has an internal shield which provides a guaranteed common mode transient immunity specification of 1000V/µs minimum.This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The coupled parameters are guaranteed over the temperature range of 0°C to 70°C, such that a maximum input signal of 5mA will provide a minimum output sink current of 13mA(equivalent to fan-out of eight gates)

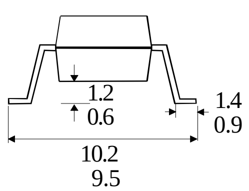
FEATURES

- High speed - 10MBit/s
- High Common Mode Transient Immunity 10kV/µs typical
- Logic gate output
- ICPL2601 has improved noise shield for superior common mode rejection
- Options :-
  10mm lead spread - add G after part no.
  Surface mount - add SM after part no.
  Tape&reel - add SMT&R after part no.

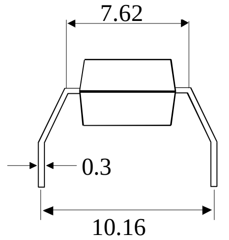
APPLICATIONS

- Line receiver, data transmission
- Computer-peripheral interface
- Data multiplexing
- Pulse transformer replacement

OPTION SM
SURFACE MOUNT



OPTION G



TRUTH TABLE

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

A 0.1µF bypass capacitor must be connected between pins 8 and 5 (See note 1)

ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise specified)

Storage Temperature	-55°C to + 125°C
Operating Temperature	0°C to + 70°C
Lead Soldering Temperature (1/16 inch (1.6mm) from case for 10 secs)	260°C

INPUT DIODE

Average Forward Current	20mA
Reverse Voltage	5V

DETECTOR

Enable Input Voltage (V_E) (not to exceed V_{CC} by more than 500mV)	5.5V
Reverse Supply Voltage(- V_{CC})	-500mV
Supply Voltage(V_{CC}) (1 minute maximum)	7V
Output Current (I_O)	25mA
Output Voltage (V_O)	7V
Collector Output Power Dissipation	40mW

ISOCOM COMPONENTS LTD
Unit 25B, Park View Road West,
Park View Industrial Estate, Brenda Road
Hartlepool, TS25 1YD England Tel: (01429)863609
Fax : (01429) 863581 e-mail sales@isocom.co.uk
http://www.isocom.com

ISOCOM INC
1024 S. Greenville Ave, Suite 240,
Allen, TX 75002 USA
Tel: (214) 495-0755 Fax: (214) 495-0901
e-mail info@isocom.com
http://www.isocom.com

ELECTRICAL CHARACTERISTICS (T_A= 0°C to 70°C Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
High Level Output Current	I_{OH}			0.02	250	µA	V_{CC} = 5.5V, V_O = 5.5V I_F = 250µA, V_E = 2V
Low Level Output Voltage	V_{OL}			0.4	0.6	V	V_{CC} = 5.5V, I_F = 5mA V_E = 2V I_{OL} (sinking) = 13mA
High Level Supply Current	I_{CCH}			10	15	mA	V_{CC} = 5.5V, I_F = 0mA V_E = 0.5V
Low Level Supply Current	I_{CCL}			15	18	mA	V_{CC} = 5.5V, I_F = 10mA V_E = 0.5V
High Level Enable Current	I_{EH}			-1.0		mA	V_{CC} = 5.5V, V_E = 2V
Low Level Enable Current	I_{EL}			-1.5	-2.0	mA	V_{CC} = 5.5V, V_E = 0.5V
High Level Enable Voltage (note 10)	V_{EH}		2			V	V_{CC} = 5.5V, I_F = 10mA
Low Level Enable Voltage	V_{EL}				0.8	V	V_{CC} = 5.5V, I_F = 10mA
Input Forward Voltage	V_F			1.55	1.75	V	I_F = 10mA, T_A = 25°C
Input Reverse Breakdown Voltage	V_{BR}		5			V	I_R = 10µA, T_A = 25°C
Input Capacitance	C_{IN}			60		pF	V_F = 0, f = 1MHz
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.4		mV/°C	I_F = 10mA
Input-output Isolation Voltage (note 3)	V_{ISO}		2500	5000		V_{RMS}	R.H.equal to or less than 50%, t = 1min, T_A= 25°C
Input-output Insulation Leakage Current (note 3)	I_{I-O}				1	µA	R.H. = 45% t = 5s, T_A= 25°C V_{I-O} = 3000V dc
Resistance (Input to Output) (note 3)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500V dc
Capacitance (Input to Output) (note 3)	C_{I-O}			0.6		pF	f = 1MHz

* All typicals at T_A= 25°C

RECOMMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Enable Voltage, Low Level	V_{EL}	0	0.8	V
Enable Voltage, High Level	V_{EH}	2.0	V_{CC}	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

*6.3mA is a guard banded value which allows for at least 20% CTR degradation.
Initial input current threshold value is 5.0mA or less

SWITCHING SPECIFICATIONS AT T_A = 25°C (V_{CC} = 5V, I_F = 7.5mA Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time to Logic Low at Output (fig 1)(note4)	t_{PHL}			55	75	ns	R_L = 350Ω, C_L = 15pF
Propagation Delay Time to Logic High at Output (fig 1)(note5)	t_{PLH}			45	75	ns	R_L = 350Ω, C_L = 15pF
Propagation Delay Time of Enable from V_{EH} to V_{EL} (note6)	t_{EHL}			14		ns	R_L = 350Ω, C_L = 15pF V_{EL} = 0V, V_{EH} = 3V
Propagation Delay Time of Enable from V_{EL} to V_{EH} (note7)	t_{ELH}			25		ns	R_L = 350Ω, C_L = 15pF V_{EL} = 0V, V_{EH} = 3V
Common Mode Transient Immunity at Logic High Level Output (fig 2)(note8)	CM_H	6N137 ICPL2601	 1000	10000 10000		V/µs V/µs	I_F = 0mA, V_{CM} = 50V_{PP} R_L= 350Ω,V_{OH}= 2Vmin.
Common Mode Transient Immunity at Logic Low Level Output (fig 2)(note9)	CM_L	6N137 ICPL2601	 -1000	-10000 -10000		V/µs V/µs	V_{CM}= 50V_{PP} R_L=350Ω,V_{OL}=0.8Vmax.

NOTES:-

1 Bypassing of the power supply line is required, with a 0.01µF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be seperate from the bus for any active loads. Otherwise a larger value of bypass capacitor (up to 0.1µF) may be needed to supress regenerative feedback via the power supply.

2 Peaking circuits may produce transient input currents up to 50mA, 50ns maximum pulse width, provided average current does not exceed 20mA.

3 Device considered a two terminal device; pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

4 The t_{PHL} propagation delay is measured from the 3.75 mA level Low to High transition of the input current pulse to the 1.5V level on the High to Low transition of the output voltage pulse.

5 The t_{PLH} propagation delay is measured from the 3.75mA level High to Low transition of the input current pulse to the 1.5V level on the Low to High transition of the output voltage pulse.

6 The t_{EHL} enable input propagation delay is measured from the 1.5V level on the Low to High transition of the enable input voltage pulse to the 1.5V level on the High to Low of the output voltage pulse.

7 The t_{ELH} enable input propagation delay is measured from the 1.5V level on the High to Low transition of the enable input voltage pulse to the 1.5V level on the Low to High of the output voltage pulse.

8 CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (ie Vout > 2.0V).

9 CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (ie Vout < 0.8V)

10 No external pull up is required for a high logic state on the enable input.

FIG.1 SWITCHING TEST CIRCUIT

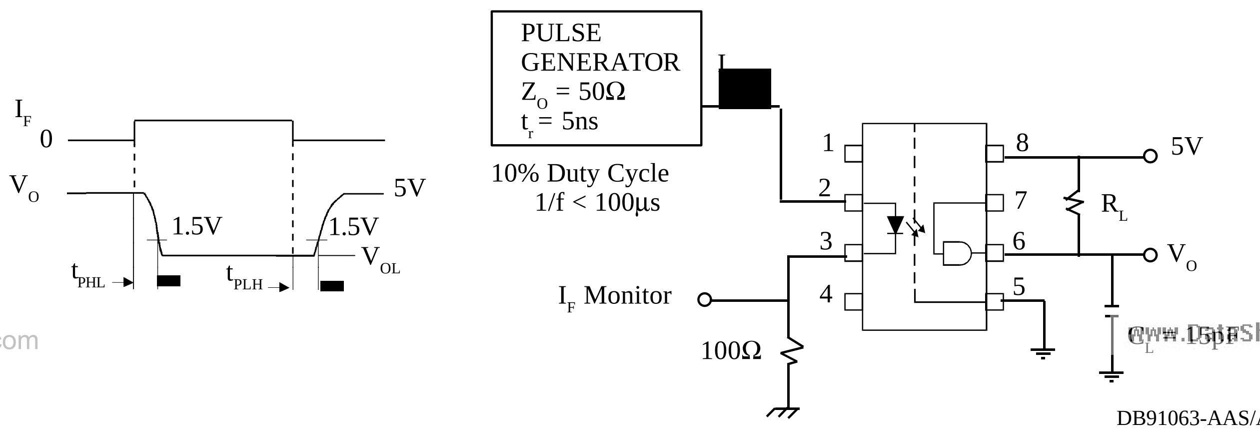
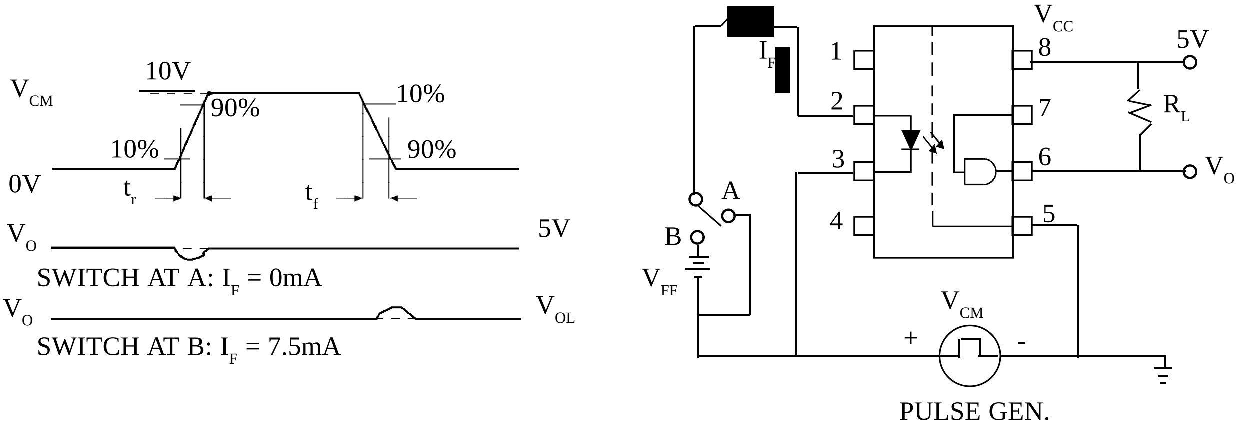
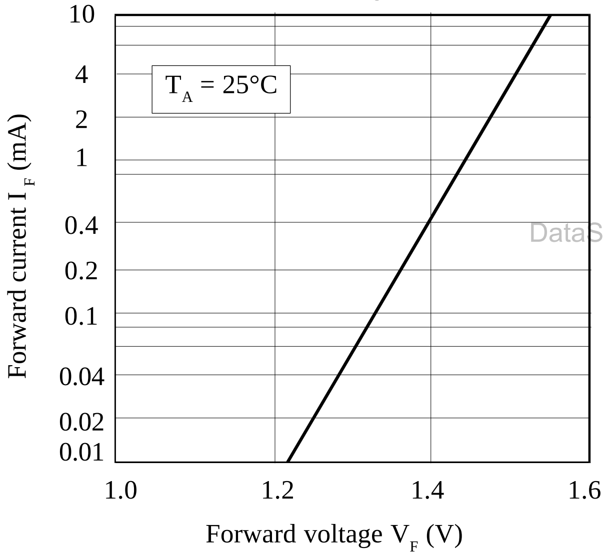


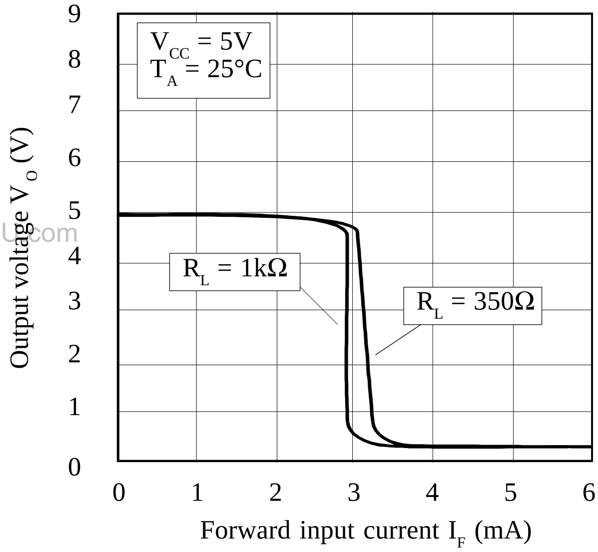
FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS



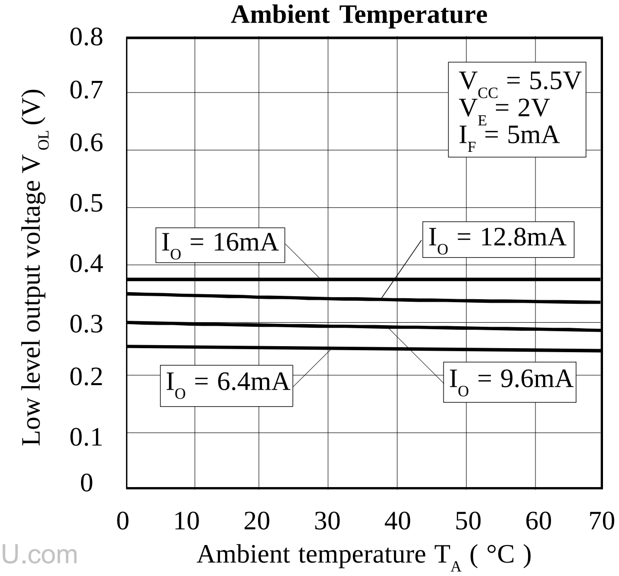
Forward Current vs. Forward Voltage



Output Voltage vs. Forward Input Current



Low Level Output Voltage vs. Ambient Temperature



High Level Output Current vs. Ambient Temperature