HN62V454 Series

262144-word × 16-bit/524288-word × 8-bit CMOS Mask Programmable ROM

HITACHI

ADE-203-615B (Z)
Rev. 2.0
Jun. 26, 1997

Description

The Hitachi HN62V454 series is a 4-Mbit CMOS mask programmable ROM organized either as 262144-word × 16-bit or as 524288-word × 8-bit. It has realized high speed normal access 200 ns on 3.0 V supply. It is the most suitable to the program and data memory for low voltage portable system. It has the package variations of standard 40-pin plastic DIP, standard 40-pin plastic SOP and standard 44-pin plastic TSOPII.

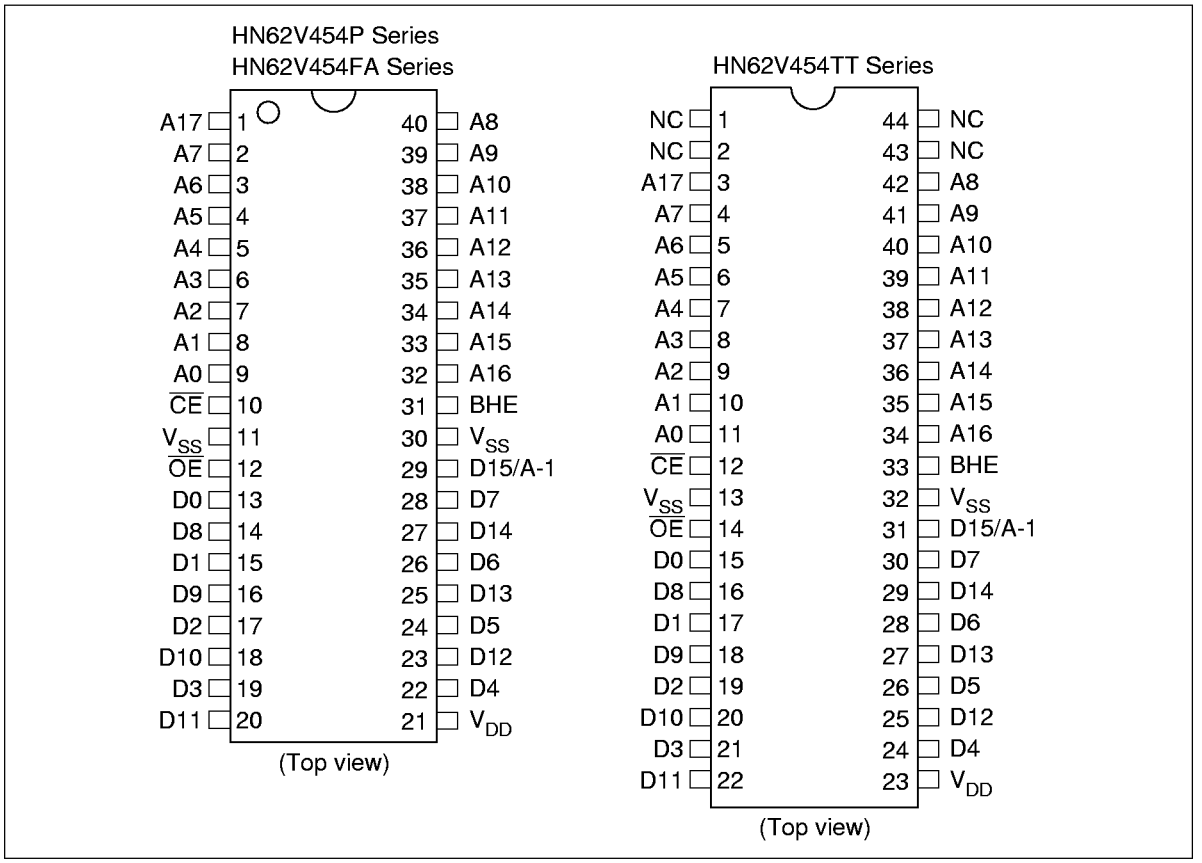
Features

- Single 3.0 V supply : 2.7 V to 3.6 V
- Access time: 200 ns (max)
- Power dissipation
  - — Active: 72 mW (max)
  - — Standby: 72 µW (max)
- Byte-wide or word-wide data organization with byte/word selection (BHE)
- Three-state data output for wired or-tying
- Directly LVTTL compatible all inputs and outputs

Ordering Information

Type No.	Access time	Package
HN62V454P-20	200 ns	600-mil 40-pin plastic DIP (DP-40)
HN62V454FA-20	200 ns	525-mil 40-pin plastic SOP (FP-40D)
HN62V454TT-20	200 ns	400-mil 44-pin plastic TSOPII (TTP-44D)

Pin Arrangement

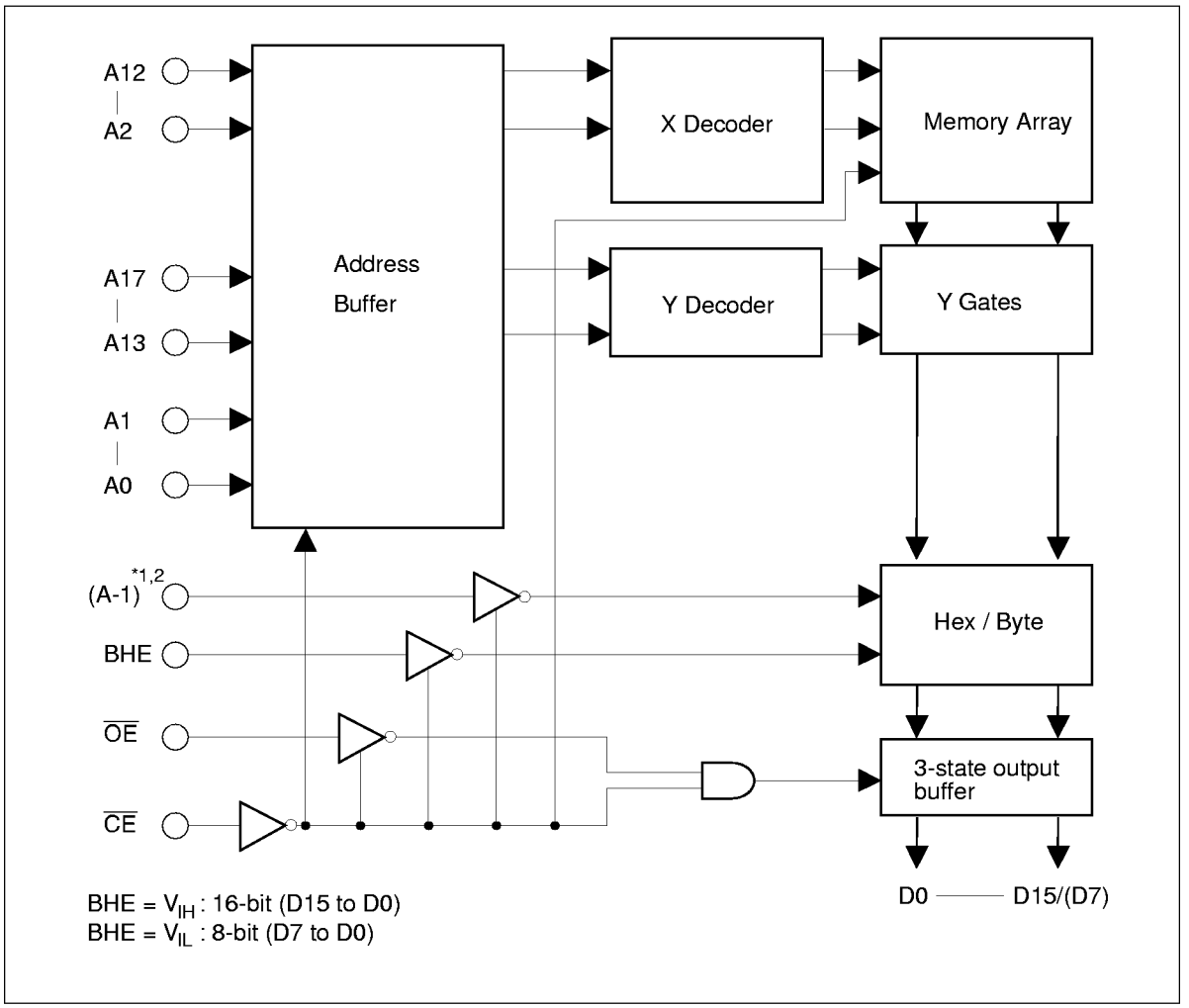


Pin Description

Pin name	Function
A-1, A0 to A17	Address input
D0 to D15	Data output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram

Notes: 1. A-1 is least significant address.
2. When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.



Operation Table

					Data output		Address input	
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**BHE**	**D15/A-1**	**D0-D7**	**D8-D15**	**LSB**	**MSB**
Standby	H	×*1	×	×	High-Z	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Note: 1. ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{DD}	−0.3 to +5.5	V
All input and output voltage relative to V_{SS}	Vin, Vout	−0.3 to V_{DD} +0.3	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Temperature range under bias	Tbias	−20 to +85	°C

DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
Input low voltage	V_{IL}	−0.3	—	0.8	V

DC Characteristics (V_{DD} =2.7 V to 3.6 V, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Operating V_{DD} current	I_{DD}	—	20	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 200 ns
Standby V_{DD} current	I_{SB1}	—	20	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ −0.2 V
	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq$ 2.2 V
Input leakage current	$\|I_{IL}\|$	—	2	µA	Vin = 0 to V_{DD}
Output leakage current	$\|I_{OL}\|$	—	2	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{DD}
Output high voltage	V_{OH}	V_{DD} − 0.2	—	V	I_{OH} = −100 µA
Output low voltage	V_{OL}	—	0.2	V	I_{OL} = 100 µA

Capacitance (V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance	Cin	—	10	pF
Output capacitance	Cout	—	15	pF

AC Characteristics (V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

- Input pulse levels: 0.4 to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: 1TTL + C_L = 50 pF (including jig)

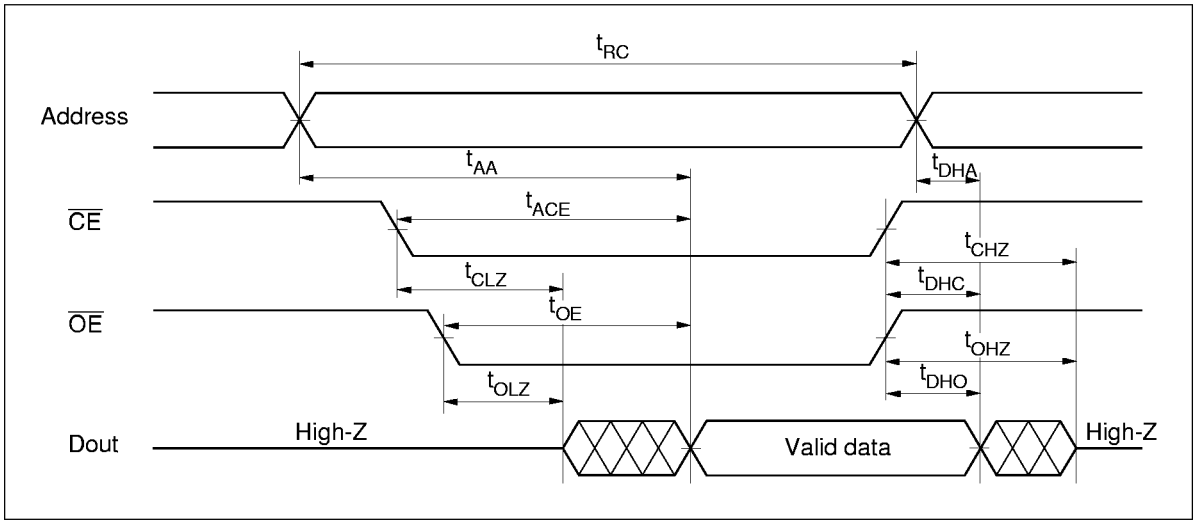
Read Cycle

		HN62V454-20			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	Notes
Read cycle time	t_{RC}	200	—	ns	
Address access time	t_{AA}	—	200	ns	3
$\overline{CE}$ access time	t_{ACE}	—	200	ns	3
$\overline{OE}$ access time	t_{OE}	—	70	ns	3
BHE access time	t_{BHE}	—	200	ns	
Output hold time from address change	t_{DHA}	0	—	ns	2
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	2
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	70	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	70	ns	1
BHE to output in high-Z	t_{BHZ}	—	70	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	4
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	ns	

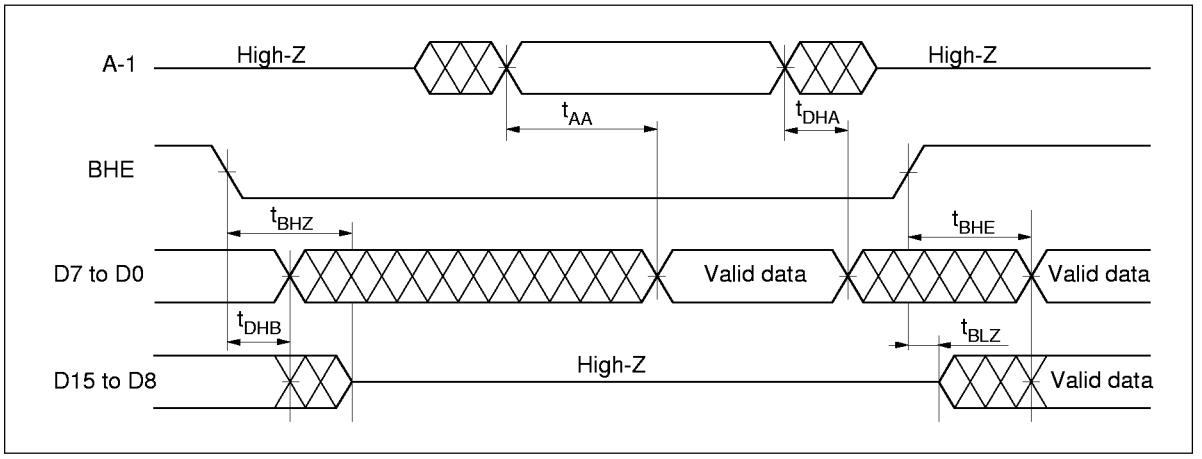
Notes: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
2. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
3. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
4. t_{CLZ}, t_{OLZ}: Determined by slower.
5. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
6. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must be applied to them.

Timing Waveforms

Word Mode (BHE = 'V_{IH}') **or Byte Mode** (BHE = 'V_{IL}')*[2, 3, 4]



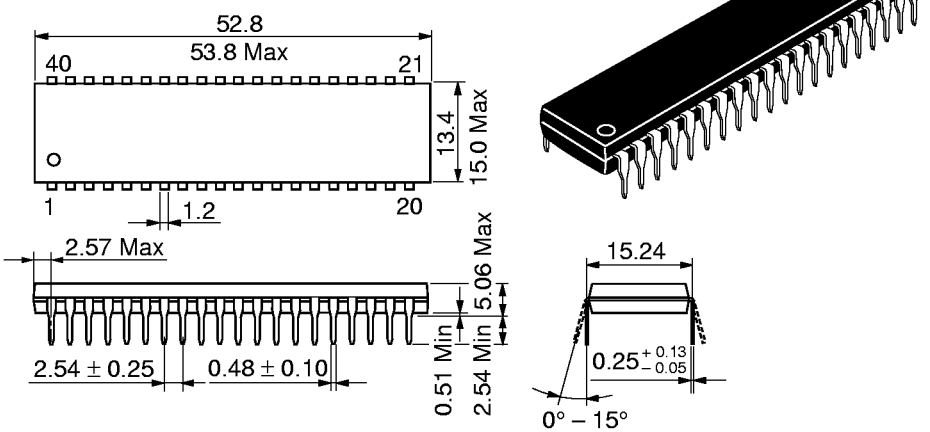
Word Mode, Byte Mode Switch*[5, 6]



Package Dimensions

HN62V454P Series (DP-40)

Unit: mm

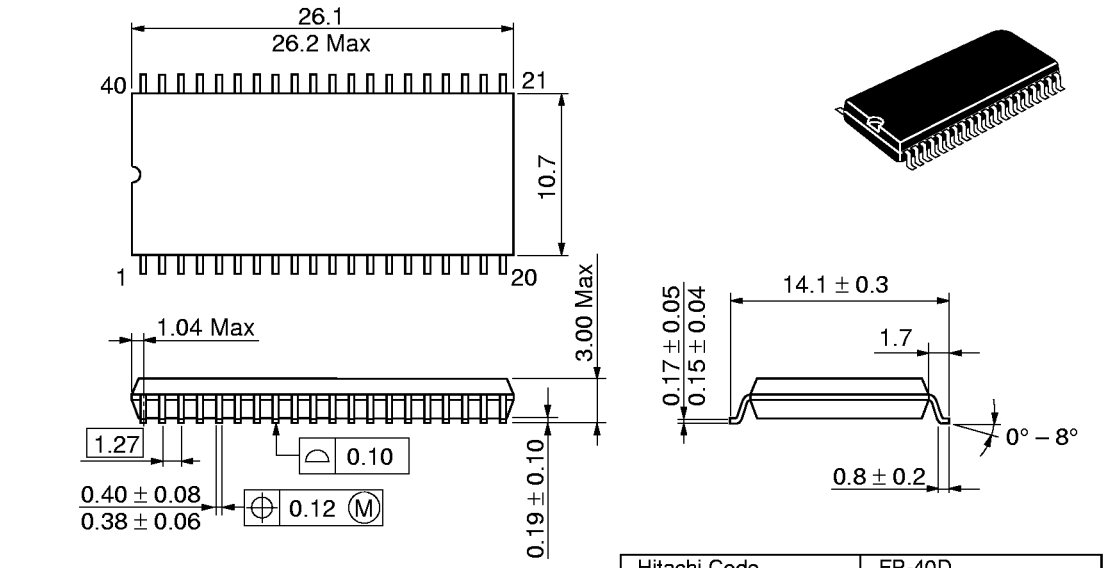


Hitachi Code	DP-40
JEDEC Code	MO-015J Mod.
EIAJ Code	SC-511-40D
Weight (reference value)	6.0 g

Package Dimensions (cont.)

HN62V454FA Series (FP-40D)

Unit: mm



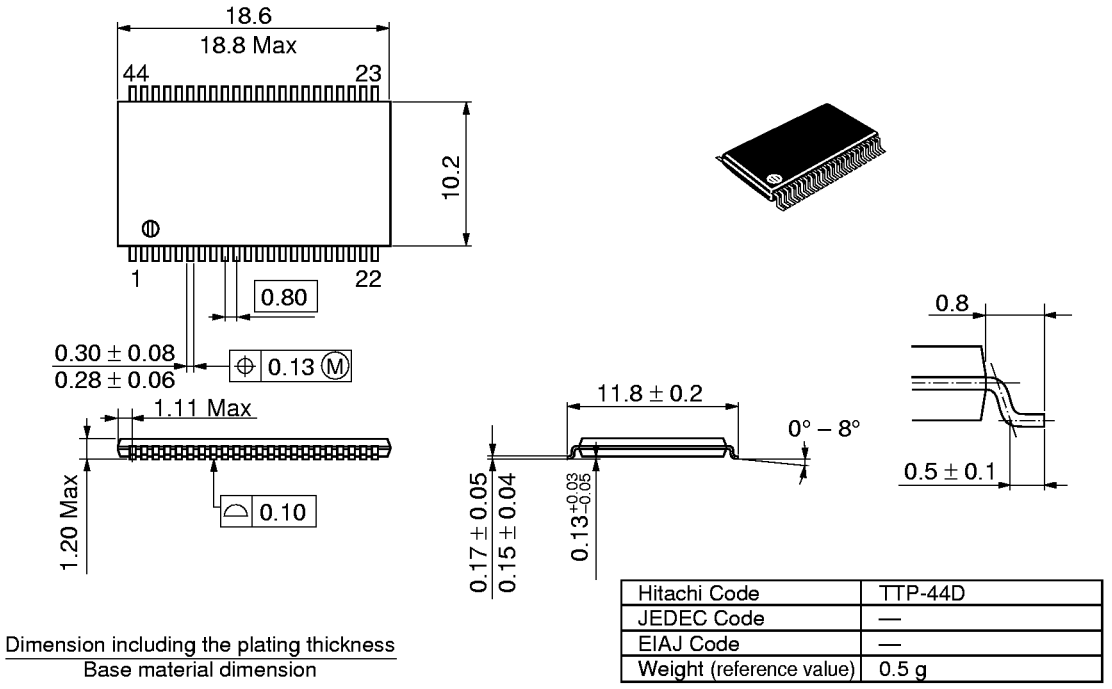
Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-40D
JEDEC Code	—
EIAJ Code	—
Weight (reference value)	1.5 g

Package Dimensions (cont.)

HN62V454TT Series (TTP-44D)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44D
JEDEC Code	—
EIAJ Code	—
Weight (reference value)	0.5 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jul. 4, 1996	Initial issue	M. Shirai	T. Wada
2.0	Jun. 26, 1997	Operation Table Deletion of note 2 Capacitance Deletion of note		