

HN62414, HN62434 Series

T-46-13-15

262144-word × 16-bit/524288-word × 8-bit CMOS MASK Programmable Read Only Memory

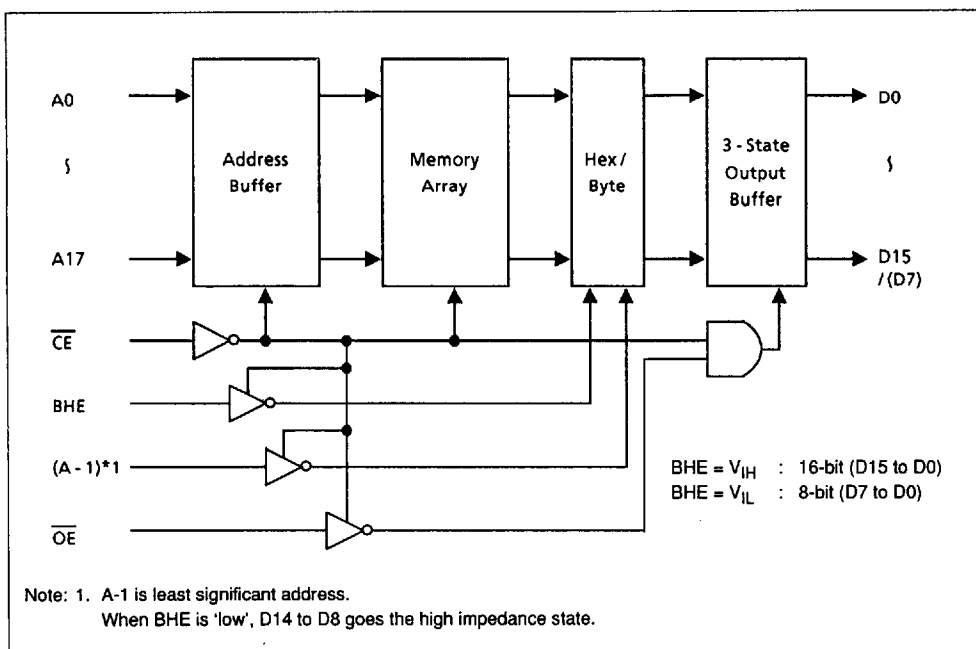
The HN62414, HN62434 is a 4-Mbit CMOS mask-programmable ROM organized either as 262144 words by 16 bits or as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

Features

- Single +5 V power supply
- Wired OR is permitted for the output in three status.
- TTL compatible
- Maximum access time : 120/150/170/200 ns (max)
- Low power consumption : 100 mW (typ) active
5 μ W (typ) standby
- Byte-wide or word-wide data organization with BHE

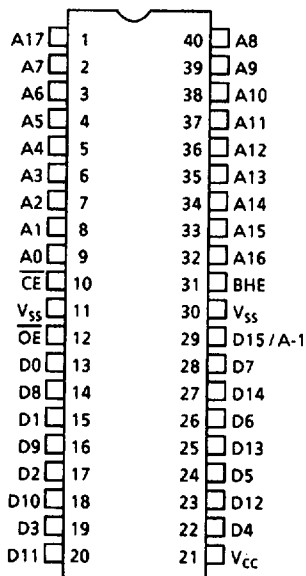
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Block Diagram



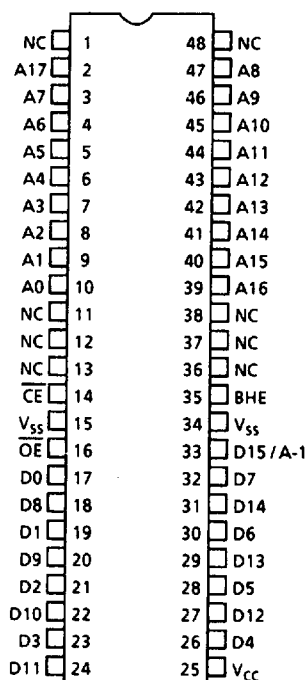
HN62414, HN62434 Series**HITACHI/ LOGIC/ARRAYS/MEM****Pin Arrangement**

• HN62414P, HN62434P



(Top View)

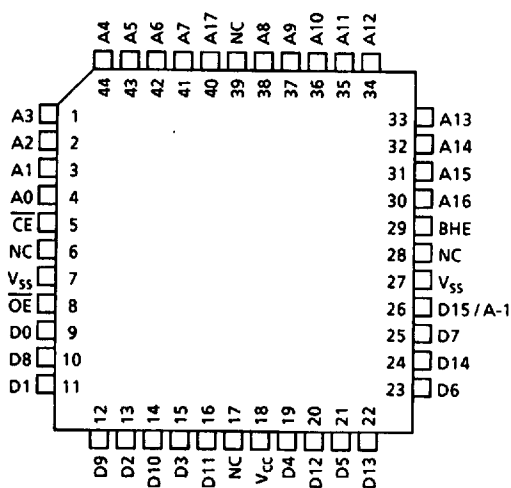
• HN62414F, HN62434F



(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

• HN62414FP, HN62434FP, HN62414TFP, HN62434TFP



(Top View)

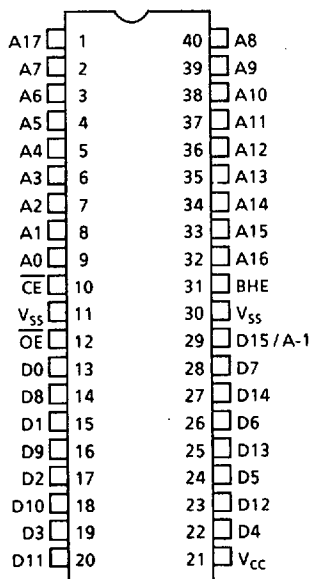
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Pin Arrangement (cont)

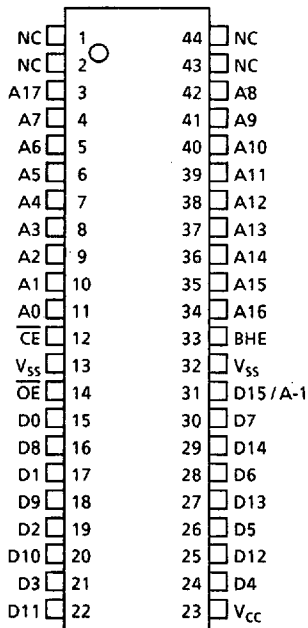
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• HN62414FA, HN62434FA

• HN62434TT, HN62414TT



(Top view)



(Top view)

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Ordering Information

Type No.	Access time	Package
HN62434P-12/-15/HN62414P-17/-20	120/150/170/200 ns	600 mil 40-pin plastic DIP (DP-40)
HN62434FP-12/-15/HN62414FP-17/-20	120/150/170/200 ns	44-pin plastic QFP (FP-44A)
HN62434F-12/-15/HN62414F-17/-20	120/150/170/200 ns	48-pin plastic SOP (FP-48DA)
HN62434TT-12/-15/HN62414TT-17/-20	120/150/170/200 ns	44-pin plastic TSOP-II (TTP-44D)
HN62434FA-12/-15/HN62414FA-17/-20	120/150/170/200 ns	40-pin plastic SOP (FP-40D)
HN62434TFP-12/-15/HN62414TFP-17/-20	120/150/170/200 ns	44-pin plastic TQFP (TFP-44)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
All input and output voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature range	T_{opr}	0 to +70	°C	
Storage temperature range	T_{stg}	-55 to +125	°C	
Temperature under bias	T_{bias}	-20 to +85	°C	

Note: 1. With respect to V_{SS} .

Recommended Operating Conditions ($V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

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DC Electrical Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	$V_{CC} = 5.5\text{ V}$, $I_{DOUT} = 0\text{ mA}$, $t_{RC} = \text{min}$
	Standby	I_{SB}	—	30	μA	$V_{CC} = 5.5\text{ V}$, $CE \geq V_{CC} - 0.2\text{ V}$
Input leakage current		$ I_{IL} $	—	10	μA	$V_{in} = 0\text{ to } V_{CC}$
Output leakage current		$ I_{OL} $	—	10	μA	$CE = 2.2\text{ V}$, $V_{out} = 0\text{ to } V_{CC}$
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -205\text{ }\mu\text{A}$
		V_{OL}	—	0.4	V	$I_{OL} = 1.6\text{ mA}$

Capacitance ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{IN} = 0\text{ V}$, $f = 1\text{ MHz}$)

Item	Symbol	Min	Max	Unit
Input capacitance	C_{IN}	—	15	pF
Output capacitance	C_{OUT}	—	15	pF

Note: This parameter is sampled and not 100% tested.

HN62414, HN62434 Series **HITACHI/ LOGIC/ARRAYS/MEM****AC Electrical Characteristics** ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$)

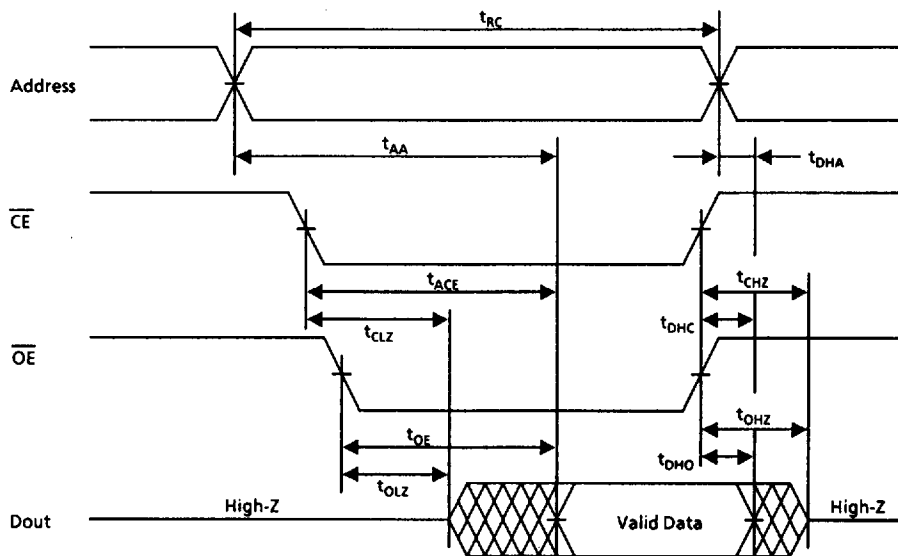
- Output load: 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level: 0.8 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

Item	Symbol	HN62434-12		HN62434-15		HN62414-17		HN62414-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	120	—	150	—	170	—	200	—	ns
Address access time	t_{AA}	—	120	—	150	—	170	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	—	170	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	70	—	70	—	100	ns
BHE access time	t_{BHE}	—	120	—	150	—	170	—	200	ns
Output hold time from address change	t_{DHA}	0	—	0	—	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	0	—	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}^{*1}	—	60	—	70	—	70	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}^{*1}	—	60	—	70	—	70	—	70	ns
BHE to output in high Z	t_{BHZ}^{*1}	—	60	—	70	—	70	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	10	—	10	—	10	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	10	—	10	—	10	—	ns
BHE to output in low Z	t_{BLZ}	5	—	10	—	10	—	10	—	ns

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Diagram

(1) Word Mode (BHE = 'VIH') or Byte Mode (BHE = 'VIL')

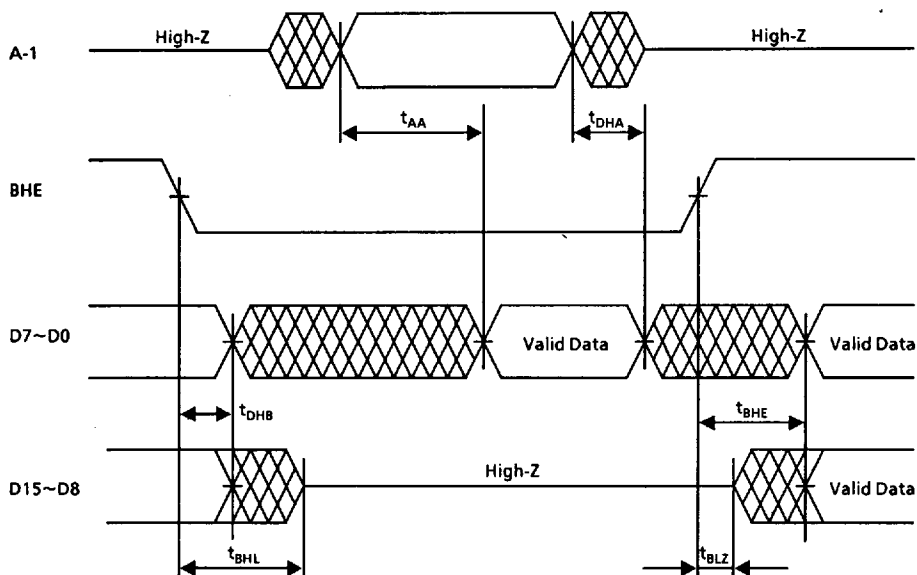


- Notes:
1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 3. t_{CLZ} , t_{OLZ} : Determined by slower.

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(2) Word Mode, Byte Mode Switch



- Notes:
1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
 2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not applied to them.