HI-8504

QUAD INVERTING HIGH VOLTAGE UP/DOWN LEVEL SHIFTER

General Description

The HI-8504 is a CMOS quad inverting level shifter which can perform either low to high voltage translation or high to low voltage translation depending on the power pin connections. Power pins VI + and VI- set the input voltage range, while VO + and VO- set the output voltage range. VSUB must be connected to the most positive voltage either VI+ or VO+. The HI-8504 is fabricated with silicon gate CMOS technology. In the quiescent state with input voltages near the rails, e.g., CMOS input levels, the translators consume no DC current, even while level shifting from 3V to 30V or vice versa. The HI-8504 finds typical application interfacing circuits operating at different supply voltages, such as 5V logic to ±15V analog.

Features

- **Low to high level translaltion, from 3V to 30V**
- **High to low level translation, from 30V to 3V**
- **Translation direction pin programmable**
- **Low power CMOS**
- **TTL, CMOS input and output compatibility**
- **Military temperature range and processing available**

Applications

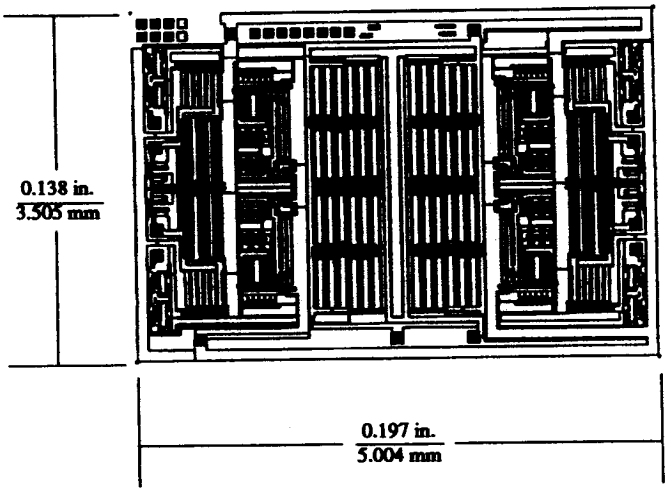
- Interface ±15V analog to 5V logic
- Drive high voltage displays from low level logic
- Level translate between subsystems

Ordering Information **

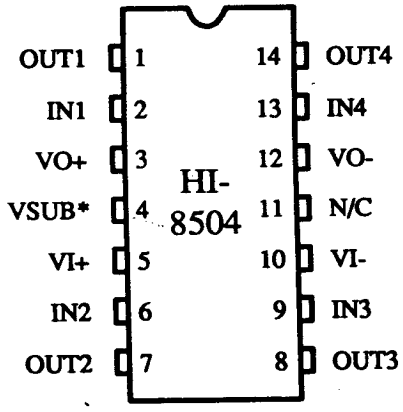
HI-8504P - Plastic DIP, 14 pin, Commercial
HI-8504C - Ceramic DIP, 14 pin, Commercial
HI-8504D - CERDIP, 14 pin, Commercial

** Other packaging and screening options available upon request

Chip Topography HI-8504



Pin Assignment



* VSUB pin must be connected to the most positive supply pin (VI+ or VO+).

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INTEGRATED CIRCUITS

Functional Description

Referring to Figure 1, each level shifter contains a two stage voltage translator. First, the input is translated to the desired positive output level, VO+. The only restrictions on this translation are:

$$3.0V \leq [(VO+) - (VI-)] \leq 30V$$

While

$$3.0V \leq [(VI+) - (VI-)] \leq 30V$$

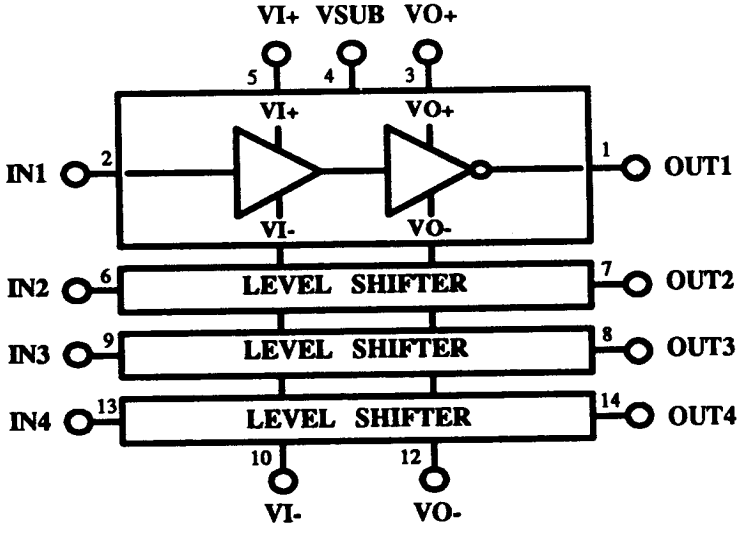
The next translator stage shifts the signal to the VO- output level. The only restriction is:

$$3.0V \leq [(VO+) - (VO-)] \leq 30V$$

The substrate pin, VSUB, must be connected to the most positive voltage of either VI+ or VO+. Failure to properly connect VSUB can cause permanent damage to the device.

***CAUTION:** For applications where [(VI+) - (VI-)] > 15V and the DC component of V_{IN} can be near [(VI+) - (VI-)] / 2, a current limiting resistor in series with VI- is necessary. For 30V applications, the a 1Kohm resistor is recommended.*

Functional Block Diagram



Schematic (Single Level Shifter)

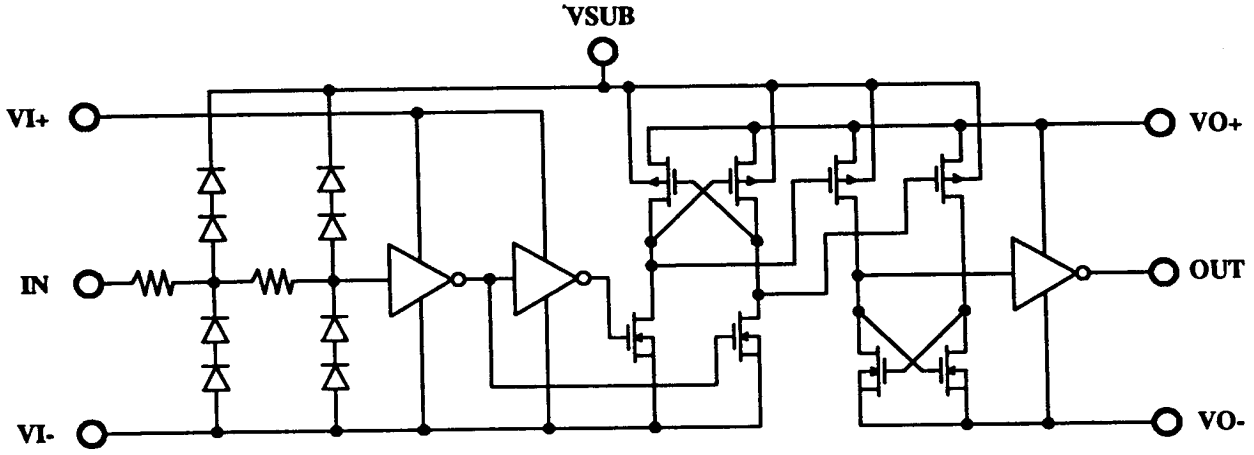


Figure 1

Pin Descriptions

Pin	Symbol	Function	Description	Pin	Symbol	Function	Description
1	OUT1	Output	Level Shifter #1 Output Pin	6	IN2	Input	Level Shifter #2 Input Pin
2	IN1	Input	Level Shifter #1 Input Pin	7	OUT2	Output	Level Shifter #2 Output Pin
3	VO+	Power	Output Positive Supply Pin	8	OUT3	Output	Level Shifter #3 Output Pin
4	VSUB	Power	Device Substrate. For VI+ ≥ VO+, Connect to VI+ (Pin 5). For VO+ > VI+, Connect to VO+ (Pin 3). Caution must be taken to properly connect the VSUB Pin. Failure to do so can result in permanent damage to the device.	9	IN3	Input	Level Shifter #3 Input Pin
				10	VI-	Power	Input Negative Suppl, Pin
				12	VO-	Power	Output Negative Supply Pin
				13	IN4	Input	Level Shifter #4 Input Pin
5	VI+	Power	Input Positive Supply Pin	14	OUT4	Output	Level Shifter #4 Output Pin

Absolute Maximum Ratings

Supply Voltages:	VI+ to VI- ..... -0.3V to +35V VI+ to VO- ..... -0.3V to +35V VO+ to VI- ..... -0.3V to +35V VO+ to VO- ..... -0.3V to +35V VSUB to VI- ..... -0.3V to +35V VSUB to VO- ..... -0.3V to +35V	DC Current Drain per Pin ..... 10 mA	
Voltage at any Input ..... (VI+) + 0.3V to (VI-) - O.3V		Power Dissipation per Package ..... 500 mW	
		Operating Temperature Range:	Plastic ..... -40°C to +85°C Ceramic ..... -55°C to +125°C
		Storage Temperature Range:	Plastic ..... -50°C to +150°C Ceramic ..... -65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

T_A = -55°C to +125°C (Unless Otherwise Specified)

Parameter	Symbol	VI+	VI-	VO+	VO-	VSUB	Conditions	Min	Typ	Max	Units
Output Voltage Low Level	V_{OL}	5V	0V	10V	0V	10V	V_{IH} = VI+, V_{IL} = VI-	-	0.0	0.05	V
		5V	0V	15V	-15V	15V	V_{IH} = VI+, V_{IL} = VI-	-	-15.0	-14.95	V
		15V	-15V	5V	0V	15V	V_{IH} = VI+, V_{IL} = VI-	-	0.0	0.05	V
		15V	-15V	5V	-5V	15V	V_{IH} = VI+, V_{IL} = VI-	-	-5.0	-4.95	V
Output Voltage High Level	V_{OH}	5V	0V	10V	0V	10V	V_{IH} = VI+, V_{IL} = VI-	9.95	10.0	-	V
		5V	0V	15V	-15V	15V	V_{IH} = VI+, V_{IL} = VI-	14.95	15.0	-	V
		15V	-15V	5V	0V	15V	V_{IH} = VI+, V_{IL} = VI-	4.95	5.0	-	V
		15V	-15V	5V	-5V	15V	V_{IH} = VI+, V_{IL} = VI-	4.95	5.0	-	V
Output Sink Current	I_{OL}	5V	0V	10V	0V	10V	V_{OL} = 0.05V	-0.15	-0.35	-	mA
		5V	0V	15V	-15V	15V	V_{OL} = -14.95V	-0.20	-0.55	-	mA
		15V	-15V	5V	0V	15V	V_{OL} = 0.05V	-0.10	-0.24	-	mA
		15V	-15V	5V	-5V	15V	V_{OL} = -4.95V	-0.15	-0.35	-	mA
Output Source Current	I_{OH}	5V	0V	10V	0V	10V	V_{OH} = 9.95V	0.12	0.36	-	mA
		5V	0V	15V	-15V	15V	V_{OH} = 14.95V	0.16	0.47	-	mA
		15V	-15V	5V	0V	15V	V_{OH} = 4.95V	0.04	0.16	-	mA
		15V	-15V	5V	-5V	15V	V_{OH} = 4.95V	0.09	0.28	-	mA
Input Low Voltage	V_{IL}	5V	0V	10V	0V	10V		-	-	1.2	V
		5V	0V	15V	-15V	15V		-	-	1.2	V
		15V	-15V	5V	0V	15V		-	-	-12.0	V
		15V	-15V	5V	-5V	15V		-	-	-12.0	V
Input High Voltage	V_{IH}	5V	0V	10V	0V	10V		3.2	-	-	V
		5V	0V	15V	-15V	15V		3.2	-	-	V
		15V	-15V	5V	0V	15V		12.0	-	-	V
		15V	-15V	5V	-5V	15V		12.0	-	-	V
Input Current	I_{IN}	15V	-15V	-	-	15V		-	-	1.0	µA
Input Capacitance	C_{IN}	-	-	-	-	-		-	35	-	pf
Quiesent Current - Input Supply	I_{VI}	30V	0V	30V	0V	30V	T_A = +25°C	-	0.001	0.1	µA
		30V	0V	30V	0V	30V	T_A = +85°C	-	0.01	1.0	µA
		30V	0V	30V	0V	30V	T_A = +125°C	-	0.1	10	µA
Quiesent Current - Output Supply	I_{VO}	30V	0V	30V	0V	30V	T_A = +25°C	-	0.001	0.1	µA
		30V	0V	30V	0V	30V	T_A = +85°C	-	0.01	1.0	µA
		30V	0V	30V	0V	30V	T_A = +125°C	-	0.1	10	µA
Quiesent Current - Substrate	I_{SUB}	30V	0V	30V	0V	30V	T_A = +25°C	-	0.01	1	µA
		30V	0V	30V	0V	30V	T_A = +85°C	-	0.1	10	µA
		30V	0V	30V	0V	30V	T_A = +125°C	-	2	30	µA

AC Electrical Characteristics

C_L = 50 pf, $t_{ir} = t_{if}$ = 100ns, T_A = -55°C to +125°C (Unless Otherwise Specified)

Parameter	Symbol	VI+	VI-	VO+	VO-	VSUB	Conditions	Min	Typ	25°C Max	125°C Max	Units
Propagation Delay (High to Low)	t_{PHL}	15V	-15V	5V	0V	15V		-	0.8	2.0	3.0	µs
		5V	0V	15V	-15V	5V		-	0.4	1.0	1.5	µs
Propagation Delay (Low to High)	t_{PLH}	15V	-15V	5V	0V	15V		-	1.1	2.5	3.5	µs
		5V	0V	15V	-15V	5V		-	0.6	1.5	2.0	µs
Output rise and fall time	t_{or}, t_{of}	15V	-15V	5V	0V	15V		-	200	500	700	ns
		5V	0V	15V	-15V	5V		-	80	200	350	ns
Dynamic Current	I_{VI}	15V	-15V	5V	0V	15V	f=100KHz	-	0.6	-	-	mA
		15V	-15V	5V	0V	15V	f=500KHz	-	2.0	-	-	mA
		5V	0V	15V	-15V	15V	f=100KHz	-	0.03	-	-	mA
		5V	0V	15V	-15V	15V	f=500KHz	-	0.15	-	-	mA
	I_{VO}	15V	-15V	5V	0V	15V	f=100KHz	-	0.14	-	-	mA
		15V	-15V	5V	0V	15V	f=500KHz	-	0.7	-	-	mA
		5V	0V	15V	-15V	15V	f=100KHz	-	1.9	-	-	mA
		5V	0V	15V	-15V	15V	f=500KHz	-	9.7	-	-	mA
	I_{SUB}	15V	-15V	5V	0V	15V	f=100KHz	-	0.5	-	-	mA
		15V	-15V	5V	0V	15V	f=500KHz	-	2.9	-	-	mA
		5V	0V	15V	-15V	15V	f=100KHz	-	0.2	-	-	mA
		5V	0V	15V	-15V	15V	f=500KHz	-	1.2	-	-	mA

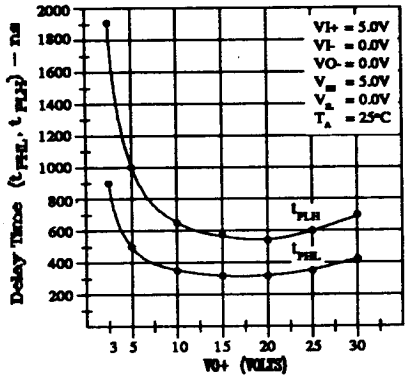


Fig. 2 Typical Delay Time for UP Conversion as a Function of Output Positive Reference Supply Voltage.

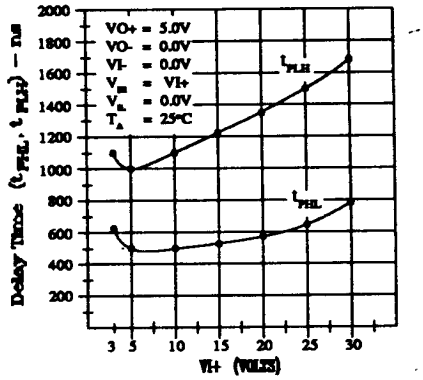
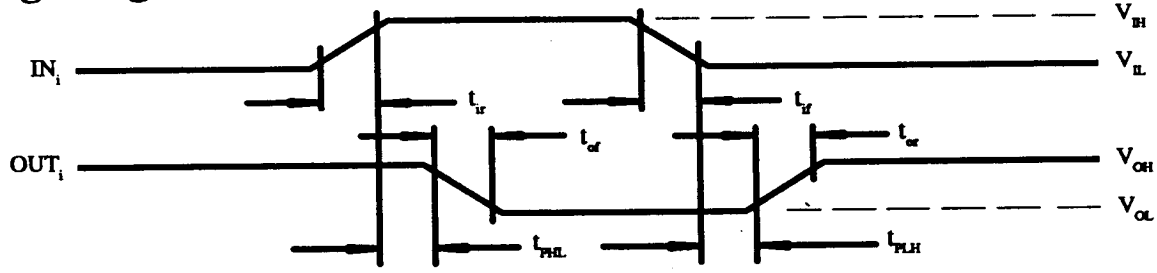


Fig. 3 Typical Delay Time for DOWN Conversion as a Function of Input Positive Reference Supply Voltage.

Timing Diagram



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