High-Performance
8K×8
CMOS SRAM

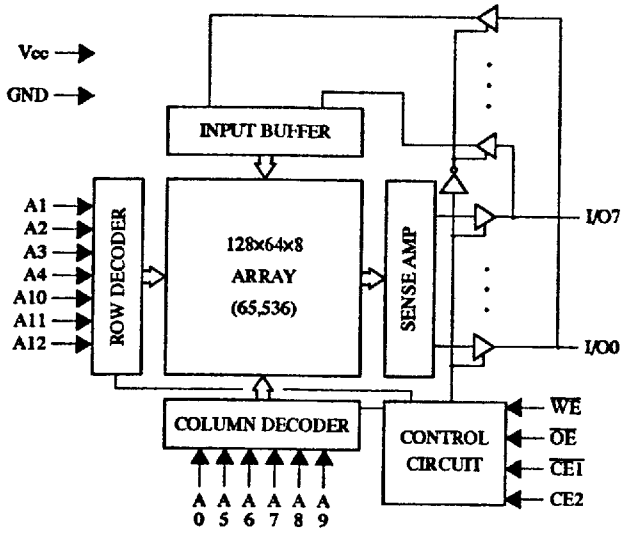
AS7C164
AS7C164L

8K×8 CMOS SRAM (Common I/O)

FEATURES

- Organization: 8,192 words × 8 bits
- High speed
  - 10/12/15/20/25 ns address access time
  - 3/3/4/5/6 ns output enable access time
- Low power consumption
  - Active: 633 mW max (10 ns cycle)
  - Standby: 11 mW max, CMOS I/O
    1.1 mW max, CMOS I/O, L version
  - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Very fast 3 ns output enable access time
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
- ESD protection > 2000 volts
- Latch-up current > 200 mA

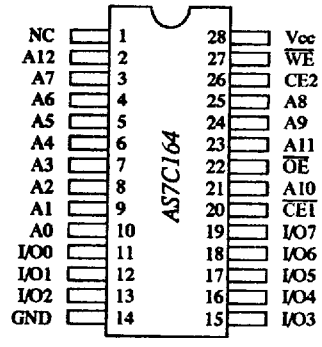
LOGIC BLOCK DIAGRAM



AS7C164-01

PIN ARRANGEMENT

DIP, SOJ



AS7C164-02

SELECTION GUIDE

		7C164-10	7C164-12	7C164-15	7C164-20	7C164-25	Unit
Maximum Address Access Time		10	12	15	20	25	ns
Maximum Output Enable Access Time		3	3	4	5	6	ns
Maximum Operating Current		115	110	100	90	80	mA
Maximum CMOS Standby Current		2.0	2.0	2.0	2.0	2.0	mA
	L	0.2	0.2	0.2	0.2	0.2	mA

FUNCTIONAL DESCRIPTION

The AS7C164 is a high performance CMOS 65,536-bit Static Random Access Memory (SRAM) organized as 8,192 words x 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20/25 ns with output enable access times (t_{OE}) of 3/3/4/5/6 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. The standard AS7C164 is guaranteed not to exceed 11.0 mW power consumption in standby mode; the L version is guaranteed not to exceed 1.1 mW, and typically requires only 250 µW. The L version also offers 2.0V data retention, with maximum power of 120 µW.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C164 is packaged in all high volume industry standard packages.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	-	1.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	°C
Temperature Under Bias	T_{bias}	-10	+85	°C
DC Output Current	I_{out}	-	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output Disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

RECOMMENDED OPERATING CONDITIONS (T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	-	V_{CC}+1	V
	V_{IL}	-0.5*	-	0.8	V

* V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$.

DC OPERATING CHARACTERISTICS [1] (V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions		-10		-12		-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}		-	1	-	1	-	1	-	1	-	1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE1}$ = V_{IH} *or* CE2 = V_{IL}, V_{CC} = Max, V_{out} = GND to V_{CC}		-	1	-	1	-	1	-	1	-	1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $f = f_{max}$, I_{out} = 0 mA		-	115	-	110	-	100	-	90	-	80	mA
			L	-	110	-	105	-	95	-	95	-	75	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1}$ = V_{IH} *or* CE2 = V_{IL}, $f = f_{max}$		-	35	-	30	-	25	-	25	-	20	mA
			L	-	30	-	25	-	20	-	20	-	15	mA
	I_{SB1}	$\overline{CE1} \geq V_{CC}$-0.2V *or* CE2 ≤ 0.2V, $V_{in} \leq 0.2V$ *or* $V_{in} \geq V_{CC}$-0.2V, f = 0		-	2.0	-	2.0	-	2.0	-	2.0	-	2.0	mA
			L	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	mA
Output Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
	V_{OH}	I_{OH} = -4 mA, V_{CC} = Min		2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V

CAPACITANCE [2] (f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O Capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

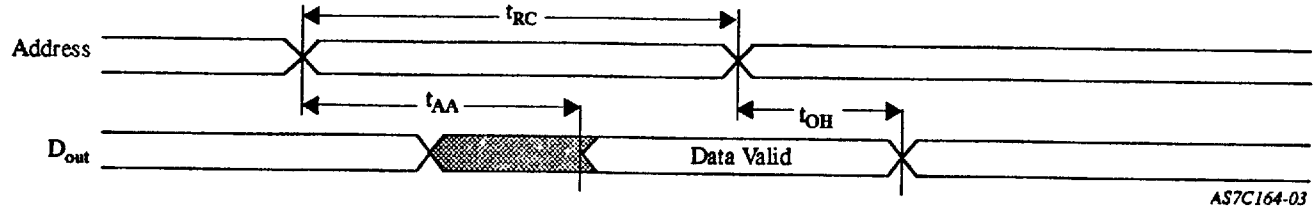
READ CYCLE [3, 9, 12]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-10		-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	10	-	12	-	15	-	20	-	25	-	ns	
Address Access Time	t_{AA}	-	10	-	12	-	15	-	20	-	25	ns	3
Chip Enable ($\overline{CE1}$) Access Time	t_{ACE1}	-	10	-	12	-	15	-	20	-	25	ns	3, 12
Chip Enable (CE2) Access Time	t_{ACE2}	-	10	-	12	-	15	-	20	-	25	ns	3, 12
Output Enable ($\overline{OE}$) Access Time	t_{OE}	-	3	-	3	-	4	-	5	-	6	ns	
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	3	-	ns	5
$\overline{CE1}$ LOW to Output in Low Z	t_{CLZ1}	3	-	3	-	3	-	3	-	3	-	ns	4, 5, 12
CE2 HIGH to Output in Low Z	t_{CLZ2}	3	-	3	-	3	-	3	-	3	-	ns	4, 5, 12
$\overline{CE1}$ HIGH to Output in High Z	t_{CHZ1}	-	3	-	3	-	4	-	5	-	6	ns	4, 5, 12
CE2 LOW to Output in High Z	t_{CHZ2}	-	3	-	3	-	4	-	5	-	6	ns	4, 5, 12
$\overline{OE}$ LOW to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	0	-	ns	4, 5
$\overline{OE}$ HIGH to Output in High Z	t_{OHZ}	-	3	-	3	-	4	-	5	-	6	ns	4, 5
Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	0	-	ns	4, 5, 12
Power Down Time	t_{PD}	-	10	-	12	-	15	-	20	-	25	ns	4, 5, 12

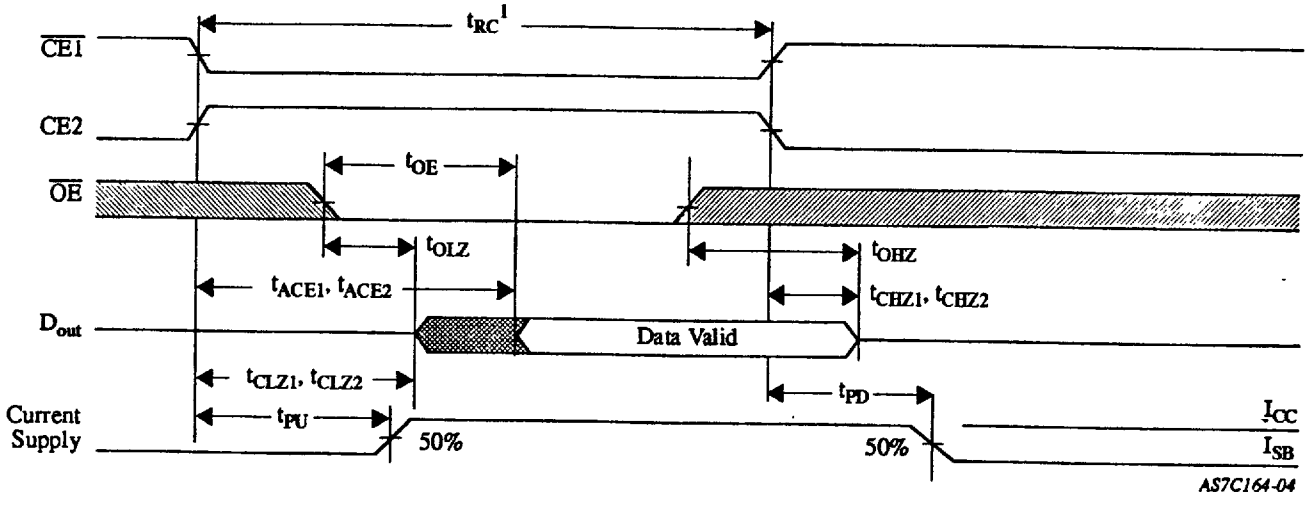
TIMING WAVEFORM OF READ CYCLE 1 [3, 6, 7, 9, 12]

(Address Controlled)



TIMING WAVEFORM OF READ CYCLE 2 [3, 6, 8, 9, 12]

($\overline{CE1}$ and CE2 Controlled)

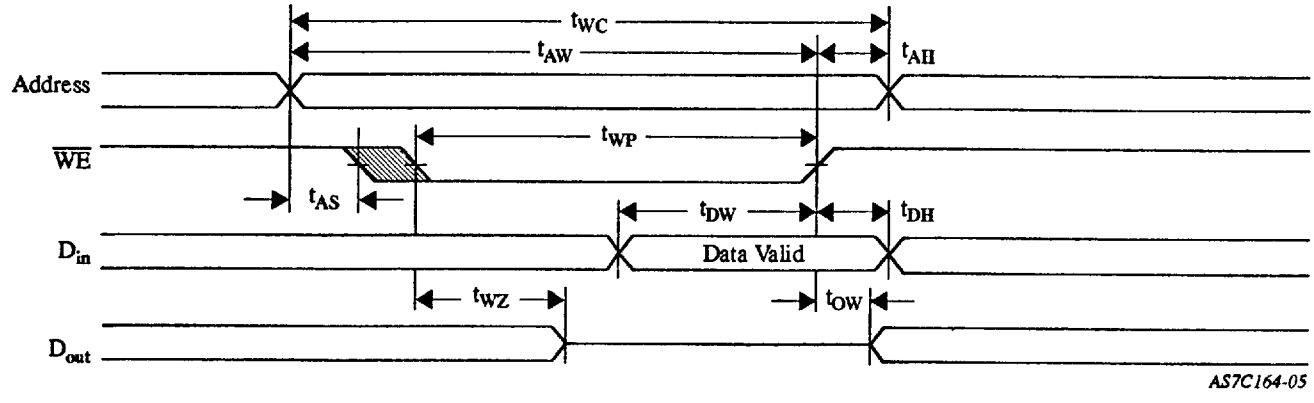


WRITE CYCLE [11, 12]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

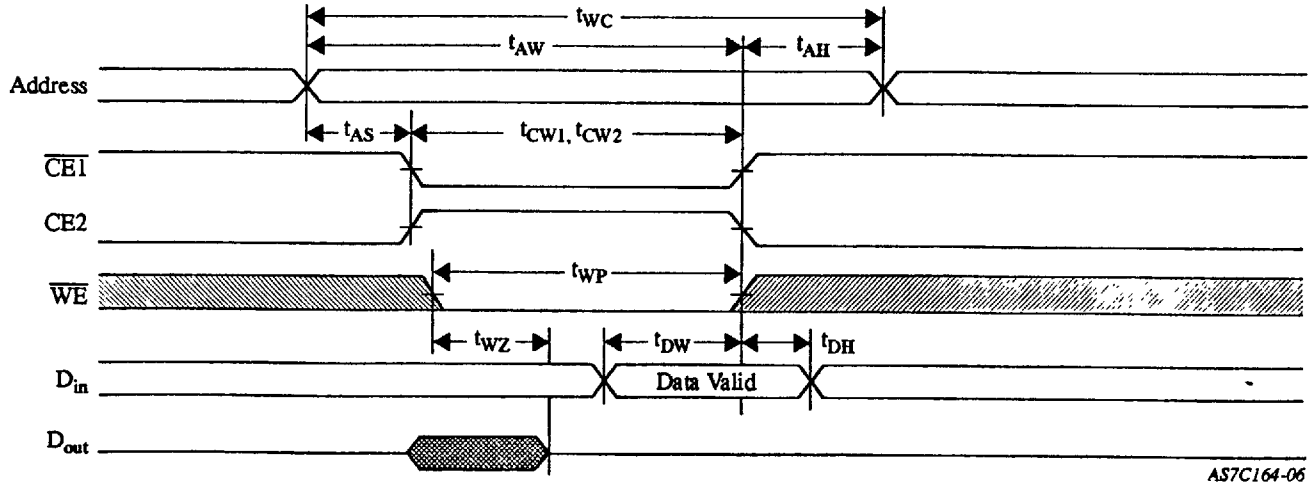
Parameter	Symbol	-10		-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	10	-	12	-	15	-	20	-	20	-	ns	
Chip Enable ($\overline{CE1}$) to Write End	t_{CW1}	8	-	9	-	10	-	12	-	15	-	ns	12
Chip Enable (CE2) to Write End	t_{CW2}	8	-	9	-	10	-	12	-	15	-	ns	12
Address Setup to Write End	t_{AW}	8	-	9	-	10	-	12	-	15	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	0	-	ns	12
Write Pulse Width	t_{WP}	7	-	8	-	9	-	12	-	15	-	ns	
Address Hold From End of Write	t_{AH}	0	-	0	-	0	-	0	-	0	-	ns	
Data Valid to Write End	t_{DW}	6	-	6	-	7	-	8	-	10	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	0	-	ns	4, 5
Write Enable to Output in High Z	t_{WZ}	-	5	-	5	-	5	-	5	-	5	ns	4, 5
Output Active From Write End	t_{OW}	2	-	3	-	3	-	3	-	3	-	ns	4, 5

TIMING WAVEFORM OF WRITE CYCLE 1 [10, 11, 12] ($\overline{WE}$ Controlled)



AS7C164-05

TIMING WAVEFORM OF WRITE CYCLE 2 [10, 11, 12] ($\overline{CE1}$ and CE2 Controlled)

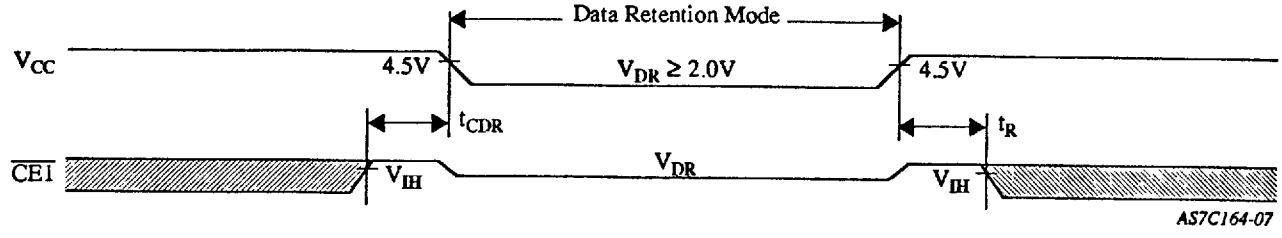


AS7C164-06

DATA RETENTION CHARACTERISTICS (L Version Only)

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	V_{CC} = 2.0V	2.0	-	V
Data Retention Current	I_{CCDR}	$\overline{CE1} \geq V_{CC}$-0.2V *or* CE2 ≤ 0.2V	-	60	µA
Chip Enable to Data Retention Time	t_{CDR}		0	-	ns
Operation Recovery Time	t_R	$V_{in} \geq V_{CC}$-0.2V *or* $V_{in} \leq$ 0.2V	t_{RC}	-	ns
Input Leakage Current	$\|I_{LI}\|$		-	1	µA

DATA RETENTION WAVEFORM (L Version Only)



AS7C164-07

AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

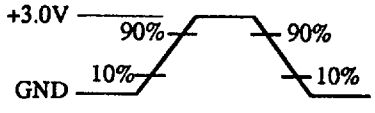


Figure A: Input Waveform
AS7C164-08

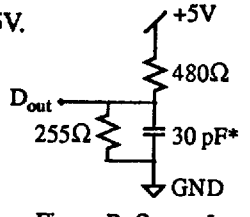
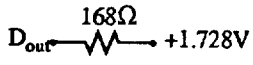
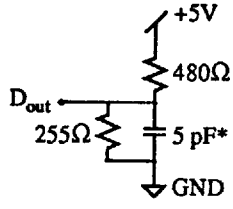


Figure B: Output Load
AS7C164-09

Thevenin equivalent:





*including scope and jig capacitance

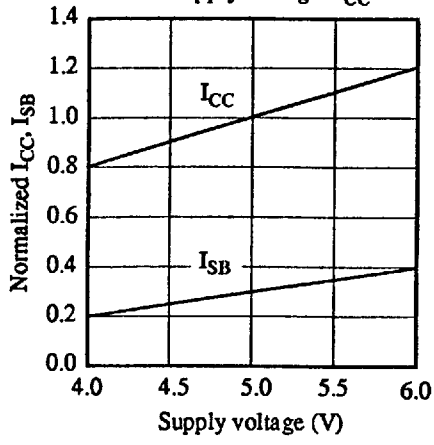
Figure C: Output Load for t_{CLZ}, t_{CHZ}
AS7C164-10

NOTES

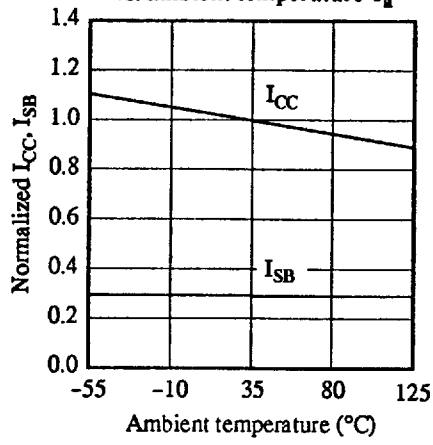
1. During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see *AC Test Conditions*, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW and CE2 transition HIGH.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.
12. $\overline{CE1}$ and CE2 have identical timing.

TYPICAL DC AND AC CHARACTERISTICS

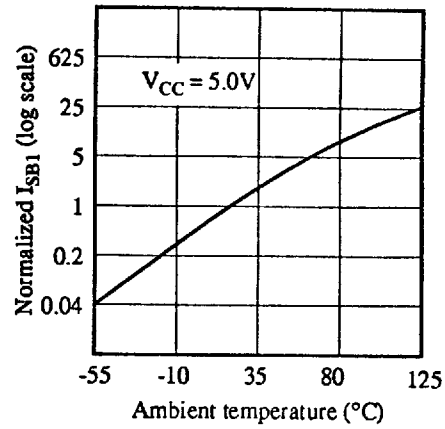
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



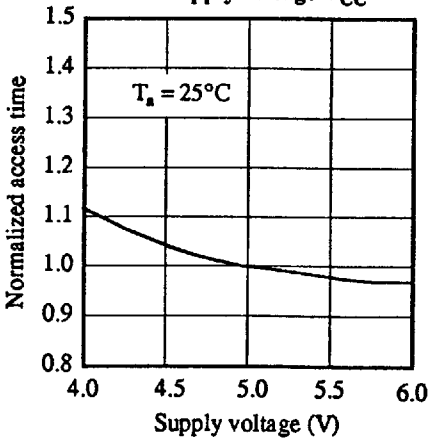
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



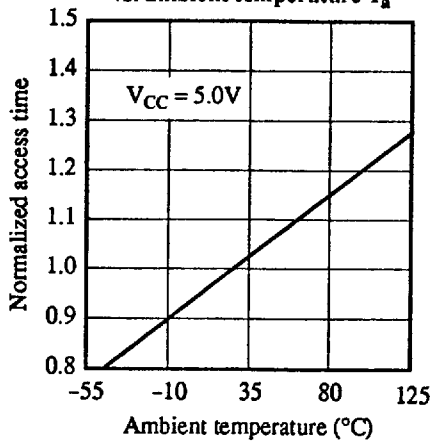
Normalized supply current I_{SB1} vs. ambient temperature T_a



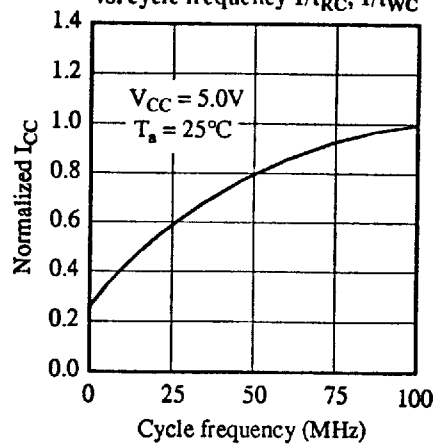
Normalized access time t_{AA} vs. supply voltage V_{CC}



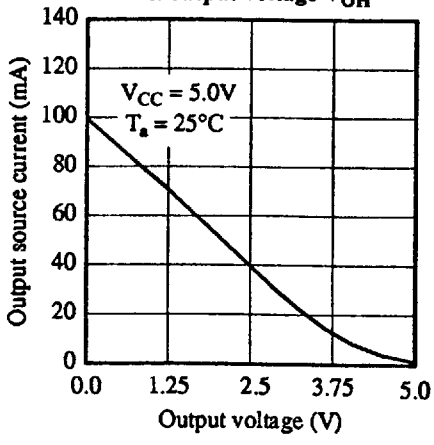
Normalized access time t_{AA} vs. ambient temperature T_a



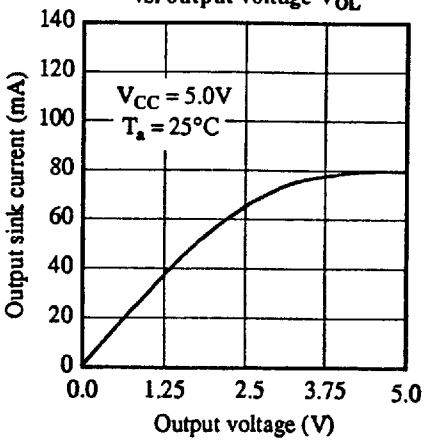
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



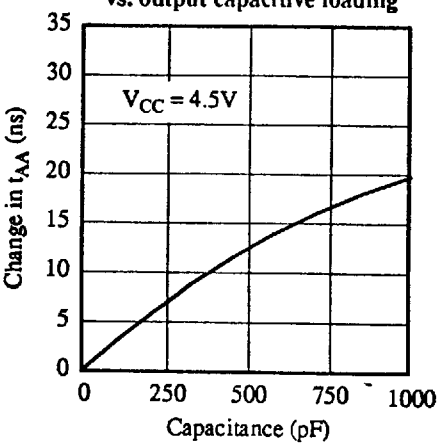
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



AS7C164-11

ORDERING CODES

Package \ Access Time	10 ns	12 ns	15 ns	20 ns	25 ns
Plastic DIP, 300 mil	AS7C164-10PC AS7C164L-10PC	AS7C164-12PC AS7C164L-12PC	AS7C164-15PC AS7C164L-15PC	AS7C164-20PC AS7C164L-20PC	AS7C164-25PC AS7C164L-25PC
Plastic SOJ, 300 mil	AS7C164-10JC AS7C164L-10JC	AS7C164-12JC AS7C164L-12JC	AS7C164-15JC AS7C164L-15JC	AS7C164-20JC AS7C164L-20JC	AS7C164-25JC AS7C164L-25JC

PART NUMBERING SYSTEM

AS7C	164	X	-XX	X	C
SRAM Prefix	Device Number	Blank = Standard Power L = Low Power	Access Time	Package: P = PDIP 300 mil J = SOJ 300 mil	Commercial Temperature Range, 0°C to 70°C

REPRESENTATIVES, DISTRIBUTORS, AND SALES OFFICES

DOMESTIC REPS

ALABAMA
Concord Component
(205) 772-8883

ARIZONA
Competitive Technology
(602) 265-9224

ARKANSAS
Southern States Marketing
(501) 922-0807

CALIFORNIA
North: Brooks Technical
(415) 960-3880
South: Competitive Tech.
(714) 540-5501

COLORADO
Megatronix
(303) 730-6262

CONNECTICUT
Kitchen & Kutchin Inc.
(203) 239-0212

DELAWARE
Vantage Sales
(609) 424-6777

FLORIDA
Micro-Electronic Comp.
(305) 426-8944

GEORGIA
Concord Component
(404) 416-9597

HAWAII
Brooks Technical
(415) 960-3880

IDAHO
E²/Electronic Solutions
(503) 292-8204

ILLINOIS
El-Mech
(312) 794-9100

INDIANA
CC Electro Sales
(317) 921-5000

KENTUCKY
CC Electro Sales
(317) 921-5000

LOUISIANA
Southern States Marketing
North: (501) 922-0807
South: (713) 868-5780

MAINE
Kitchen & Kutchin Inc.
(617) 229-2660

MARYLAND
Beacon North Inc.
(703) 478-2480

MASSACHUSETTS
Kitchen & Kutchin Inc.
(617) 229-2660

MICHIGAN
Enco Group
(313) 338-8600

MINNESOTA
D. A. Case Associates
(612) 831-6777

MISSISSIPPI
Concord Component
(205) 772-8883

MONTANA
E²/Electronic Solutions
(206) 637-0302

NEVADA
North: Brooks Technical
(916) 965-3255
South: Competitive Tech.
(602) 265-9224

NEW HAMPSHIRE
Kitchen & Kutchin Inc.
(617) 229-2660

NEW JERSEY
North: ERA Associates
(800) 645-5500
South: Vantage Sales
(609) 424-6777

NEW MEXICO
Competitive Technology
(602) 265-9224

NEW YORK
NYC: ERA Associates
(516) 543-0510
Upstate: Tri-Tech
(716) 385-6500

NORTH CAROLINA
Concord Component
(919) 846-3441

NORTH DAKOTA
D. A. Case Associates
(612) 831-6777

OHIO
Midwest Marketing Assoc.
Lyndhurst: (216) 381-8575
Dayton: (513) 433-2511

OKLAHOMA
Southern States Marketing
(214) 238-7500

OREGON
E²/Electronic Solutions
(503) 292-8204

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East: Vantage Sales
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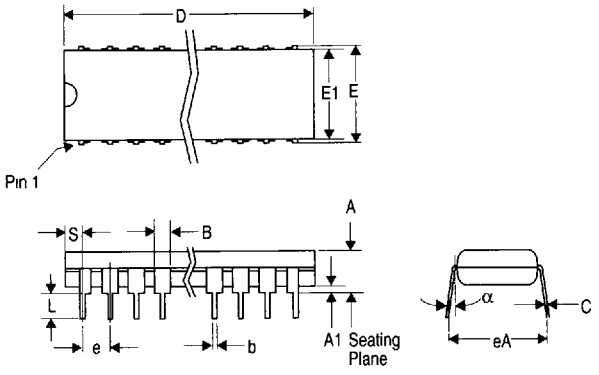
Printed in U.S.A.

June 1994

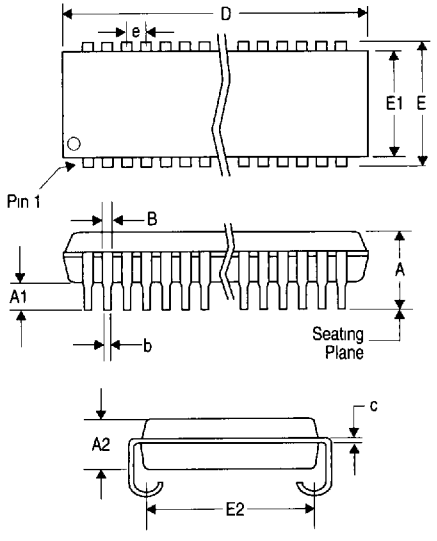
Plastic Dual In-line Package (PDIP)



	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max
A	–	0.175	–	0.175	–	0.180	–	0.200
A1	0.010	–	0.010	–	0.020	–	0.015	–
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022
C	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015
D	–	0.980	–	1.400	1.560	1.570	1.610	1.620
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.330	0.370
L	0.110	0.130	0.120	0.140	0.125	0.135	0.115	0.160
α	0°	15°	0°	15°	0°	15°	0°	15°
S	–	0.040	–	0.055	–	0.038	–	0.040

Dimensions in inches

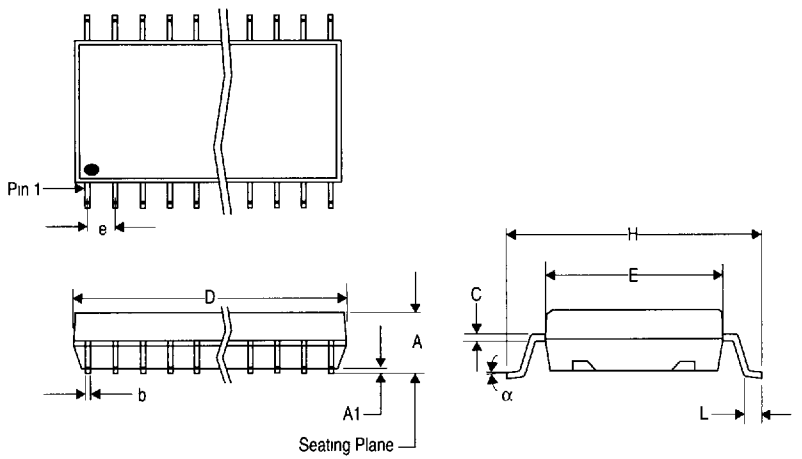
Plastic Small Outline J-Bend (SOJ)



	20/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil		40-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	–	0.140	–	0.140	–	0.145	–	0.145	–	0.145
A1	0.020	–	0.025	–	0.025	–	0.025	–	0.025	–
A2	0.095	0.105	0.095	0.105	0.086	0.094	0.086	0.090	0.086	0.115
B	0.026	0.032	0.028 TYP		0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.018 TYP		0.014	0.020	0.015	0.020	0.015	0.022
c	0.008	0.014	0.010 TYP		0.006	0.013	0.007	0.013	0.007	0.014
D	–	0.686	–	0.730	0.820	0.830	0.820	0.830	1.015	1.035
E	0.327	0.347	0.327	0.347	0.330	0.340	0.435	0.445	0.435	0.445
E1	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405
E2	0.245	0.285	0.245	0.285	0.250	0.275	0.360	0.380	0.378	0.390
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	

Dimensions in inches

Plastic Small Outline Gull-Wing IC (SOIC)



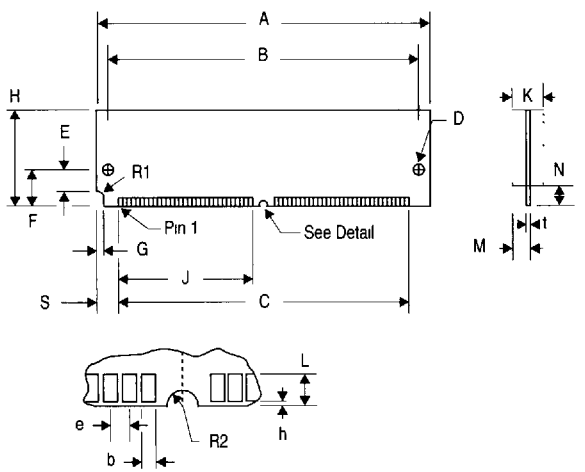
32-pin 525 mil

	Min	Max
A	–	0.118
A1	0.002	
b	0.014	0.020
C	0.008	0.012
D	0.801	0.811
e	0.050 BSC	
E	0.445	0.455
H	0.546	0.570
	0.026	0.036
α	0°	8°

Dimensions in inches

PRELIMINARY

Single In-Line Memory Module (SIMM)



64 dual readout

	Min	Max
A	3.840	3.860
B	3.584 TYP	
b	0.040	0.042
C	3.350 TYP	
D	0.123	0.127
E	0.150 TYP	
e	0.050 BSC	
F	0.400 TYP	
G	0.075	0.085
H	–	1.125
h	–	0.010
J	1.550 TYP	
K	–	0.360

64 dual cont'd

	Min	Max
L	0.100	–
M	–	0.208
N	0.225	–
R1	0.060	0.064
R2	0.060	0.064
S	0.250 TYP	
t	0.045	0.055

Dimensions in inches