AKN62414 Series
AKN62434 Series

262144-Word × 16-Bit/524288-Word × 8-Bit CMOS Mask Programmable ROM

AKN62414, AKN62434 Series is a 4-Mbit CMOS mask-programable ROM organized either as 262144-word x 16-bit or as 524288-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

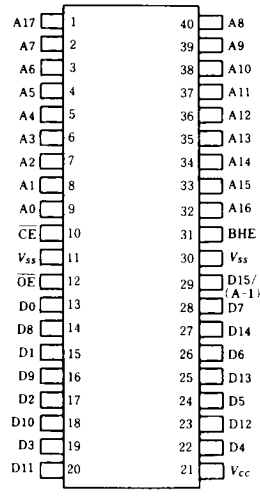
Features

- Single +5V power supply
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/170/200 ns (max)
- Low power consumption: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization(switched by BHE terminal)

Ordering Information

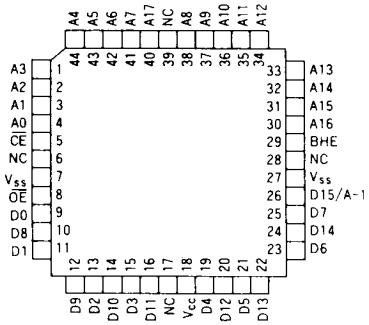
Type No.	Address Access time	Package
AKN62414P-20	200 ns	600 mil 40-pin plastic DIP
AKN62414P-17	170 ns	
AKN62434P	150 ns	
AKN62414FP-20	200 ns	44-pin plastic QFP
AKN62414FP-17	170 ns	
AKN62434FP	150 ns	
AKN62414F-20	200 ns	48 pin plastic SOP
AKN62414F-17	170 ns	
AKN62434F	150 ns	
AKN62414FS-20	200 ns	64-pin plastic QFP
AKN62414FS-17	170 ns	
AKN62434FS	150 ns	
AKN62414FA-20	200 ns	40-pin plastic SOP
AKN62414FA-17	170 ns	
ANK62434FA	150 ns	

AKN62414P, AKN62434P



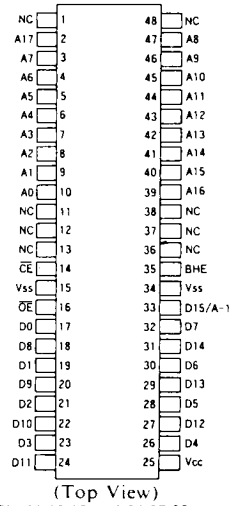
(Top View)

AKN62414FP, AKN62434FP



(Top View)

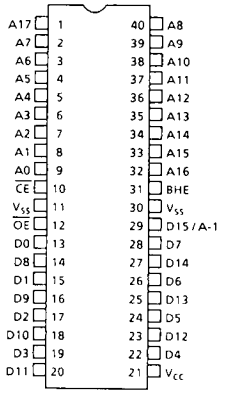
AKN62414F, AKN62434F



(Top View)

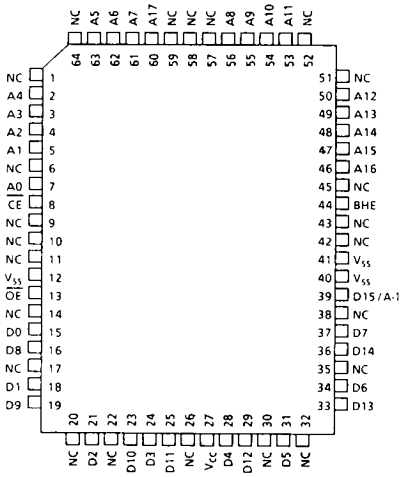
Pin 11-12-13 and 36-37-38 are connected each other internally.

AKN62414FA, AKN62434FA



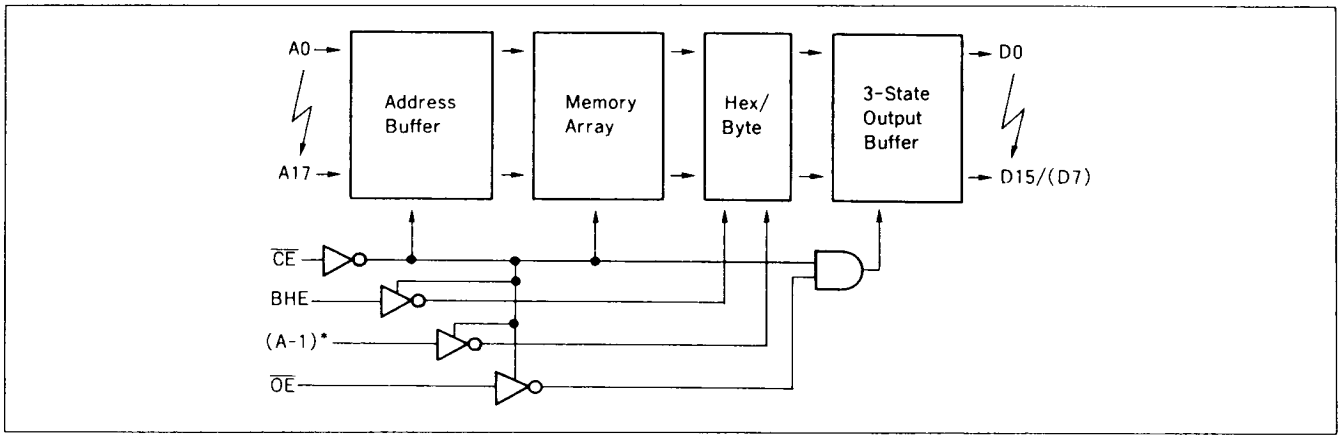
(Top view)

AKN62414FS, AKN62434FS



(Top view)

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, when BHE is low. (In this mode, D14-D8 pins are of high impedance.)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to Vcc + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to Vss.

Recommended Operating Conditions (Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	Vcc + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	Icc	—	50	mA	Vcc = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	Vcc = 5.5 V, $\overline{CE}$ ≥ Vcc – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to Vcc
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to Vcc
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (VCC = 5 V ± 10%, VSS = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (VCC = 5 V ± 10%, VSS = 0 V, Ta = 0 to +70°C)

Test Conditions

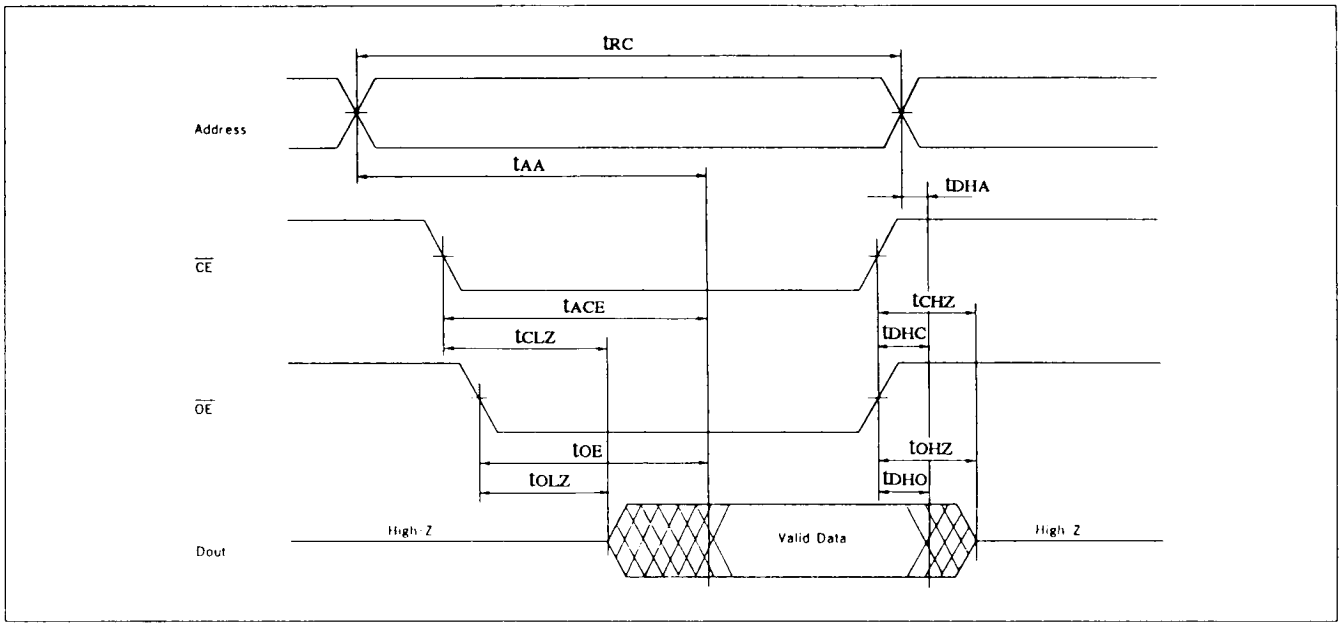
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	AKN62434		AKN62414-17		AKN62414-20		Unit
		Min	Max	Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	170		200	—	ns
Address access time	t_{AA}	—	150	—	170	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	170	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	70	—	100	ns
BHE access time	t_{BHE}	—	150	—	170	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	0	—	ns
Output Hold Time from BHE	t_{DHB}	0	—	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	10	—	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

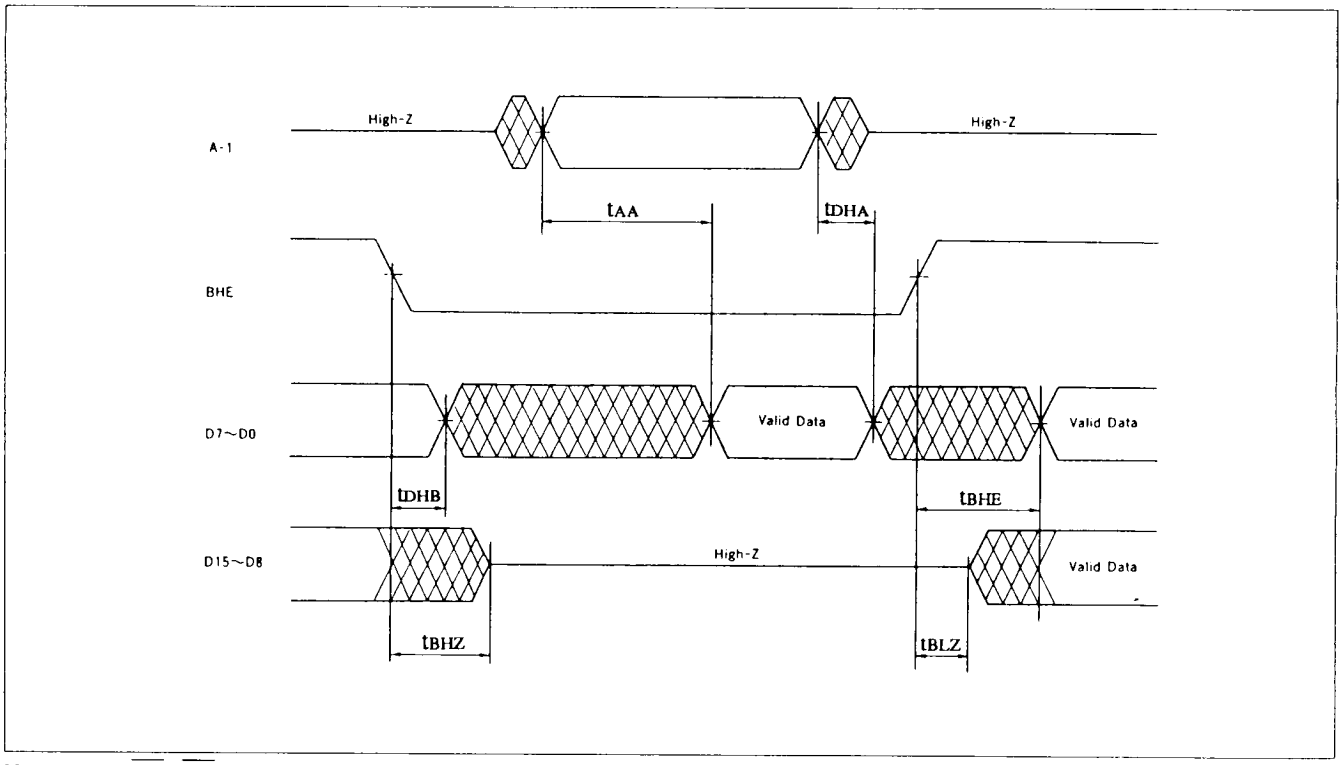
Timing Waveform

Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A17-A0 are valid.
2. D15/A-1 pin becomes output when BHE = V_{IH} and CE and OE are enabled. In this mode, an input signal should not be applied to this pin.