10-MEMORY TONE/PULSE DIALER WITH REDIAL FUNCTION

GENERAL DESCRIPTION

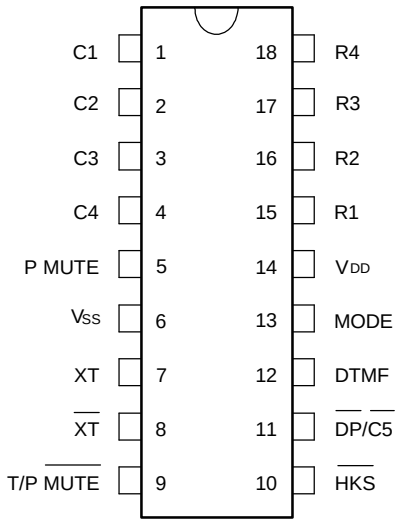
The W91630 series are Si-gate CMOS ICs that provide the signals needed for either pulse or tone dialing. The W91630 series features a ten-channel, 32-digit automatic dialing memory.

FEATURES

- DTMF/Pulse switchable dialer
- 32-digit redial memory
- Ten by 32 digit two-touch indirect repertory memory
- Mixed dialing, cascade dialing allowed
- Pulse-to-tone (P→T) keypad for long distance call operation
- Easy operation with redial, flash, pause and P→T keypads
- Pause, pulse-to-tone (P→T) can be stored as a digit in memory
- Tone output duration: as long as key is depressed or 90 mS minimum
- Minimum intertone pause: 90 mS
- Flash time: 100/300 mS
- Uses 4 × 5 keyboard
- On-chip power-on reset
- Uses 3.579545 MHz crystal or ceramic resonator
- Packaged in 18-pin DIP
- The different dialers in the W91630 series are shown in the following table:

TYPE NO.	DIALING RATE	PAUSE	M/B	FLASH
W91630	10 ppS	4 sec	1:2	300 mS
W91631			2:3	
W91632	10 ppS	4 sec	1:2	100 mS
W91633			2:3	

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NO.	I/O	FUNCTION
Column-Row Inputs	1–4 & 15–18	I	Keyboard inputs are designed for use with either a standard 4 × 5 keyboard or an inexpensive single contact (Form A) keyboard. Electronic input from a μC can also be used. Valid key entry is defined by a connection between a single row and a single column.
XT, $\overline{XT}$	7, 8	I, O	A built-in inverter provides oscillation with an inexpensive 3.579545 MHz crystal or ceramic resonator.
T/P $\overline{MUTE}$	9	O	The T/P $\overline{MUTE}$ is a conventional CMOS inverter output. It is low during pulse and tone mode dialing sequence and flash break; otherwise, it remains high.
MODE	13	I	Pulling the mode pin to VSS place the dialer in tone mode. Pull to VDD or leave floating: Pulse mode (10 ppS, M/B = 2:3 or 1:2)

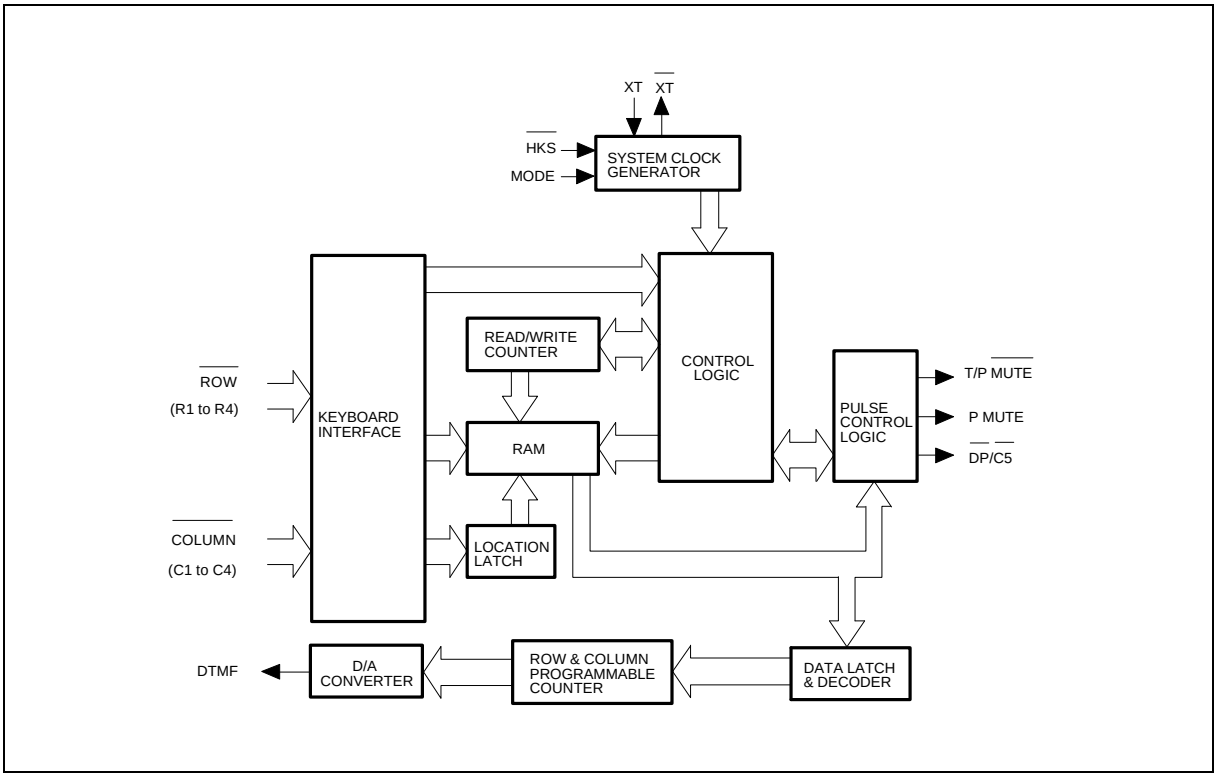
Pin Description, continued

SYMBOL	PIN NO.	I/O	FUNCTION
$\overline{HKS}$	10	I	Hook switch input. Conventional CMOS input with an internal protection diode and a pull-high resistor to V_{DD}. $\overline{HKS}$ = V_{DD}: On-hook state. Chip in sleep mode, no operation. $\overline{HKS}$ = V_{SS}: Off-hook state. Chip enabled for normal operation. During dialing, this input ignores $\overline{HKS}$ = V_{DD} for durations of less than 150 mS (i.e., dialing is not terminated).
$\overline{DP}/\overline{C5}$	11	O	Open drain dialing pulse output (Figure 1). Flash key causes $\overline{DP}/\overline{C5}$ to be active in both tone mode and pulse mode.
DTMF	12	O	During pulse dialing, maintains low state at all times. In tone mode, outputs a dual or single tone. Detailed timing diagram for tone mode is shown in Figure 2(a, b).
V_{DD}, V_{SS}	14, 6	I	Power input pins.
P MUTE	5	O	The P MUTE is a conventional CMOS inverter output. It is high during pulse dialing sequence and flash break. Otherwise, it remains low.

OUTPUT FREQUENCY

	Specified	Actual	Error %
R1	697	699	+0.28
R2	770	766	-0.52
R3	852	848	-0.47
R4	941	948	+0.74
C1	1209	1216	+0.57
C2	1336	1332	-0.30
C3	1477	1472	-0.34

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Keyboard Operation

C1	C2	C3	C4	$\overline{DP}$ / $\overline{C5}$	
1	2	3	S	P→T	R1
4	5	6	F	P	R2
7	8	9	A		R3
*	0	#	R		R4

- S: Store function key
- F: Flash key
- P→T: In pulse mode, this key works as Pulse→Tone key
- R: The redial function can be excuted only as first key-in after off-hook.
- A: Indirect repertory dialing key
- P: Pause key

Normal Dialing

OFF HOOK , D1 , D2 , ..., Dn

1. D1, D2, ..., Dn will be dialed out.
2. Dialing length is unlimited, but redial is inhibited if length oversteps 32 digits in normal dialing.
3. Dialing mode is determined at the on/off hook transition.

Redialing

1. OFF HOOK , D1 , D2 , ..., Dn , Busy, Come ON HOOK , OFF HOOK , R

The R key executes the redialing function.

2. Redial content = D1, D2, ..., Dn

OFF HOOK , R , D1' , D2' , P→T , D3' , D4'

a. D1, D2, ..., Dn, D1', D2', P→T, D3', D4' will be dialed out.

b. Redial register is changed to D1, D2, ..., Dn, D1', D2'.

3. Ln content = D1, D2, P→T, D3, D4

OFF HOOK , A , Ln , will dial out D1, D2, P→T, D3, D4

then ON HOOK , OFF HOOK , R will dial out D1, D2, P→T, D3, D4.

4. OFF HOOK , A , Lm , A , Ln , A , Lp

Busy, then ON HOOK , OFF HOOK , R

a. The digits stored in Lm, Ln, and Lp will be dialed out after the R key is pressed.

b. If length oversteps 32 digits, redial is inhibited.

c. Redial register stores not only normal dialing digits but also repertory or mixed dialed numbers.

d. Redialing is valid for first key-in only.

Number Store

1. OFF HOOK , S , D1 , D2 , ..., Dn , A , Ln , ON HOOK

a. D1, D2, ..., Dn will be stored in memory location Ln but will not be dialed out.

b. Ln = 0 to 9; Dn = 0 to 9, *, #, Pause, P→T.

c. The store mode is released to the initial state only when all store operations are finished.

There is no need to perform [ON HOOK] , [OFF HOOK] to begin a second store operation.

For example [S] , [D1] , [D2] , [D3] , [D4] , [A] , [Ln] ,

then [S] , [D1'] , [D2'] , [D3'] , [D4'] , [A] , [Lp] ,

then [S] , ..., is still available.

But the following sequence is not valid:

[S] , [D1] , [D2] , [D3] , [D4] , [A] , [Ln] ,

then [S] , [R] , [A] , [Ln]

2. [OFF HOOK] , [S] , [R] , [A] , [Ln] , [ON HOOK]

a. Redial content is transferred to memory Ln.

b. When the last number was dialed from redial memory, the content of the redial memory cannot be transferred to a memory location. For example, if the redial content is 1 2 3 4 5 + A 3, it cannot be transferred to a memory location, and the content of Ln will not be modified.

Memory Clear

[OFF HOOK] , [S] , [A] , [Ln] , [S] , [A] , [Lp] , ...

The Ln, Lp, etc., memories will be cleared.

Repertory Dialing

[OFF HOOK] , [A] , [Ln]

1. The digits stored in Ln will be dialed out.

2. The type of output signal is determined by the mode switch.

3. The redial register content is the content of location number Ln.

4. If the content of Ln is 1, 2, 3, P→T, 4, 5, 6, the redial function will execute the Pi÷T function and the system will change to tone mode.

Access Pause

[OFF HOOK] , [D1] , [D2] , [P] , [D3] , ..., [Dn]

1. The pause function can be stored in memory.

2. The pause function may be executed in normal dialing, redialing, or memory dialing (4.0 sec/pause).

3. The pause function can be stored as the first digit in memory.

4. The pause time depends on the number of times the P key is depressed. For example, if the sequence 1, 2, P, P, 4, 5, 6 is keyed in, then the pause time is 8 seconds.

5. The pause function timing diagram is shown in Figure 3.

Pulse-to-tone (P→T)

1. [OFF HOOK] , [D1] , [D2] , ..., [Dn] , [P→T] , [D1'] , [D2'] , ..., [Dn']

   a. If the mode switch is set to pulse mode, then the output signal will be as follows:

   D1, D2, ..., Dn, no pause, D1', D2', ..., Dn'

   (Pulse) (Tone)

In this case, the device can be reset to pulse mode only by going on-hook, because tone mode remains enabled after the digits have been dialed out.

   b. If the mode switch is set to tone mode, then the output signal will be as follows:

   D1, D2, ..., Dn, no pause, D1', D2', ..., Dn'

   (Tone) (Tone)

   c. The P→T key may be pressed before the first sequence is dialed out completely.

2. [OFF HOOK] , [R]

   If the mode switch is set to pulse mode, then the output signal will be as follows:

   D1, D2, ..., Dn, no pause, D1', D2', ..., Dn'

   (Pulse) (Tone)

3. [OFF HOOK] , [A] , [Ln]

   a. The P→T key can be stored in memory as a digit. The digits after the P→T key are also sent in repertory dialing.

   b. The P→T key does not stop dialing (no pause).

   c. The number stored in memory location Ln will be transferred to the redial register.

   d. The P→T function timing diagram is shown in Figure 4.

Flash

[OFF HOOK] , [D1] , [D2] , [D3] , [F] , [D4] , [D5] , [D6]

1. The [F] key may be pressed before digits D1, D2, D3 are sent completely. Digits D4, D5, D6 may be pressed during the 100/300 mS. flash period.
2. The flash key cannot be stored as a digit in memory or in the redial register.
3. [OFF HOOK] , [S] , [D1] , [D2] , [D3] , [F] , [D4] , [D5] , [D6] , [A] , [Ln] then [ON HOOK] , [OFF HOOK] , [A] , [Ln]

   D1, D2, D3, D4, D5, D6 will be dialed out.

4. The flash does not have first priority among the keyboard functions.
5. The flash pause time is 800 mS, so there is a pause of 800 mS between the flash and the next digit dialed (see Figure 5).
6. The dialer will not return to the initial state after the flash break time has elapsed.

7. The flash function timing diagram is shown in Figure 5.

Cascaded & Mixed Dialing

Cascaded Dialing

1. Definition of cascaded dialing:

   The next sequence may be pressed before the previous sequence is sent out completely.

   Examples of cascaded dialing.

   Example 1: [Normal dialing] ¡Ï [Repertory dialing 1] ¡Ï [Repertory dialing 2] ¡Ï...

   Example 2: [Repertory dialing 1] ¡Ï [Normal dialing] ¡Ï [Repertory dialing 2] ¡Ï...

   Example 3: [Redialing] ¡Ï [Normal dialing] ¡Ï [Repertory dialing] ¡Ï...

2. The rectangles above represent one sequence of normal dialing, redialing, or repertory dialing.
3. At most 64 digits are allowed in cascaded dialing. There is no limitation on the number of sequences.
4. The content of cascaded dialing may include a combination of normal dialing, redialing, and repertory dialing. Redialing is valid only as the first key-in, however.
5. [ON HOOK] , [OFF HOOK] , [R] : The cascaded dialing sequences described in the above examples will be dialed out only if they do not exceed a total of 32 digits. If the length of the combined sequences oversteps 32 digits then redialing is inhibited.

Mixed Dialing

1. Definition of mixed dialing:

   Mixed dialing is a combination of sequences of normal dialing, repertory dialing, and redialing. The three examples given for cascaded dialing are also examples of mixed dialing, provided each sequence is dialed out completely before the next sequence is entered.

2. There is no limitation on the number of digits and sequences in mixed dialing.
3. If a mixed dialing sequence includes redialing, the redialing is valid only as the first key-in.
4. [ON HOOK] , [OFF HOOK] , [R] : The mixed dialing sequences described in the above examples will be dialed out only if the total number of digits does not exceed 32. If the total oversteps 32 digits, then redialing is inhibited.

Combination of Cascaded and Mixed Dialing

1. Cascaded dialing and mixed dialing can be combined; each follows the rules described above.
2. To apply redialing to combinations of cascaded and mixed dialing:

   [ON HOOK] , [OFF HOOK] , [R] : Redialing will be executed only if the total number of digits

   does not exceed 32. If the total oversteps 32 digits, then redialing is inhibited.

3. If n cascaded sequences with a total of 60 digits have been dialed, then for the (n+1)th cascaded sequence, either one 4-digit normal dialing sequence or one complete repertory dialing sequence (length up to 32 digits) may be dialed. The (n+2)th sequence is not accepted for cascaded dialing.

4. After a total of 64 digits of cascaded dialing, mixed dialing can be added.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}–V_{SS}	-0.3 to +7.0	V
Input/Output Voltage	V_{IL}	V_{SS} -0.3	V
	V_{IH}	V_{DD} +0.3	V
	V_{OL}	V_{SS} -0.3	V
	V_{OH}	V_{DD} +0.3	V
Power Dissipation	P_D	120	mW
Operating Temperature	T_{OPR}	-20 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

($F_{OSC.}$ = 3.58 MHz, Ta = 25° C, all outputs unloaded)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	-	2.0	-	5.5	V
Operating Current	I_{OP}	Tone, V_{DD} = 2.5V	-	0.30	0.50	mA
		Pulse, V_{DD} =2.5V	-	0.15	0.30	
Standby Current	I_{SB}	$\overline{HKS}$ = 0, No load & No key entry	-	-	15	µA
Memory Retention Current	I_{MR}	$\overline{HKS}$ = 1, V_{DD} = 1.0V	-	-	0.2	µA
DTMF Output Voltage	V_{TO}	Row group, R_L = 5 KΩ	130	150	170	mVrms
Pre-emphasis		Col/Row, V_{DD} = 2.0 to 5.5V	1	2	3	dB
DTMF Distortion	THD	R_L = 5 KΩ V_{DD} = 2.0 to 5.5V	-	-30	-23	dB
DTMF Output DC Level	V_{TDC}	R_L = 5 KΩ V_{DD} = 2.0 to 5.5V	1.0	-	3.0	V

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF Output Sink Current	I_{TL}	V_{TO} = 0.5V V_{DD} = 2.5V	0.2	-	-	mA
$\overline{DP}$/$\overline{C5}$ Output Sink Current	I_{PL}	V_{PO} = 0.5V V_{DD} = 2.5V	0.5	-	-	mA
P MUTE & T/P $\overline{MUTE}$ Output Drive Current	I_{MH}	V_{MO} = 2.0V V_{DD} = 2.5V	0.2	-	-	mA
P MUTE & T/P $\overline{MUTE}$ Output Sink Current	I_{ML}	V_{MO} = 0.5V V_{DD} = 2.5V	0.5	-	-	mA
Keypad Input Drive Current	I_{KD}	V_I = 0V, V_{DD} = 2.5V	4	-	-	µA
Keypad Input Sink Current	I_{KS}	V_I = 2.5V, V_{DD} = 2.5V	200	400	-	µA
Keypad Resistance	R_K	-	-	-	5.0	KΩ
$\overline{HKS}$ Input Pull High Resistance	R_{HK}	-	-	300	-	KΩ
Input Voltage Low Level	V_{IL}	Pins 1, 2, 3, 4, 10, 13, 15, 16, 17, 18	0	-	0.2 V_{DD}	V
Input Voltage High Level	V_{IH}		0.8 V_{DD}	-	V_{DD}	V

AC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Keypad Active in Debounce	T_{KID}	-	-	20	-	mS
Key Release Debounce	T_{KRD}	-	-	20	-	mS
Pre-digit Pause	T_{PDP1}	Mode Pin = Floating	-	33.3	-	mS
	10 ppS	Mode Pin = V_{DD}	-	40	-	
Interdigit Pause (Auto Dialing)	T_{IDP}	10 ppS	-	800	-	mS
Make/Break Ratio	M/B	M/B = 1:2	-	33:67	-	%
		M/B = 2:3	-	40:60	-	
DTMF Output Duration	T_{TD}	Auto Dialing	-	90	-	mS
Intertone Pause	T_{ITP}		-	90	-	mS
Flash Break Time	T_{FB}	W91630/1	-	300	-	mS
		W91632/3	-	100	-	
Flash Pause	T_{FP}	-	-	800	-	mS
Pause Time	T_P	-	-	4.0	-	S
Pre-tone Mute	T_{PTM}	-	-	70	-	mS

Notes:
1. Crystal parameters suggested for proper operation are R_S < 100 Ω, Lm = 96 mH, Cm = 0.02 pF, Cn = 5 pF, Cl = 18 pF, $F_{OSC.}$ = 3.579545 MHz ±0.02%.

2. Crystal oscillator accuracy directly affects these times.

TIMING WAVEFORMS

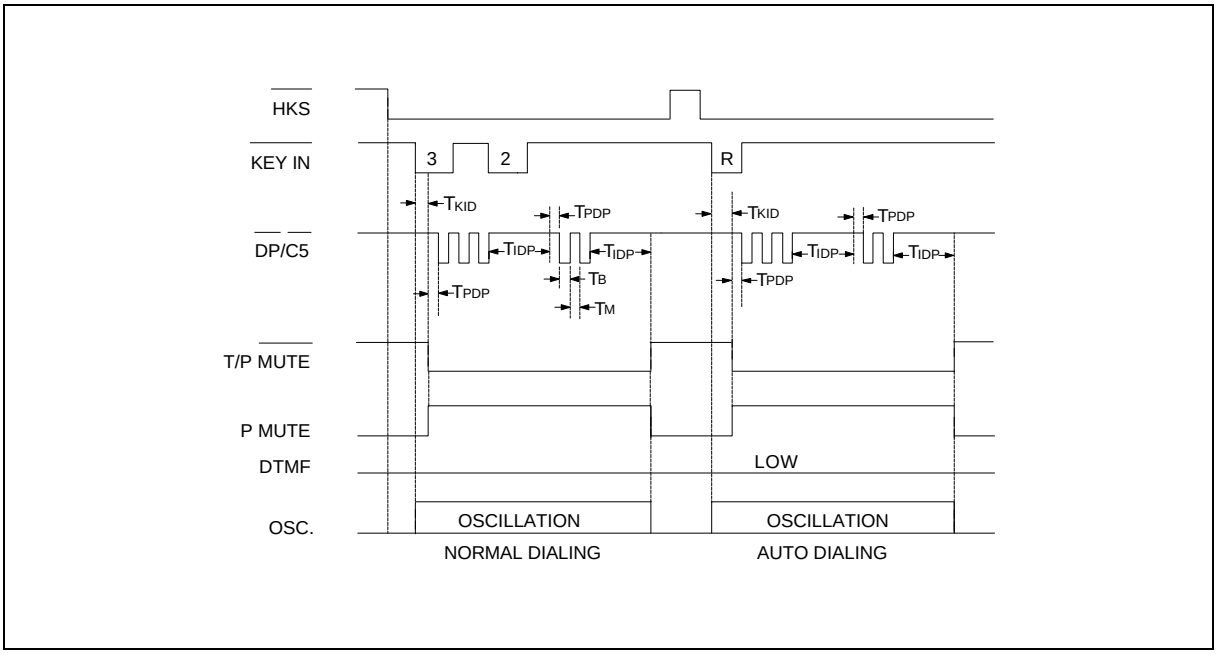


Figure 1. Pulse Mode Timing Diagram

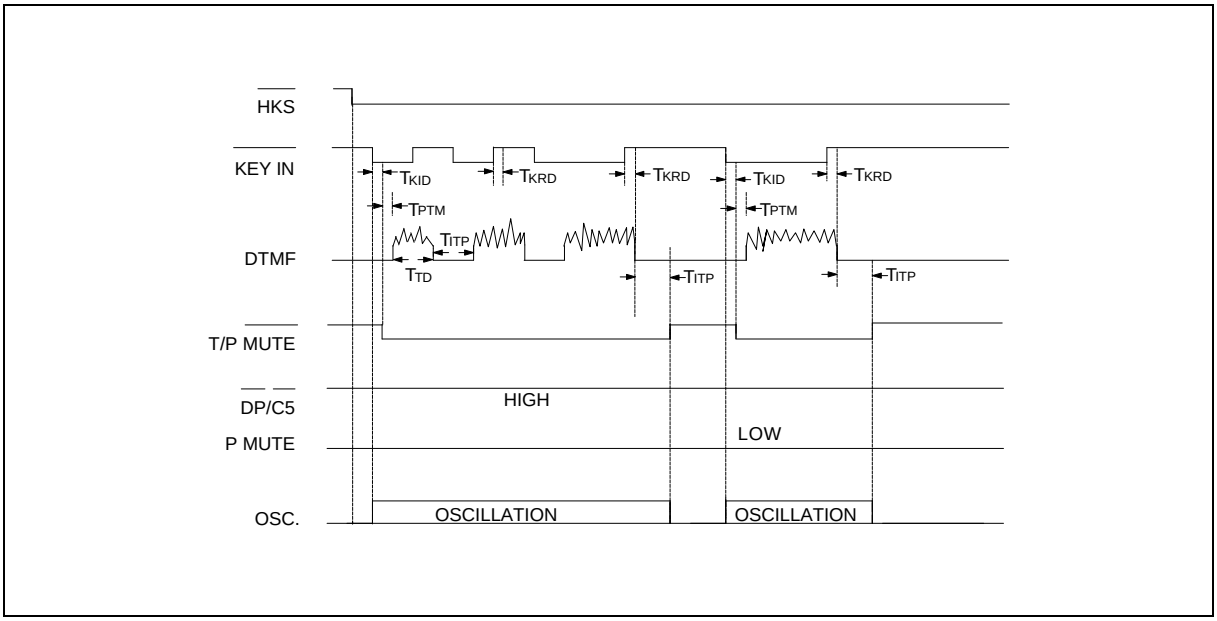


Figure 2(a). Tone Mode Normal Dialing Timing Diagram

Timing Waveforms, continued

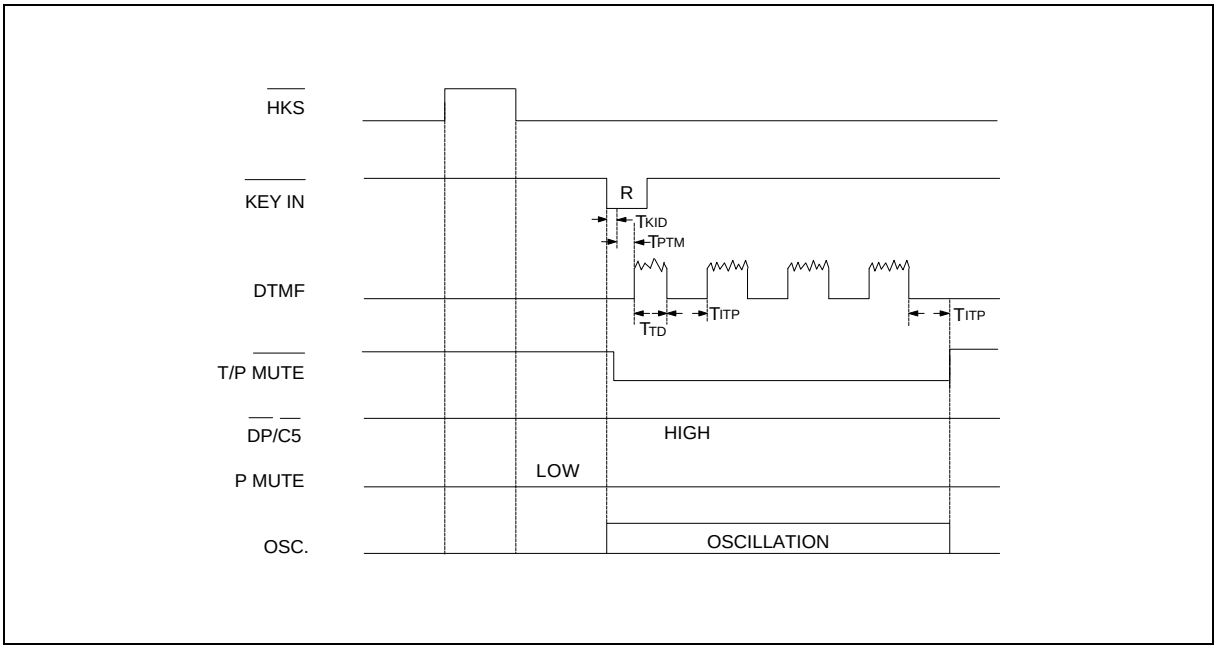


Figure 2(b). Tone Mode Auto Dialing Timing Diagram

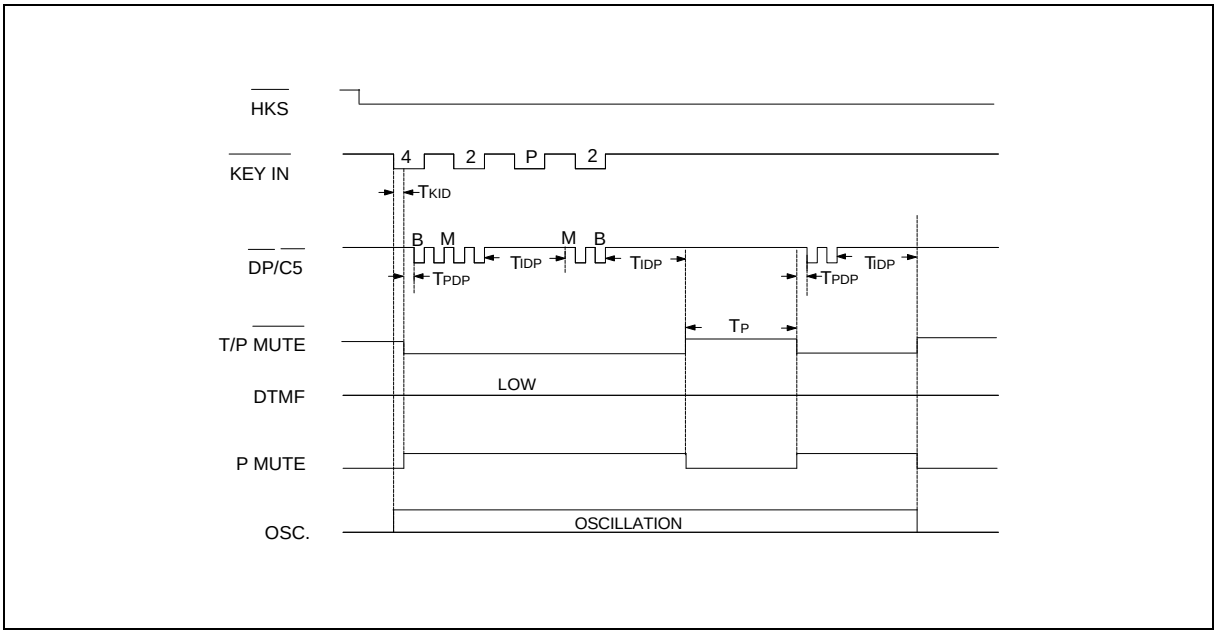


Figure 3. Pause Function Timing Diagram

Timing Waveforms, continued

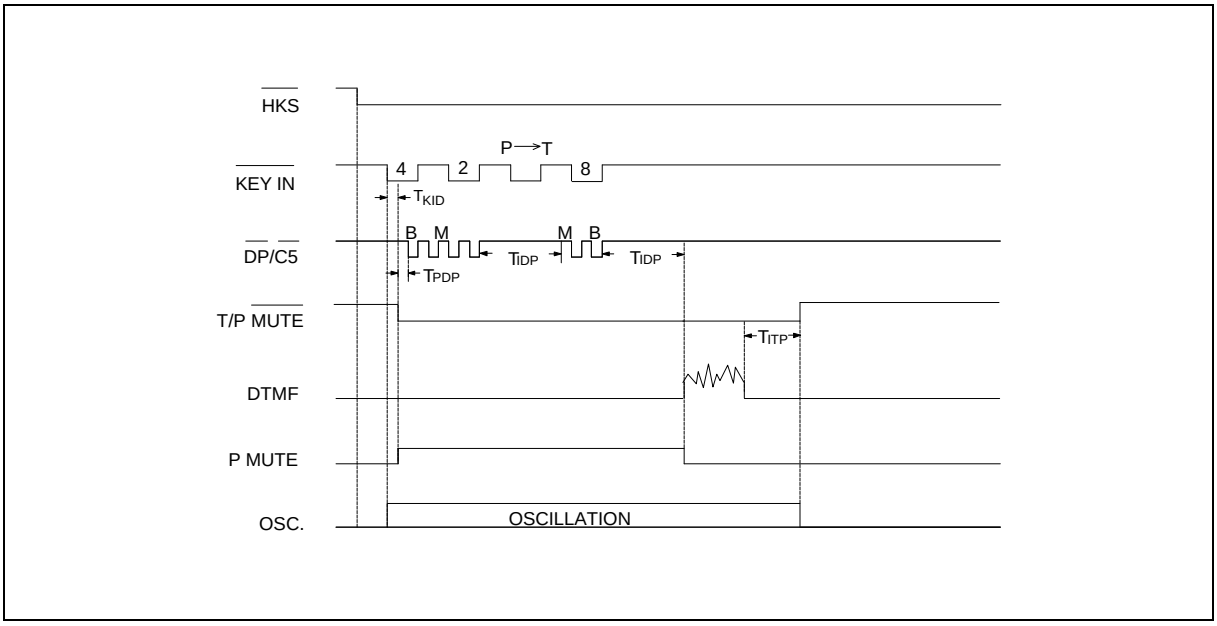


Figure 4. P→T Operation Timing Diagram in Normal Dialing

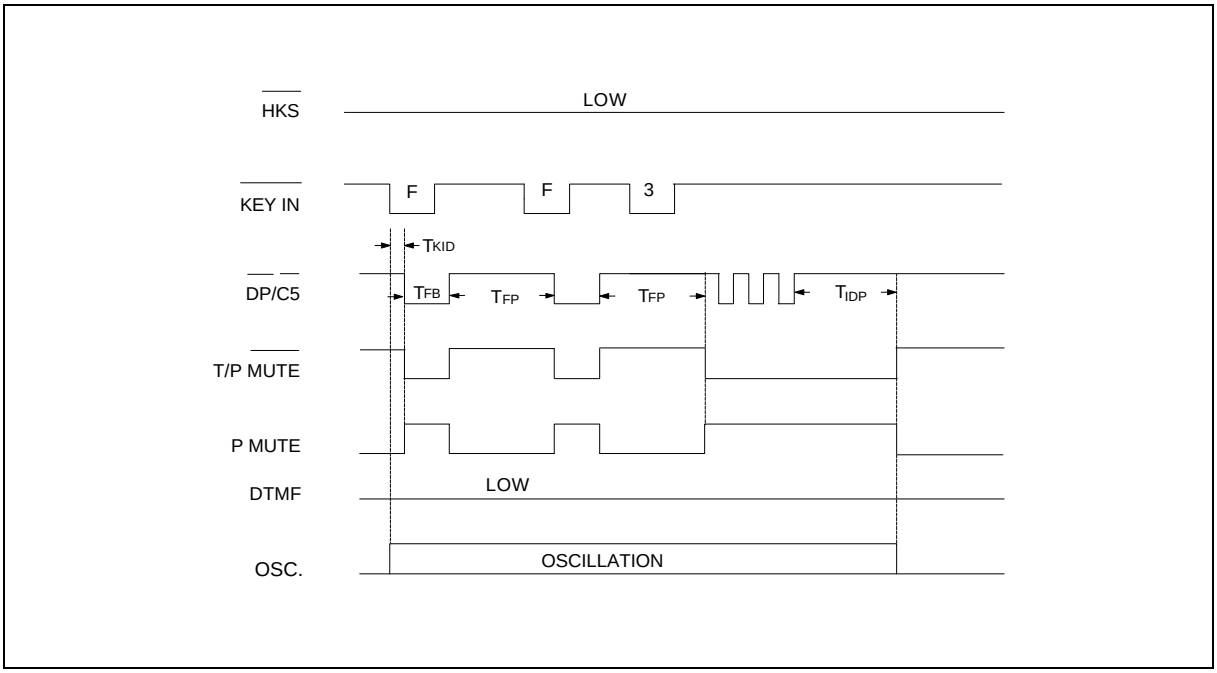


Figure 5. Flash Operation Timing Diagram

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