PRELIMINARY

Am79C410

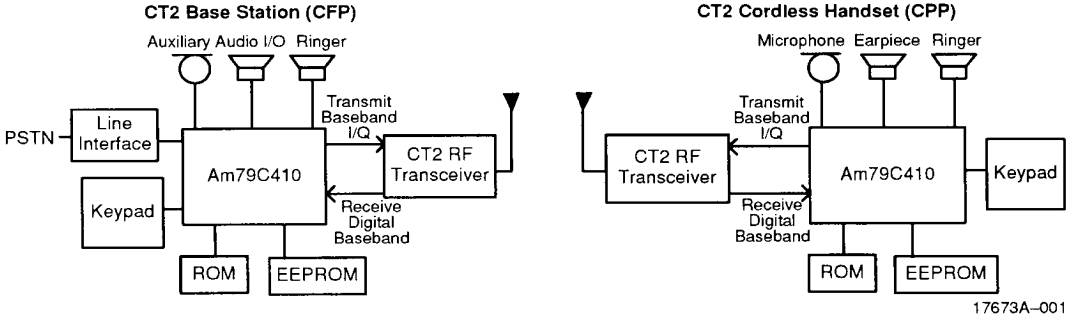
CT2 PhoX™ Controller for Digital Cordless Telephones

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Performs all protocol, data formatting, audio processing, and peripheral functions for CAI CT2 (Common Air Interface, Cordless Telephone, 2nd generation) digital cordless telephones.**
- **May be used in the base station and the handset.**
- **High integration and low power consumption allow compact handsets and extended battery life.**
- **On-chip 8051-class microcontroller controls all functions.**
- **Special CAI CT2 features**
  - — Link controller which performs all data transmission and reception
  - — Baseband I/Q GMSK modulator which conforms to CAI CT2 transmission spectrum requirements
  - — Receive signal strength indicator for channel scanning
- **Special audio features**
  - — ADPCM codec compliant with CCITT G.721
  - — Programmable noise suppression
  - — DTMF generator and ringing tone generator
  - — Flexible audio interface with 16-ohm speaker drive
- **Other on-chip peripheral functions**
  - — 1-Kbyte battery-backed static RAM
  - — Battery-backed Real Time Clock for time keeping and alarm generation
  - — Serial port for EEPROM, LCD, and/or synthesizer
  - — 36-key scanner for dialing and special function keys
  - — Up to ten general-purpose output ports
  - — Watchdog timer
- **Built-in power management features**
  - — Single 3-V supply (5 V also available)
  - — Low active power consumption, 80 mW typ
  - — Super low power shutdown mode, 900 µW typ
  - — Battery level detection
  - — Line-powered emergency dialing mode
- **Test and development features**
  - — In-circuit 8051 emulator support for code development
  - — Numerous test paths and loopbacks for bit error rate, continuity, and performance testing
  - — Continuous transmit RF spectral measurement and modulator bypass features
- **100-pin PQFP package**

SYSTEM ARCHITECTURE



17673A–001

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General Description

The competitive supplier of digital cordless handsets for residential or telepoint applications must offer the consumer compact size, light weight, and extended battery life. The Am79C410 CT2 PhoX controller meets these needs with an integrated baseband solution for the CAI CT2 digital cordless telephone standard described by ETSI document I-ETS 300 131. The Am79C410 incorporates all of the baseband functions required by CT2 telephones in a single chip, including audio processing, protocol control, data formatting, and peripheral functions such as serial port, a real time clock, and a keypad scanner. An architecture optimized for low power consumption is combined with special power management features to maximize battery life.

CT2 telephones use a time division duplex 32-kbit/s ADPCM (Adaptive Differential Pulse Code Modulation) voice (B) channel and a 1-, 2-, or 16-kbit/s control (D) channel between the handset and the base station. The physical implementation is a 72-kbit/s ping-pong type radio link with identical transmit and receive frequencies in the 860-MHz range. The Am79C410 formatter performs all the CT2 protocol requirements as well as baseband transmission and reception under control of the on-chip 8051-class microcontroller.

Baseband transmit data is filtered on-chip to provide analog Gaussian Minimum Shift Key (GMSK) output meeting CT2 spectral requirements. GMSK is a form of frequency shift keying modulation which minimizes bandwidth by conditioning the pulse shapes of the individual transmitted data bits.

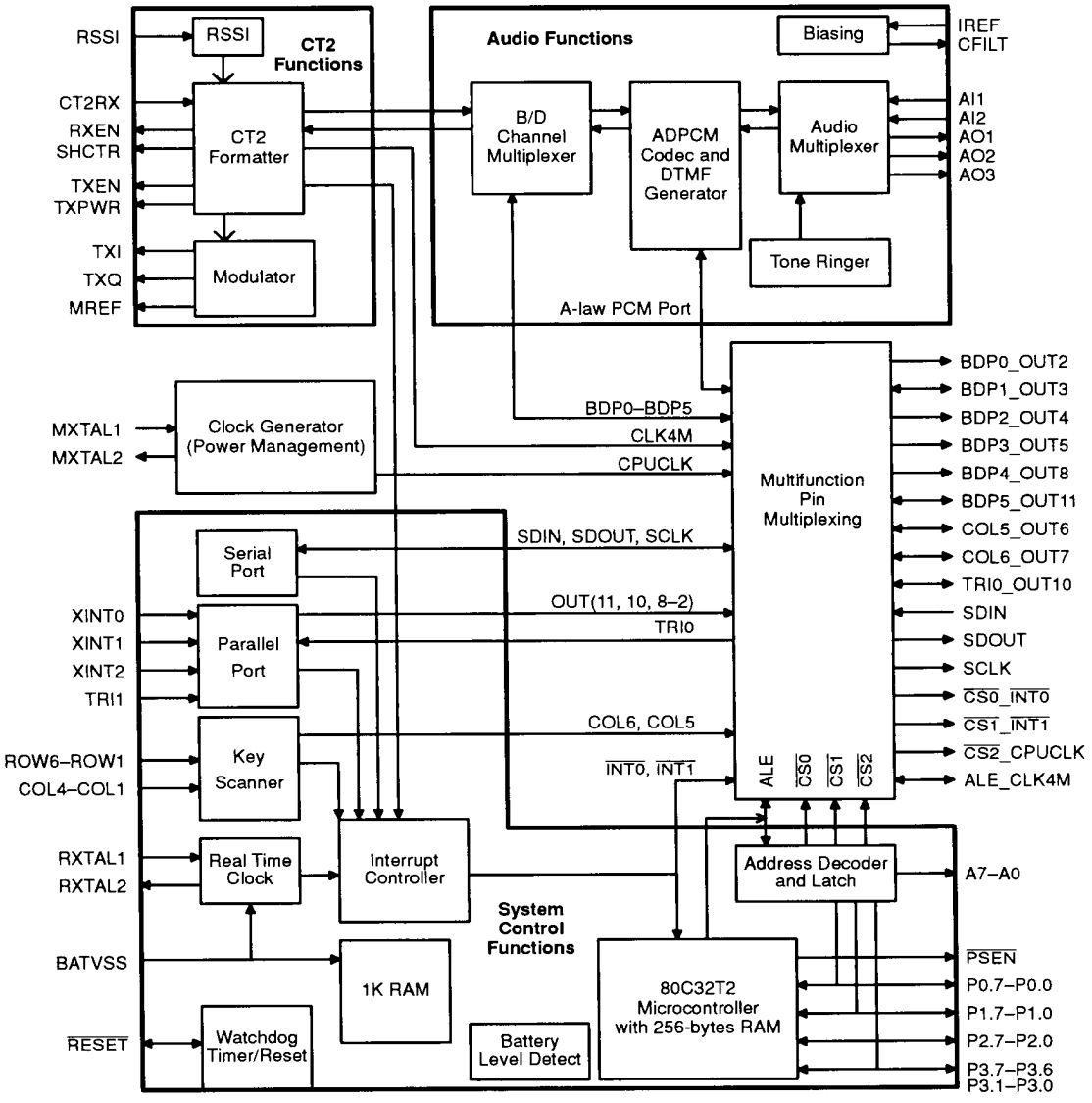
The CT2 voice (B) channel is a 32-kbit/s ADPCM stream. The Am79C410 converts analog voice input at the microphone interface to ADPCM format and converts ADPCM received data to analog output at the earpiece or loudspeaker output. The device also provides digitally generated DTMF and ringing tones.

The Am79C410 incorporates many peripheral functions necessary for digital cordless telephones. For example, it has a 36-key keypad scanner and a serial port for interfacing with an EEPROM or serial LCD. The chip includes a real time clock which may be battery-backed and a host of multifunction ports.

The heart of the device is the 80C32T2, an 8051-class microcontroller. The controller can perform CT2 Layer 3 and partial Layer 2 functions and drive the hardware which performs the partial Layer 2 and Layer 1 functions. It initializes the audio path and services the various on-chip peripherals. The on-chip 1-Kbyte static RAM is used for variable storage. For software development, the chip interfaces directly to standard 8051 in-circuit emulators in ICE mode.

The Am79C410 is designed for power management in a battery-operated environment. It has low power dissipation and operates over a 2.7- to 3.6-V supply (2.7 V to 5.25 V for the extended range device). The chip also includes a very low power shutdown mode. For battery support, there is a battery level measurement facility. The on-chip 1-Kbyte RAM and real time clock are battery backed through a separate battery back-up pin, allowing memory retention even when the main power supply is removed.

Block Diagram



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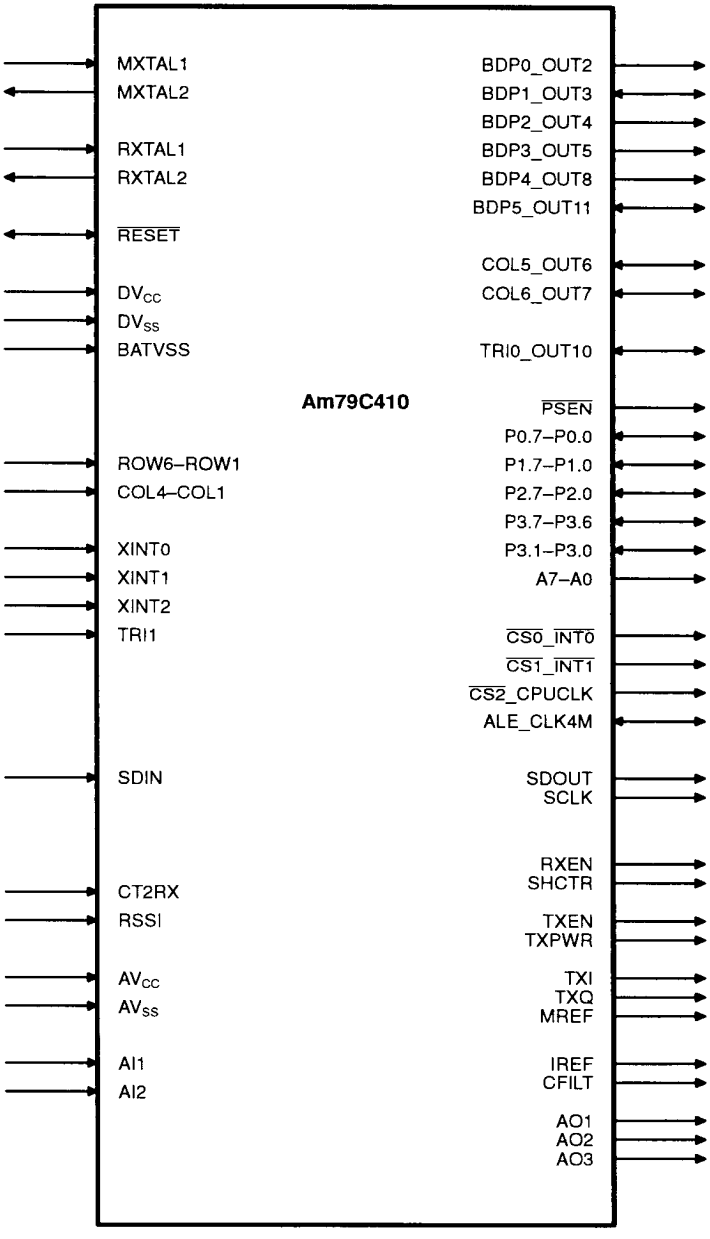
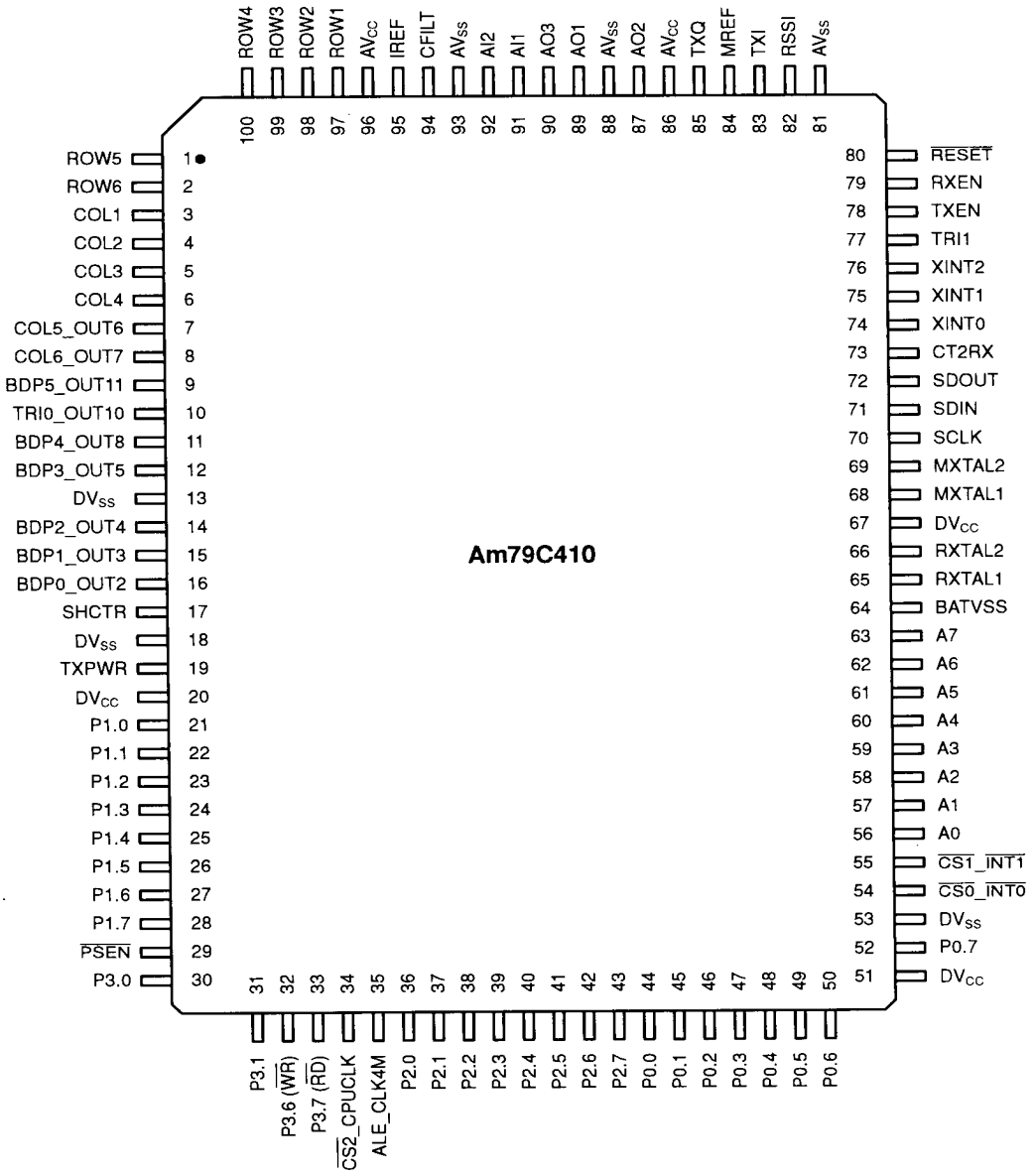
LOGIC DIAGRAM



Connection Diagram

Top View, Contacts Facing Down

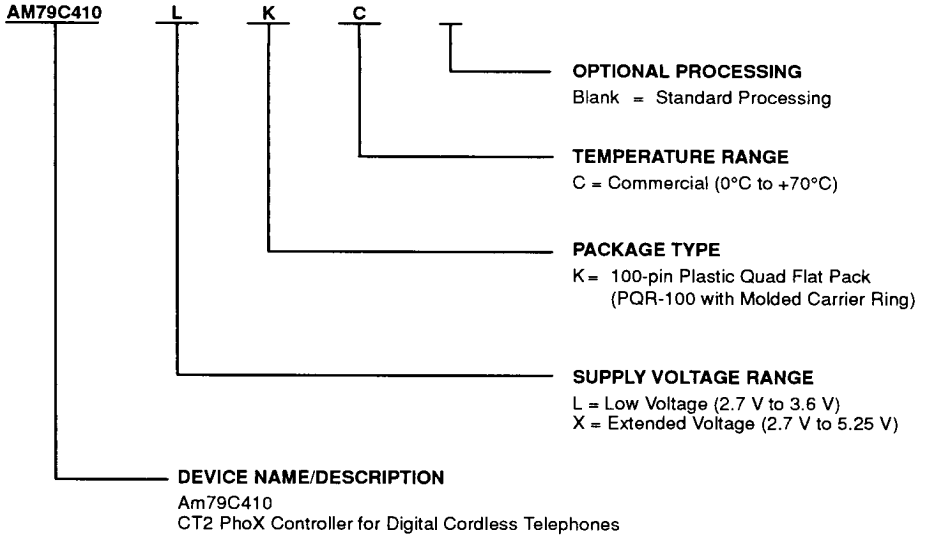


Note: *Pin One marked for orientation purposes only.*

Ordering Information

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C410	LKC
	XKC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Pin Descriptions

All signals are CMOS levels unless otherwise stated. A (♦) indicates multifunction pins whose characteristics depend on software configuration and which may be described in more than one table in this section.

CT2 Pins

Pin	Pin Name	I/O Type	Description
35	ALE_CLK4M♦	I/O	4.608-MHz 50% duty cycle clock output.
16	BDP0_OUT2♦	O	Digital B- or D-channel output or clock. In shutdown mode, the pin retains its value.
15	BDP1_OUT3♦	I/O	Digital B-channel input, D-channel I/O, B+D transmit data (CT2TXD signal) or modulator test data input. As an output in shutdown mode, the pin retains its value.
14	BDP2_OUT4♦	O	Digital B- or D-channel clock output. In shutdown mode, the pin retains its value. Also, the CT2TXEN pulse, active during transmission when properly configured.
12	BDP3_OUT5♦	O	Digital B- or D-channel clock output. In shutdown mode, the pin retains its value.
73	CT2RX	I	72-kHz digital receive data.
84	MREF	O	Modulator DC reference. 0.5 × V_{CC} ±5%. When disabled, the pin looks like a 25-kΩ resistance to analog ground.
82	RSSI	I	Receive signal strength indicator analog input. High impedance, DC coupled. For noise rejection, a small filter capacitor may be tied between RSSI and analog ground.
79	RXEN	O	Active High strobe indicating CT2 receive window for enabling receiver and IF and RF circuits.
17	SHCTR	O	Sample/hold control for maintaining receiver discriminator DC level between receive windows.
78	TXEN	O	Active High strobe indicating CT2 transmit window for enabling transmitter IF and RF circuits.
83	TXI	O	Modulator in-phase output. ±0.5-V peak, DC coupled, internally DC biased to MREF. When disabled, the pin looks like a 25-kΩ resistance to analog ground.
19	TXPWR	O	High power/low power transmitter mode control output.
85	TXQ	O	Modulator quadrature output. ±0.5-V peak, DC coupled, internally DC biased to MREF. When disabled, the pin looks like a 25-kΩ resistance to analog ground.

Audio Pins

Pin #	Pin Name	I/O Type	Description
91	AI1	I	Analog audio input. ±0.5-V peak, AC coupled, internally DC biased to $0.32 \times V_{CC}$. Rin > 10 kΩ. Typically used for PSTN input.
92	AI2	I	Analog audio input. ±0.354-V peak, AC coupled, internally DC biased to $0.32 \times V_{CC}$. Programmable gain applied internally. Rin > 10 kΩ. Typically used for microphone input.
89	AO1	O	Analog audio output. ±0.5-V peak, AC coupled, internally DC biased to $0.32 \times V_{CC}$. Maximum load: $R_{LOAD} \geq 1$ kΩ, $C_{LOAD} \leq 100$ pF. When disabled or in shutdown, output is high impedance. Typically used for PSTN output.
87	AO2	O	High current drive analog audio output. ±1.0-V peak, AC coupled, internally DC biased to $0.5 \times V_{CC}$. Programmable gain applied internally. Maximum load: $R_{LOAD} \geq 13$ Ω, $C_{LOAD} \leq 100$ pF. When disabled or in shutdown, output is high impedance. Typically used for loudspeaker driver.
90	AO3	O	Analog audio output. ±1.0-V peak, AC coupled, internally DC biased to $0.5 \times V_{CC}$. Programmable gain applied internally. Maximum load: $R_{LOAD} \geq 160$ Ω, $C_{LOAD} \leq 100$ pF. When disabled or in shutdown, output is high impedance. Typically used for earpiece speaker driver.
16	BDP0_OUT2♦	O	32-kbit/s ADPCM B-channel output. In shutdown mode, the pin retains its value.
15	BDP1_OUT3♦	I/O	32-kbit/s ADPCM B-channel input.
14	BDP2_OUT4♦	O	Digital B-channel frame clock output. In shutdown mode, the pin retains its value.
12	BDP3_OUT5♦	O	Digital B-channel bit clock output. In shutdown mode, the pin retains its value.
11	BDP4_OUT8♦	O	Digital B-channel encryption output. In shutdown mode, the pin retains its value.
9	BDP5_OUT11♦	O	Digital B-channel encryption output.
94	CFILT	O	$0.32 \times V_{CC}$ DC bias filter pin. Must be connected to 11 µF (10-µF electrolytic in parallel with 1-µF ceramic) tied to ground and located close to the IC to minimize noise. The pin is not disabled by shutdown or reset.
95	IREF	O	Current reference output, which must be tied to a temperature stable resistor connected to analog ground and located as close as possible to the IC to minimize noise. The resistor should be 61.9 kΩ with 1% tolerance, creating a ≈20-µA reference. The pin goes to high impedance in shutdown mode.
70	SCLK♦	O	A-law PCM clock output. It is pulled Low when the serial port is disabled or when the chip is in shutdown.
71	SDIN♦	I	A-law PCM data input.
72	SDOUT♦	O	A-law PCM data output. The pin is pulled Low when the serial port is disabled or when the chip is in shutdown.

Microcontroller and Address Decoder Pins

Pin #	Pin Name	I/O Type	Description
—	A7–A0	O	Lower-order address bytes, latched on ALE from the Port 0 bus.
35	ALE_CLK4M♦	I/O	This multifunction pin is configured by software and basic mode selection to be an ALE input, an ALE output, or a 4.608-MHz clock output associated with the CT2 functions. The ALE signal is the 80C32T2 address latch enable for latching the lower-order address on the Port 0 bus during external accesses. In ICE mode, the pin is the ALE input for addressing on-chip memory and registers.
54	$\overline{CS0}$_$\overline{INT0}$♦	O	In normal mode $\overline{CS0}$_$\overline{INT0}$ drives the $\overline{CS0}$ output, an active Low address space decode. In ICE mode it drives the $\overline{INT0}$ signal, which is ordinarily connected to the 8051 emulator $\overline{INT0}$ input.
55	$\overline{CS1}$_$\overline{INT1}$♦	O	In normal mode $\overline{CS1}$_$\overline{INT1}$ drives the $\overline{CS1}$ output, an active Low address space decode. In ICE mode it drives the $\overline{INT1}$ signal, which is ordinarily connected to the 8051 emulator $\overline{INT1}$ input.
34	$\overline{CS2}$_CPUCLK♦	O	This multifunction pin is configured by software and ICE mode selection to be either the $\overline{CS2}$ address space decode output or the 80C32T2 clock output.
—	P0.7–P0.0	I/O	Port 0 is the multiplexed data and lower-order address bus for external data and program memory access, using strong internal pull-ups when driving 1s. P0.7–P0.0 are held weakly High during reset. In shutdown mode, they are held strongly Low or weakly High, depending on the last operation performed on them. They are high impedance in ICE mode.
—	P1.7–P1.0	I/O	Port 1 is an 8-bit I/O port with internal pull-ups. Port 1 pins written to 1s are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins externally pulled Low source current because of the pull-ups. All Port 1 pins may be programmed to generate interrupts in response to changes of state. P1.7–P1.0 are held weakly High during reset and retain their programmed values in shutdown mode. They are high impedance in ICE mode. The pull-up associated with each pin can be individually disabled.
—	P2.7–P2.0	I/O	Port 2 is the upper-order address byte during fetches from program memory and during access to external data memory that use the MOVX@DPTR instruction. In this application, it uses strong pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), Port 2 emits the contents of the Port 2 special function register. P2.7–P2.0 are held weakly High during reset and in shutdown mode and are high impedance in ICE mode. The pull-up associated with each pin can be individually disabled.
—	P3.1–P3.0	I/O	Port 3.1–3.0 pins are I/O ports with internal pull-ups. When written to 1s they are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins externally pulled Low source current because of the pull-ups. The pull-up associated with each pin can be individually disabled. The pins also serve the functions of the special features listed below. **Port Pin** — **Alternate Function** P3.0 — RxD (serial input port) P3.1 — TxD (serial output port)
32	P3.6	I/O	The P3.6 pin is the $\overline{WR}$ signal, which is the active Low external data memory write strobe. In normal mode, P3.6 is the $\overline{WR}$ output for external components. In ICE mode, it is the $\overline{WR}$ input for writing on-chip memory and registers.
33	P3.7	I/O	The P3.7 pin is the $\overline{RD}$ signal, which is the active Low external data memory read strobe. In normal mode, P3.7 is the $\overline{RD}$ output for external components. In ICE mode, it is the $\overline{RD}$ input for reading on-chip memory and registers.
29	$\overline{PSEN}$	O	$\overline{PSEN}$ is the active Low read strobe to external program memory. In shutdown $\overline{PSEN}$ is held weakly High. In ICE mode, the pin is high impedance.

Parallel Port Pins

Pin #	Pin Name	I/O Type	Description
16	BDP0_OUT2♦	O	General purpose outputs OUT11, OUT8–OUT2 are functions that share configurable multifunction pins. When programmed for the OUT function, the pin drives the level programmed in the associated GPOCTR0 or GPOCTR1 register and retain that value when the chip goes into shutdown mode. Outputs default to 1 at reset.
15	BDP1_OUT3♦	I/O	
14	BDP2_OUT4♦	O	
12	BDP3_OUT5♦	O	
7	COL5_OUT6♦	I/O	
8	COL6_OUT7♦	I/O	
11	BDP4_OUT8♦	O	
9	BDP5_OUT11♦	I/O	
10	TRI0_OUT10♦	I/O	TRI0_OUT10 is a multifunction pin configured to provide the TRI0 input or the OUT10 output. As TRI0, it is a software readable three-level input detecting V_{SS}, V_{CC}, and open (no connect). As OUT10, it is driven to the state programmed by software in the GPOCTR1 register.
77	TRI1	I	Three-level software readable input: V_{SS}, V_{CC}, and open (no connect). During reset, the state of TRI1 determines whether the chip is in ICE mode.
74	XINT0	I	External interrupt 0 generates an interrupt on a change of state.
75	XINT1	I	External interrupt 1 generates an interrupt on a change of state.
76	XINT2	I	External interrupt 2 generates an interrupt on a change of state.

Key Scanner and Serial Port Pins

Pin #	Pin Name	I/O Type	Description
—	COL4–COL1	I	Key scanner matrix column inputs. Each input has an internal weak pull-up. Small capacitors (≈ 0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity.
7 8	COL5_OUT6♦ COL6_OUT7♦	I/O	Key scan COL5 and COL6 inputs with weak pull-ups. Small capacitors (≈ 0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity.
—	ROW6–ROW1	I	Key scanner matrix row inputs. Each input has an internal weak pull-down. Small capacitors (≈ 0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity.
70	SCLK♦	O	Serial port clock output. It is pulled Low when the serial port is disabled or when the chip is in shutdown.
71	SDIN♦	I	Serial port data input.
72	SDOUT♦	O	Serial port data output. The pin is pulled Low when the serial port is disabled or when the chip is in shutdown.

Crystal, Reset, and Power Supply Pins

Pin #	Pin Name	I/O Type	Description
86 96	AV_{CC}	I	Analog power supply, which must be connected to the digital power supply. It is important to provide decoupling capacitors of ≈1 µF across the following pin combinations: decouple pin 86 to ground pin 81 (modulator and RSSI supply) decouple pin 86 to ground pin 88 (analog audio outputs supply) decouple pin 96 to ground pin 93 (analog inputs, audio mux, A/D, D/A, and battery detector supply)
81 88 93	AV_{SS}	O	Analog ground. Analog and digital grounds must be connected. Pin 81 is the reference for the CT2 modulator and RSSI functions. Pin 88 is the ground reference for audio outputs AO1, AO2, and AO3. Pin 93 is the reference for analog inputs AI1 and AI2.
64	BATVSS	O	Back-up battery ground. This pin should be tied to an external diode in series with the negative terminal of the back-up battery.
20 51 67	DV_{CC}	I	Digital power supply. Digital and analog supplies must be tied together. It is important to provide decoupling capacitors of ≈0.1 µF across the following pin combinations: decouple pin 20 to ground pin 18 decouple pin 51 to ground pin 53 decouple pin 67 to ground pin 13 decouple pin 67 to battery ground pin 64
13 18 53	DV_{SS}	O	Digital ground. Analog and digital grounds must be connected.
68	MXTAL1	I	18.432-MHz crystal input. A 2-Vpp digital clock, AC coupled through 30 pF, may be used.
69	MXTAL2	O	18.432-MHz crystal output. If a digital clock input is used, this pin should be pulled up to DV_{CC} through a 2.2-kΩ resistor.
80	$\overline{\text{RESET}}$	I/O	Active Low, open-drain reset input returns chip to default state. The pin must be externally pulled up. The watchdog timer function drives the pin Low when the timer expires. In ICE mode the pin is an input only.
65	RXTAL1	I	32.768-kHz real time clock crystal input, accepting either a parallel resonant AT cut crystal or a CMOS logic level clock.
66	RXTAL2	O	32.768-kHz real time clock crystal output. If the crystal input is driven by a CMOS logic level clock, RXTAL2 should be left unconnected.

Functional Description

Power Management

Power management is a central theme in the Am79C410 design. Using low power CMOS technology, the device operates over a 2.7-V to 3.6-V supply range (2.7 V to 5.25 V in extended range version) with very low power consumption, typically 16 mA at 3 V in active mode. Software controls entry into the very low power shutdown mode, drawing typically 300 µA at 3 V. In shutdown mode only the real time clock functions (all other synchronous circuits are held static for minimum power consumption).

The microcontroller clock rate is programmable to minimize power consumption. The clock rate control mechanism includes an automatic speed-up feature, which allows any interrupt to immediately increase the clock rate to maximum speed for fast interrupt service.

Each synchronous functional block is also individually enabled or disabled by programming the appropriate bit in one of two control registers. Disabled blocks are held static for low power consumption.

The main battery level can be checked in the BATLEV register, so that software may generate appropriate warnings to the user or initiate some low power mode when the main battery voltage is too low.

The chip provides a low power emergency dialing mode for use in a base station equipped with a wired handset, providing basic POTS services from telephone DC line power when AC power mains fail. The mode is defined as a collection of hardware configurations under software control.

System Control Functions

The microcontroller in the Am79C410 is a member of the 8051 Family of microcontrollers, with the standard 8051 Family architecture and instruction set. While it is substantially identical to the AMD 80C32T2 microcontroller, some enhancements have been made to meet the special needs of the CT2 environment. Despite these differences, the microcontroller is referred to throughout this document as an 80C32T2 or simply 8032.

The 8032 has separate internal and external data spaces, requiring different commands for read and write access. The Am79C410 provides on-chip RAM in both internal and external 8032 data spaces. The device has no on-board program ROM.

– ROM	none
– RAM (internal data space)	256 bytes
– RAM (external data space)	1024 bytes (battery-backed)

The frequency of the 8032 clock is programmable from 72 kHz to 9.216 MHz, realized by an internal programmable crystal clock divider. By programming the device for shutdown mode, the clock stops entirely.

The **address decoder** decodes the 8032 external data space chip-selects called $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$. A latch captures the 8032 lower order address from the Port 0 multiplexed data/address bus and presents the address on the A7–A0 pins, eliminating the transparent latch customarily used in an 8051 Family data memory interface.

The **Real Time Clock** (RTC) is a 100-year calendar that keeps track of years, months, days, hours, and seconds and provides periodic and alarm interrupts. The RTC is battery backed through the BATVSS pin and continues to operate even when main battery power is removed. The RTC continues to run when the Am79C410 is in shutdown mode and its alarm function allows the chip to awaken itself at any preset time of day.

The **key scanner** is an interrupt driven, asynchronous keypad detection mechanism requiring software debouncing. It supports a 6×6 keypad configuration. Special functions include multiple-key detection and nonmaskable any-key detection for system wake-up. The scanner inputs recognize a key depression as a switch closure between a row and a column pin. Row pins have weak pull-ups and column pins have weak pull-downs. When the switch closes, the level at the pins approaches mid-supply and is recognized as active at both the row and column inputs.

The **serial port** is a synchronous peripheral residing in 8032 external data space which provides a clean interface to popular serial EEPROMs and LCDs. Serial EEPROMs may be useful for storing telephone numbers, ID codes, or system initialization data.

The **parallel port** is a grouping of four independent functions: Port 1 interrupts, external interrupts, general purpose output latch, and three-level inputs. The Port 1 interrupt function recognizes events at the eight 8032 port pins and generates maskable interrupts in response. Three external interrupt inputs are provided on the XINT0, XINT1, and XINT2 pins. Any change of state on an XINT pin causes a maskable interrupt. The nine general-purpose outputs drive their respective pins to programmed values and are designed for high current drive. Finally, the two three-level inputs establish the basic operating mode of the chip or serve as general purpose inputs.

The **watchdog timer** generates a system reset if not refreshed by software at least once every 1.82 seconds. The circuit also performs software-driven resets.

CT2 Specific Functions

CT2 Formatter

The CT2 formatter provides full support of CT2 signaling layers 1 and 2. It includes a synchronization (SYN) channel handler, a D-channel handler with hardware CRC (Cyclic Redundancy Check) and parity generation and checking, a B-channel handler, and timing recovery. Figure 1 is a block diagram of the formatter.

The CT2RX pin is the digital baseband receive data input. Transmit data appears in analog form at the TXI and TXQ pins and in digital form at the BDP1_OUT3 pin.

Timing Recovery

The CAI CT2 physical layer operates in one of four time division duplex modes called multiplexes. The CPP (Cordless Portable Part, or handset) is a timing slave to the CFP (Cordless Fixed Part, or base station) in multiplexes MUX1 and MUX2. During the receive sub-frame, the CPP phase locks to receive data, keying on data transitions. In normal operation, the CFP does not phase lock to CPP transmit data, expecting data to arrive correctly positioned in time according to CT2 specifications.

When the CPP initiates a link using MUX3, the CFP acts temporarily as a slave in order to correctly receive data. Once the CFP has locked to the incoming MUX3 frame and recognized the correct identification codes, the CFP terminates its MUX3 reception under software control and begins transmitting MUX2. When the CPP recognizes the MUX2 frame, it terminates its MUX3 transmission and becomes a MUX2 timing slave.

SYN Channel and Link Synchronization

The synchronization (SYN) channel is present in multiplex modes MUX2 and MUX3 in order to achieve burst synchronism. In MUX2, the SYN channel is a 10-bit preamble and a 24-bit CHM or SYNC pattern. In MUX3, it is a 12-bit preamble and a CHMP pattern.

The receiver searches the incoming data stream for either a CHM or a SYNC pattern and reports the synchronization status in the RXTMGR register. Once a CHM or SYNC pattern is received, an interrupt is propagated to the central interrupt controller. Once the CHM or SYNC pattern is located, the receiver frame timing remains locked. If the receiver fails to receive its expected CHM or SYNC, it generates a sync error interrupt. Writing the SYNCTR command releases the receiver to resynchronize by seeking the next CHM or SYNC pattern.

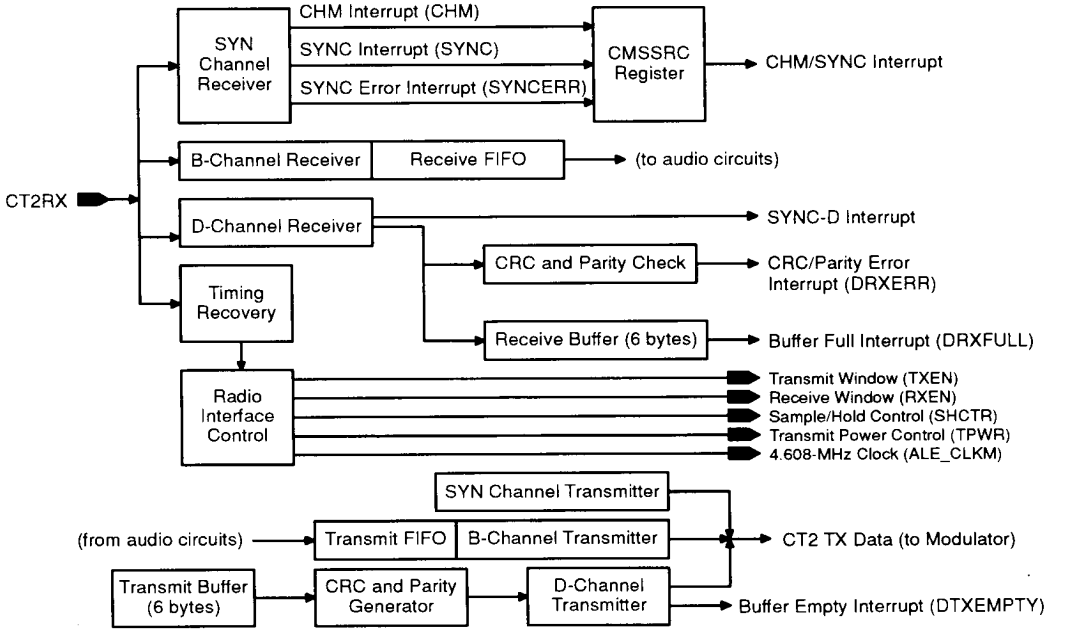


Figure 1. CT2 Formatter Block Diagram

B-Channel Operation

The B-channel handler aligns the 64 B-channel audio bits within the MUX1 transmit and receive frames and performs scrambling specified by ETSI in order to ensure reasonably random output data sequences for timing recovery and spectral considerations. In the transmitter, bits 3, 4, 6, 9, 14, 16, 18, 20, 22, 23, 27, 28, 29, 30, 31, 34, 35, 37, 40, 45, 47, 49, 50, 51, 53, 54, 58, 59, 60, 61, and 62 are inverted (scrambled). In the receiver, they are re-inverted (descrambled).

The B-channel path from the microphone and earpiece interfaces to the RF interface induces approximately 1.95 ms round-trip delay.

D-Channel Operation

The D Channel exists in all multiplex modes for link management. Layer 3 messages consist of a number of packets, each made up of one to six code words. Code words are eight octets long. The first six bytes are loaded by software into the transmit buffer or read by software from the receive buffer. The last two octets are a hardware generated check field. The first 15 bits of the check field are a CRC code. The last bit of the check field is a parity bit, such that the whole 64-bit code word has even parity.

Software controls the marking of the beginning of a new packet with a SYNCD pattern by programming a control register. Between packets, IDLE_D (alternating ones and zeroes) is transmitted.

D-Channel Transmit Operation

The D-channel transmitter drives IDLE_D when not transmitting a packet. When a packet is to be transmitted, software sets the SYNCD control bit in the SYNCDC register and loads the transmit buffer with the first 6 bytes of the code word. The transmitter drives the SYNCD pattern and begins transmission of the data bytes contained in the buffer. Once six bytes have been sent, the transmitter sends the CRC field, inverts the 15th bit, and appends the parity bit.

D-Channel Receive Operation

The D-channel receiver begins packet reception after recognizing a SYNCD data pattern. On reception of SYNCD, the receiver drives an interrupt to the on-chip interrupt controller.

The next six D-channel bytes are loaded in the receive buffer. The following 16 bits of CRC and parity are routed to a CRC/parity check circuit, which generates an interrupt in case of error. At the end of the check field reception, an interrupt notifies software that the receive buffer contains a code word. The check field is not loaded in the receive buffer.

In the case of a multiple code word packet, the next code words will be appended to the end of the preceding code words until a Layer 2 packet is completed.

The receiver continues loading the first six bytes of the incoming code words into the receive buffer until software writes a control command called RDATAC, after which the D-channel receiver will ignore data until the next SYNCD pattern is detected.

RF Delay Compensation

The modem delay measurement facility provides a means for compensating RF delay to meet CT2 specifications for relative timing of receive and transmit portions of the frame at the antenna. The feature requires the telephone RF circuitry to provide a radio frequency loopback at the antenna from transmitter to receiver.

ETSI specifies a fixed timing relationship between receive and transmit subframes, measured at the antenna.

$$t_{CFPRX \rightarrow CFPTX} = t_{RXRF} + t_{ADJ} + t_{MOD} + t_{TXRF}$$

where the left side of the equation is the time difference between the last received bit of one frame and the first transmitted bit of the next frame for the CFP, specifically 4.5 bit periods in MUX1.4 and 6.5 bits in MUX1.2 and MUX2. Receive data must pass through the receiver RF circuitry, inducing delay t_{RXRF}. Likewise, transmit data experiences delay $t_{MOD} + t_{TXRF}$ in the modulator and the RF sections. t_{ADJ} is the modem delay measurement result which is calculated by hardware to compensate the right hand side of the equation and is applied to the transmit controller so that CT2 specifications are met. The measurement operation is initiated by software command and normally occurs at power-up. During measurement, the transmitter and receiver are simultaneously enabled so that transmit data is looped back to the receiver via the antenna. The measurement circuit counts the delay in 870-nsec increments between transmission and reception of CHM and returns the result in the MODDLY register.

The measured delay in MODDLY may be moved to non-volatile memory, such as EEPROM, for use in future link initiation sequences. To force the modem delay compensation to a previously determined value, software writes the value to MODDLY.

Radio Interface Controls

The Am79C410 drives TXEN and RXEN pins High to enable RF amplifiers during the respective transmit and receive portions of the CT2 frame.

The CT2RX pin is the digital receive data input. Transmit data is available in analog form at the TXI and TXQ pins, detailed in the *Modulator* section. Digital transmit data appears on the BDP1_OUT3 pin when that pin is appropriately configured.

The TXPWR pin is controlled by software through the TPOWER register to accommodate CT2 specifications for normal and low power transmissions.

The sample/hold control (SHCTR) pin provides timing for an external sample/hold circuit which may be used to control DC offset in the receiver discriminator.

RSSI

The Receive Signal Strength Indicator (RSSI) determines the value of the RSSI analog input pin, representing the level of the received RF signal. The circuit includes a 5-bit successive approximation A/D converter requiring approximately 10-µsec conversion time, during which the RSSI pin should be held constant within 1 LSB of resolution.

The RSSI operates in synchronous and asynchronous modes, according to the CT2 link synchronization status. Asynchronous mode is intended for the channel scanning application and the A/D conversion begins immediately after a conversion request. Synchronous mode, for link monitoring, is entered automatically when the link has synchronized. In synchronous mode, all conversion requests are timed by internal sampling pulses which occur only in the receive portion of the CT2 frame.

Modulator

The modulator is a baseband GMSK modulator specifically designed to meet or exceed CT2 spectral requirements. Serial transmit data from the CT2 formatter is digitally filtered and converted to two single-ended quadrature analog outputs, called TXI and TXQ. The outputs are intended to be externally mixed with the IF or RF carrier and summed to obtain the desired frequency modulated signal (see Figure 2).

The Gaussian filter response is approximated as a 6th order Bessel filter with linear phase response and a 3-dB cut-off frequency of 14.4 kHz (i.e., the normalized 3-dB bandwidth $B_bT = 0.8$). The D/A conversion samples at 4.608 MHz with 7-bit precision over a ±0.5-V AC range, DC referenced to the MREF pin. Net delay through the modulator, from digital input to analog output, is approximately 15.1 µs.

The mathematical description of TXI and TXQ, depicted in Figure 2, is

$$TXI = 0.5\ V \times I(t) + MREF$$

$$TXQ = 0.5\ V \times Q(t) + MREF$$

$$I(t) = \sin\left(\int \omega_m(t)dt\right)$$

$$Q(t) = \cos\left(\int \omega_m(t)dt\right)$$

where $\omega_m(t)$ is the instantaneous GMSK message frequency, which has a range of ±18.0 kHz and the step response defined by the digital filter. Outputs are defined such that when I and Q are subjected to a quadrature mixer and a carrier ω_c, as in Figure 3, the result y(t) is

$$y(t) = I \times \cos(\omega_c t) + Q \times \sin(\omega_c t)$$

$$= \sin\left(\omega_c t + \int \omega_m(t)dt\right)$$

The instantaneous frequency of y(t) is then $\omega_c + \omega_m(t)$ and there are no sidelobes. The frequency eye-diagram of y(t) is shown in Figure 4.

A passive single-pole low pass filter with 3-dB frequency around 100 kHz is necessary at both TXI and TXQ outputs to remove sampling images at 4.608 MHz. The filter must have a minimum impedance of 1 kΩ. For stability, the maximum capacitance from pin to ground cannot exceed 100 pF.

To reduce frequency spread, the modulator ramps up smoothly when transmit data is driven to it from the CT2 formatter. During the ramp-up period, I is zero and Q rises from zero to full scale so that the amplitude of y(t) increases smoothly from zero to full scale. Likewise, the modulator ramps down smoothly at the end of the transmission.

The modulator responds to the transmit data without software intervention. A test register provides test modes that force the modulator to send fixed or externally generated data patterns for RF circuit evaluation.

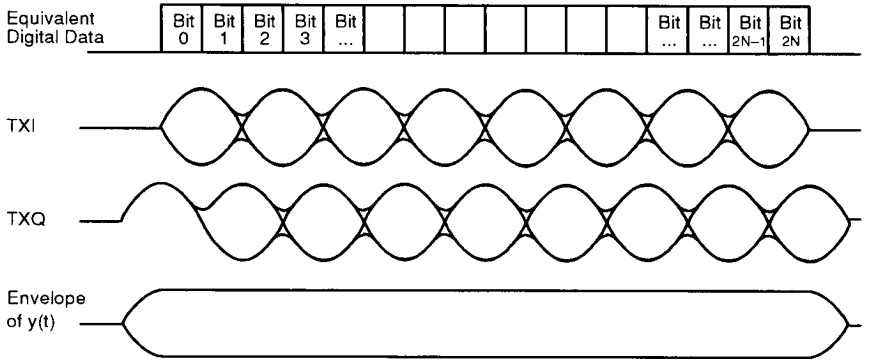


Figure 2. Modulator Waveform

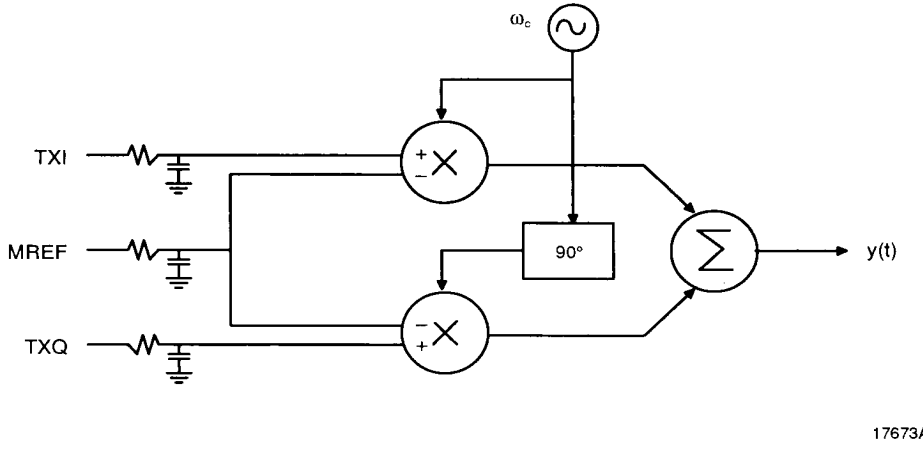


Figure 3. Modulator I/Q Mixer Block Diagram

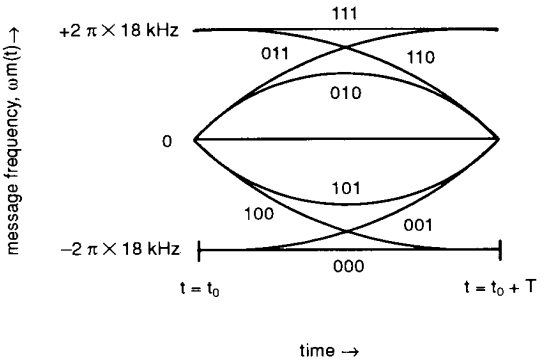


Figure 4. Modulator Eye Diagram for Three-Term Data Sequences

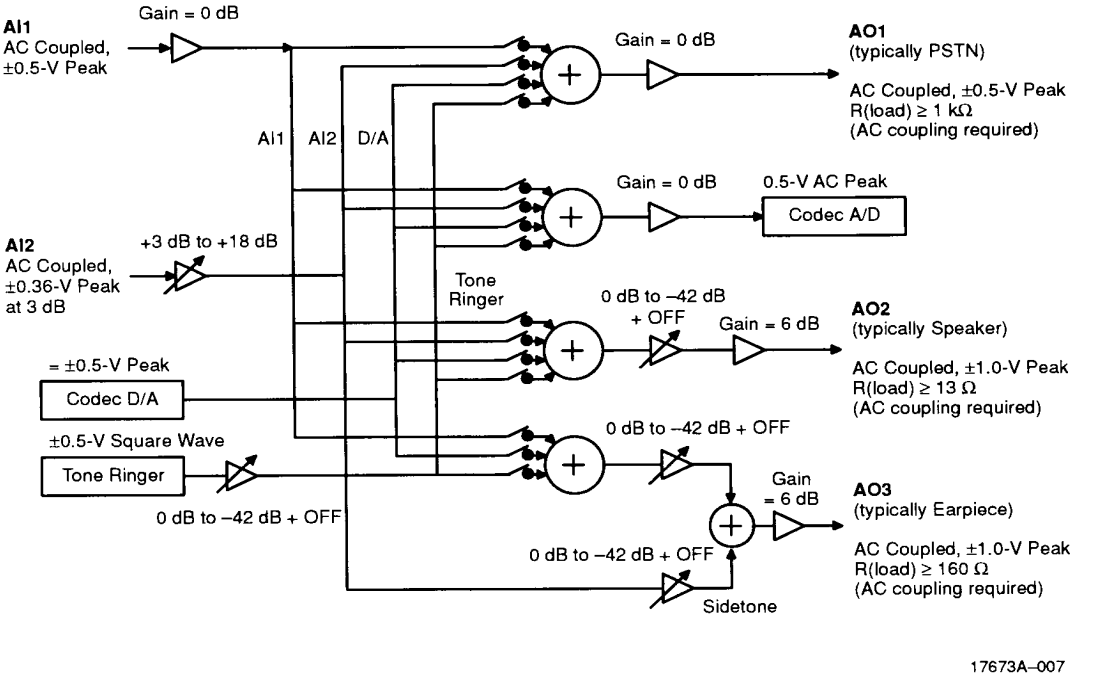


Figure 5. Audio Multiplexer

Audio Functions

Audio Multiplexer

Figure 5 shows the audio multiplexer and interface. The audio multiplexer allows flexibility in summing and applying gains to the various analog inputs and outputs.

ADPCM Codec

The codec, shown in Figure 6, performs 32-kbit/s ADPCM (Adaptive Differential Pulse Code Modulation) conversion in accordance with CCITT G.721.

The codec can be programmed in one of four configurations. The first is normal ADPCM codec configuration, which performs ADPCM ↔ analog conversion. Attenuations in the transmit and receive voice paths are programmed in the TXATTN and RXATTN registers.

The PCM codec configuration performs A-law PCM ↔ analog conversion. The SDIN and SDOUT multifunction pins provide 64-kbit/s PCM data I/O. The SCLKOUT multifunction pin drives the 512-kHz/64-kbit/s burst mode data clock.

The codec loopback 2 configuration is a digital linear data loopback through the A/D and D/A without companding.

The transcoder configuration causes the codec to behave as an A-law PCM / ADPCM transcoder. The feature may be used to verify that the ADPCM algorithm implemented in the CT2 PhoX IC conforms to CCITT G.721.

Noise Suppression

The noise suppression feature recognizes noise in the ADPCM receive data stream and mutes the receive path in response. B-channel noise is detected in two ways:

1. Non-speech frequency content, indicating bit errors
2. Jitter in the CT2 Common Air Interface received data, indicating likely loss of link synchronization

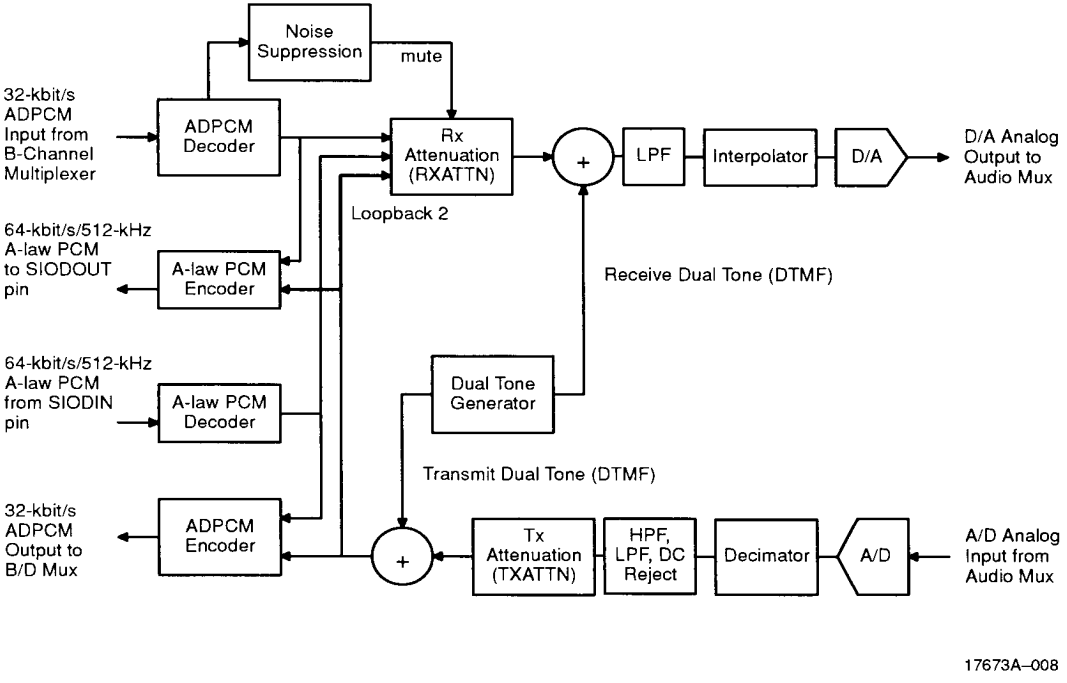


Figure 6. Codec Block Diagram

Dual Tone Generation

Figure 7 is a block diagram of the dual tone generator, which drives DTMF or alerting tones in the transmit and receive directions. Each of the two tones has a programmable frequency and amplitude. The tones are added to the transmit and receive paths of the codec, with independent gain adjustment in each path.

Tone Ringer

The tone ringer generates a square wave of programmable frequency and amplitude. The ringer waveform is an input to the audio multiplexer and may appear at any of the analog outputs, AO1, AO2, or AO3, if appropriately configured. The ringer smoothly switches from one programmed frequency to a newly programmed value with no irregular pulses.

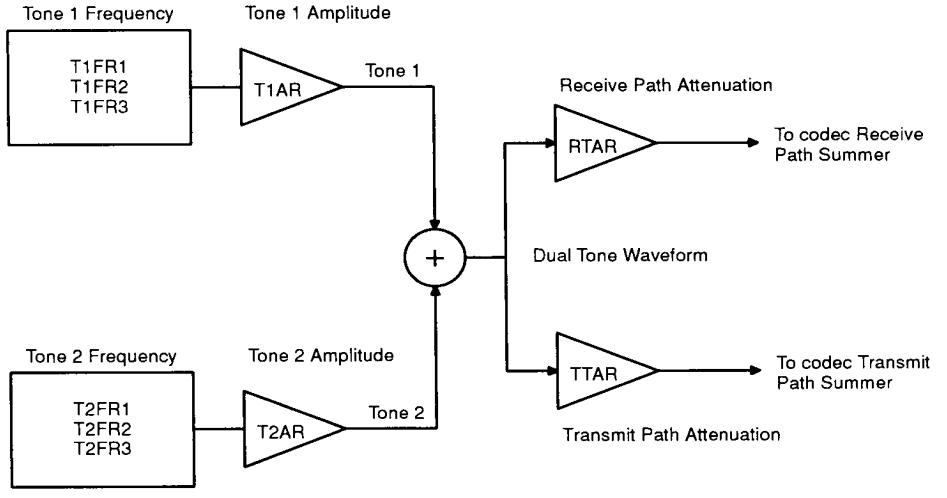
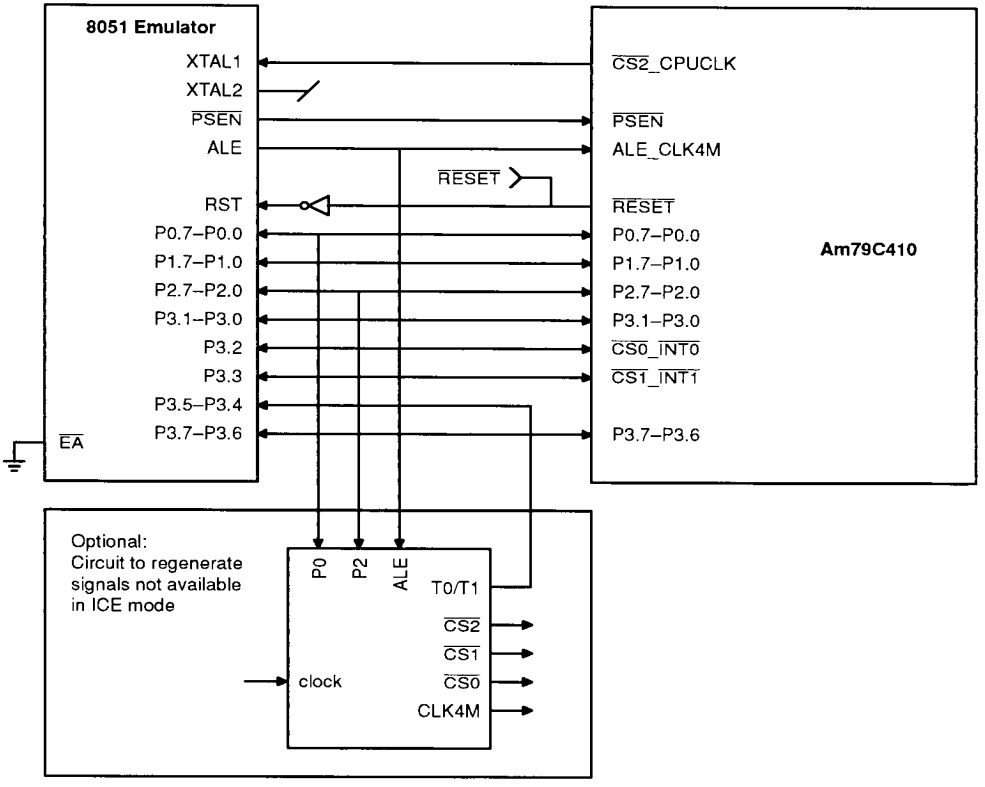


Figure 7. Dual Tone Generator Block Diagram

In-Circuit Emulation (ICE) Mode

ICE mode is for code development using an 8051 Family emulator, and is entered by driving the TRI1 pin to ground while reset is active. As shown in Figure 8, in ICE mode, an external processor with 8051 bus timing drives the Port 0, Port 1, Port 2, Port 3, and ALE inputs of the Am79C410, replacing the on-chip 8032.



17673A–010

Figure 8. Driving the Am79C410 with an 8051 Family In-Circuit Emulator

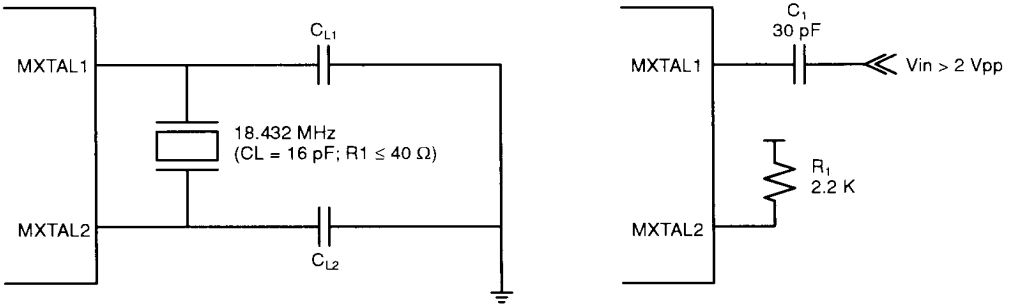
Hardware Applications

Main Crystal Oscillator

The main oscillator interface supports an 18.432-MHz parallel resonant crystal oscillator or an AC coupled digital logic level, as in Figure 9. The nominal drive level is 100 µW to work with surface-mount crystals.

Figure 10 is an equivalent circuit model for the crystal. R1, L1, and C1 make up the motional arm and represent the crystal's physical element. C0 is the pin-to-pin parasitic capacitance of the package. In order to avoid startup problems, the load capacitance CL, which includes the discrete load capacitors $C_{L1} \cdot C_{L2}/(C_{L1} + C_{L2})$ and parasitics, should be less than 20 pF. Preferred typical crystal parameters are

f	=	18.432 MHz
C1	=	9.2 fF
L1	=	8.1 mH
R1	≤	40 Ω
C0	=	2.5 pF
CL	=	16 pF
P	≤	300 µW

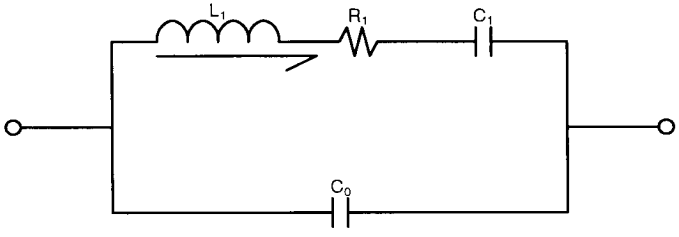


a. Crystal Source

b. CMOS Level Digital Source

17673A-011

Figure 9. Main Crystal Interface



17673A-012

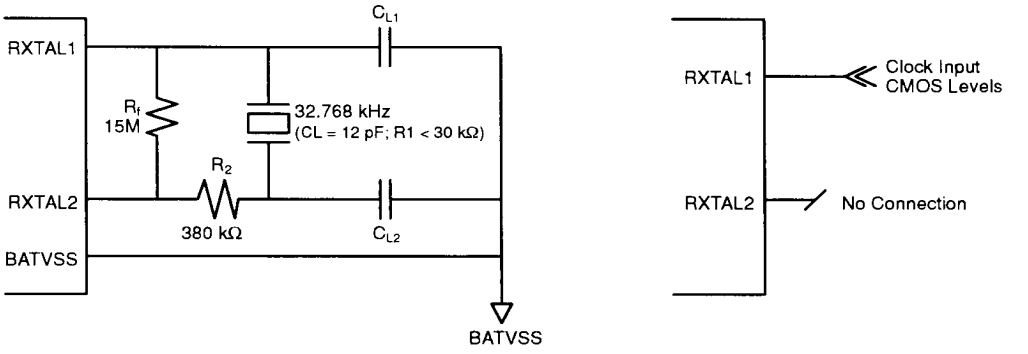
Figure 10. Crystal Parameter Model

RTC Crystal Oscillator

The real time clock timing source is a 32.768-kHz parallel resonant AT cut crystal or a digital CMOS level input. If a CMOS input is used on RXTAL1, the RXTAL2 output should be left unconnected. The RTC oscillator has been designed to operate at low voltages and very low power. The crystal model in Figure 10 applies. Figure 11 shows the recommended RTC crystal interface.

Preferred typical crystal parameters are

f	=	32.768 MHz
C1	=	2.9 fF
L1	=	8.078 mH
R1	≤	30 kΩ
C0	=	1.4 pF
CL	=	$C_{L1} \cdot C_{L2}/(C_{L1} + C_{L2})$ + parasitics = 12 pF
P	≤	1 μW



a. Crystal Source

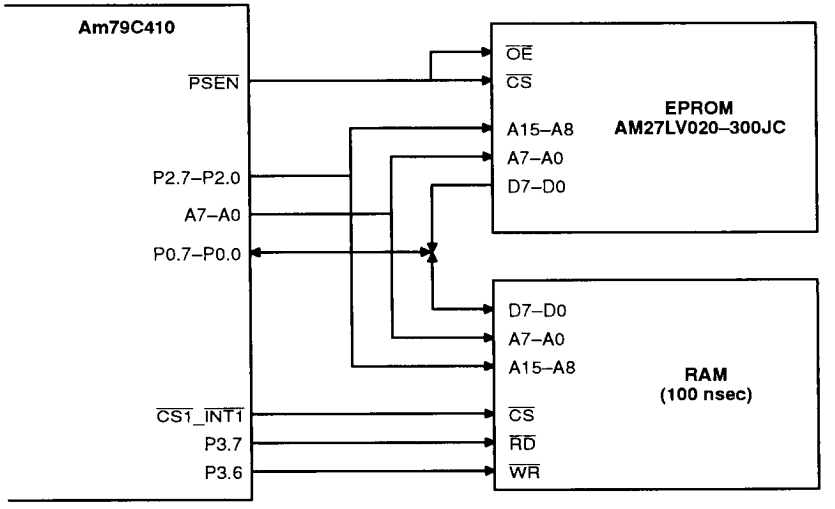
b. CMOS Digital Input Source

17673A–013

Figure 11. RTC Crystal Interface

ROM and RAM Interface

Program memory in EPROM and optional data memory can be connected directly to the CT2 PhoX controller.

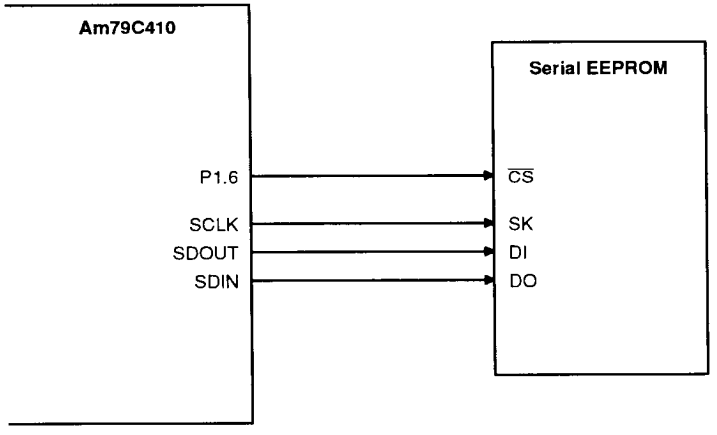


17673A–013

Figure 12. Memory Interface

EEPROM Interface

The CT2 PhoX controller connects directly to many popular serial access devices, including EEPROMS, synthesizers, and LCDs.

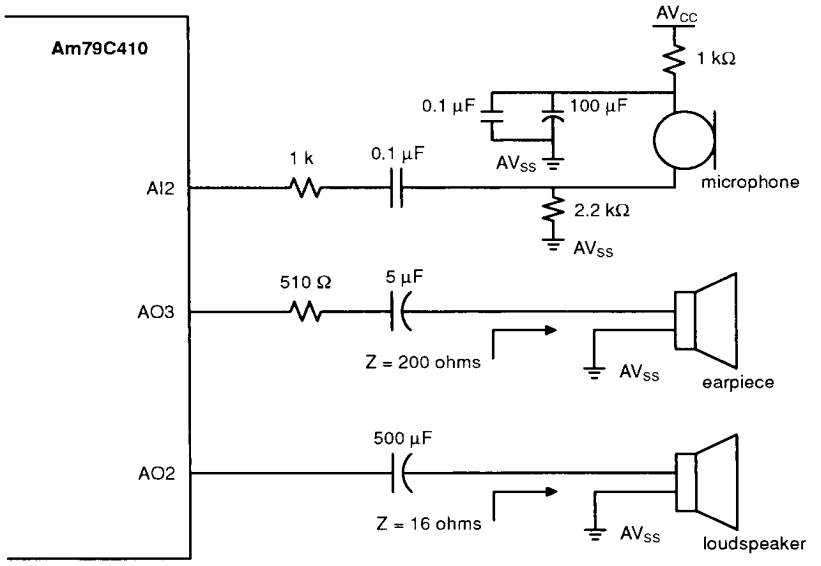


17673A–014

Figure 13. Serial EEPROM Interface

Handset and Loudspeaker Interface

A typical audio interface is shown.

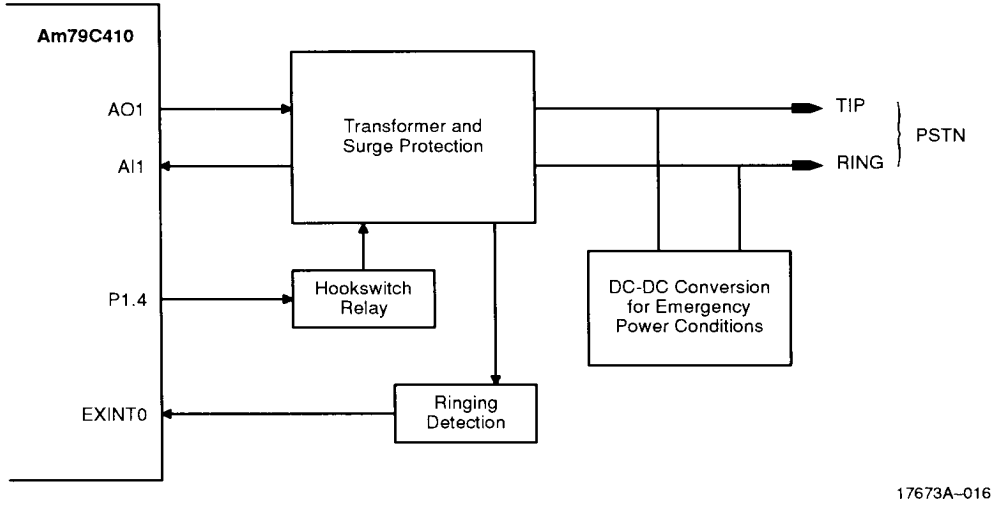


17673A–015

Figure 14. Interface to Handset and Loudspeaker

PSTN Interface

Analog interface pins AO1 and AI1 are designed to connect to external circuitry that interfaces with the Public Switched Telephone Network (PSTN).



17673A–016

Figure 15. Interface to Public Switched Telephone Network

Key Scanner Interface

Figure 16 demonstrates the connection of a 36-key keypad to the Am79C410. Columns 5 and 6 may be eliminated for a 24-key keypad.

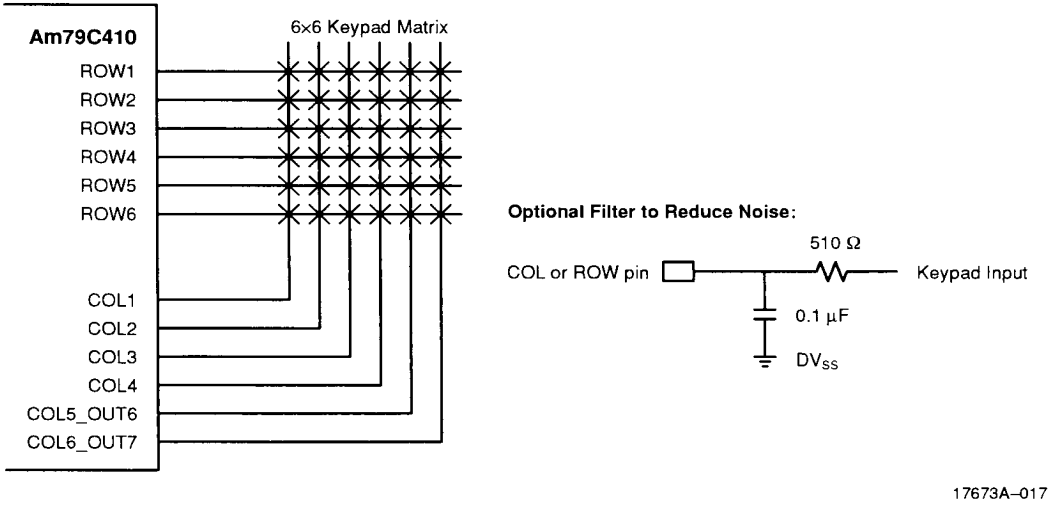


Figure 16. Interface to a 6×6 Keypad Matrix

Encryption Port Application

32-kbit/s B-channel data may be routed off-chip to an external encryption circuit for security reasons.

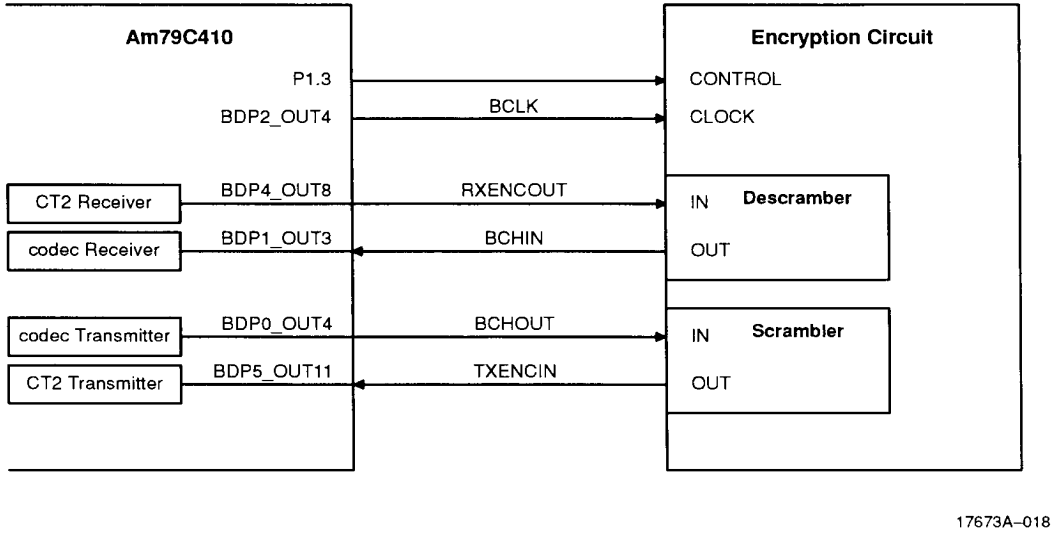


Figure 17. Voice Encryption Path

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with power applied ..... –40°C to +85°C

Supply Voltage to ground potential, continuous ..... 0 V to 6.0 V

Lead Temp. (10-sec hot-bar soldering) ..... 300°C

Lead Temperature (Reflow) ..... 107°C

Maximum Power Dissipation ..... 1.5 W

Voltage from any pin to V_{SS} ..... V_{SS} – 0.3 V to V_{CC} + 0.3 V

DC Input/Output Fault Current ..... 30 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices

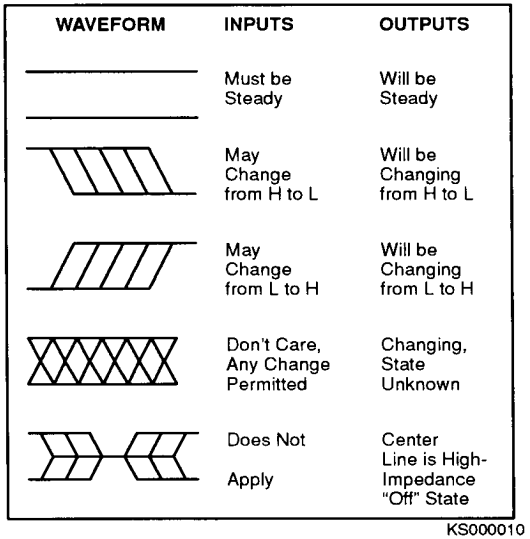
Operating V_{CC} Range ..... 2.7 V to 3.6 V, ref. to V_{SS}

Extended Voltage Range Device Only ..... 2.7 V to 5.25 V, ref. to V_{SS}

Ambient Temperature ..... 0°C to +70°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

KEY TO SWITCHING WAVEFORMS



KS000010

Digital I/O

Digital Pin DC Characteristics over operating ranges, unless otherwise specified

Applies to all pins except MXTAL1, MXTAL2, RXTAL1, RXTAL2, RSSI, TXI, TXQ, MREF, IREF, CFILT, AI1, AI2, AO3–AO1, and BATVSS.

Parameter	Parameter Description	Test Conditions	Preliminary			Unit
			Min	Typ	Max	
V_{IL}	Input Low Voltage		–0.3		$0.2 \times V_{CC}$	V
V_{IH}	Input High Voltage		$0.7 \times V_{CC}$		$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	I_{OL} = 5 mA			$0.1 \times V_{CC}$	V
V_{OH}	Output High Voltage (except Reset)	I_{OH} = –1 mA	$0.9 \times V_{CC}$			V
I_L	Input Leakage, Output High Z Leakage	$V_{SS} < V_{IN} < V_{CC}$ $V_{SS} < V_{OUT}$ (High Z) $< V_{CC}$			±10	µA
I_{OH}	Output Current Drive, Driving 1	V_{OH} = 2.4 V, V_{CC} = 3 V(1) $V_{OH} = 0.9 \times V_{CC}$, V_{CC} = 3 V(1)	–2 –1			mA
I_{OL}	Output Current Drive, Driving 0	$V_{OL} = 0.1 \times V_{CC}$, V_{CC} = 3 V(1) V_{OL} = 0.5 V, V_{CC} = 3 V(1)	5 10			mA
C_I	Pin Input Capacitance	temp = 25°C, freq = 1 MHz		10		pF
C_O	Pin Output Capacitance	temp = 25°C, freq = 1 MHz		15		pF
C_{L1}	Load Capacitance (except TRI0_OUT10 and TRI1)				40	pF
C_{L2}	Load Capacitance, TRI0_OUT10, TRI1 pins				50	pF
R_{L1}	Resistance to V_{SS}/V_{CC} for Logic 0/1, TRI0/TRI1 pins				50	Ω
R_{L2}	Leakage to V_{SS} or V_{CC} for Logical Mid-supply, TRI0/TRI1 pins		250			kΩ
R_{KO}	Keypad Open Circuit Resistance, Row to Column Pin		150			kΩ
R_{KS}	Keypad Short Circuit Resistance, Row to Column Pin				2	kΩ
I_{CC}	Supply Current	V_{CC} = 3 V; Shutdown Standby (2) Active (3)		0.3 4.0 16.0		mA

Notes:

1. *These parameters apply to all digital outputs when they are actively driven. Microcontroller Port 1 and Port 3 pins are actively driven High for two cycles of the CPUCLK and then held High by a weak "keeper" transistor.*
2. *Oscillator on, microcontroller clock = 576 kHz, CT2 formatter, RSSI A/D, and key scanner on; all other modules off.*
3. *I/Q modulator, codec, handset I/O, CT2 formatter, key scanner, RSSI A/D modules on; microcontroller clock = 1.152 MHz, serial port on at 36-kHz clock rate.*

Audio

0 dBm0 Reference Level and Digital Full Scale

A 0 dBm0 digital signal level is nominally equivalent to a 0.25-Vrms tone at the AI1 input or AO1 output pin. Digital full scale is +3.14 dBm0 for tones.

Audio Performance

The ADPCM transcoder is fully compliant with CCITT Recommendation G.721.

The codec is designed to meet CCITT Recommendation G.714 requirements for signal to distortion, gain tracking, frequency response, and idle channel noise specifications as defined in the *Transmit and Receive Half Channel Transmission Characteristics* table. Verification of conformance to G.714 is by device characterization. Production testing of individual parts includes only those parameters consistent with the testing requirements of the ETSI CT2 specification, shown in the *Audio Path Performance Specifications* table.

The half channel parameters are specified in the *Audio Path Performance Specifications* and *Transmit and Receive Half Channel Transmission Characteristics* tables for the transmit path from the AI1 audio input pin to the codec A-law serial data output with 0-dB analog and digital gains programmed. The parameters for the receive path from the codec A-law serial data input to the AO1 audio output pin are specified for 0-dB analog and digital gains. The parameters apply for A-law PCM conversion and assume psophometric filtering.

Audio Analog Pin Characteristics (applies to IREF, CFILT, AI1, AI2, AO1–AO3)

Parameter	Parameter Description	Test Conditions	Preliminary			Unit
			Min	Typ	Max	
V_{FSI}	Full Scale Input Swing	AI1 AI2, AI2CTR gain = 3 dB		±0.5 ±0.36		V
Z_I	Input Impedance (AI1, AI2)		10			kΩ
V_{FSO1}	Full Scale Output Swing (AO1)	$R_{L1} \geq 1$ kΩ		±0.5		V
V_{FSO2}	Full Scale Output Swing (AO2, AO3)	$R_{L2} \geq 13$ kΩ $R_{L3} \geq 160$ kΩ		±1.0		V
R_{L1}	Load Resistance, AO1 to Ground	AC coupled	1			kΩ
R_{L2}	Load Resistance, AO2 to Ground	AC coupled	13			Ω
R_{L3}	Load Resistance, AO3 to Ground	AC coupled	160			Ω
C_L	Load Capacitance to AC Ground				100	pF
I_L	High Z Output Leakage (AO1–AO3)			< 10		µA
V_{DC1}	Self-bias Voltage (AI1, AI2, AO1)			0.32 × V_{CC}		V_{dc}
V_{DC2}	Self-bias Voltage (AO2, AO3)			0.5 × V_{CC}		V_{dc}
R_{IREF}	External IREF Resistance (±1%) to AV_{SS}			62.5		kΩ
C_{CFILT}	External CFILT Capacitance to AV_{SS}			11		µF

Audio Path Performance Specifications (Analog Outputs AO1, AO2, and AO3 Unloaded)

Parameter Description	Test Conditions and Notes	Min	Max	Unit
Idle Channel Noise	1. Receive: ADPCM → AO3 2. Transmit: AI2 → ADPCM 3. Audio Mux (all analog): AI1 → AO1, AI1 → AO2		–75 –70 –70	dB
Signal to Total Distortion, 1-kHz tone at –10 dBm0	1. Receive: ADPCM → AO3 2. Transmit: AI2 → ADPCM 3. Audio Mux (all analog): AI1 → AO1, AI1 → AO2	35 35 35		dB
Absolute Gain Error, 1-kHz tone at –10 dBm0	1. Receive: ADPCM → AO3 2. Transmit: AI2 → ADPCM 3. Audio Mux (all analog), 0 dB: AI1 → AO1, AI1 → AO2	–1 –1 –1	+1 +1 +1	dB
DTMF Absolute Gain Error	Dual Tone Generator → analog AO1	–1	+1	dB
DTMF Frequency Deviation	Dual Tone Generator → analog AO1	–1	+1	%
DTMF Signal to Total Distortion	Dual Tone Generator → AO1 Normal mode, 0-dB gain: DTMF only mode: f < 1650 Hz f ≥ 1650 Hz	 31 31 n/a		dB
Tone Ringer Absolute Gain Error	Tone ringer → AO1, AO2, AO3	–1	+1	dB

Transmit and Receive Half Channel Transmission Characteristics

Transmit Half Channel gain is 0 dB from AI1 pin; Receive Half Channel gain is 0 dB at the AO1 pin.

Parameter Description	Test Conditions and Notes	Min	Max	Unit
Frequency Response (attenuation vs frequency, relative to 1020 Hz)	–10-dBm0 Input 50 Hz ≤ f ≤ 60 Hz (transmit only) ≤ 300 Hz 300 Hz < f ≤ 3 kHz 3 kHz < f ≤ 3.4 kHz 3.4 kHz < f < 3.6 kHz 3.6 kHz < f ≤ 3.9 kHz 3.9 kHz < f < 4.0 kHz	 20 –0.25 –0.25 –0.25 –0.25 0.0 5.0	 0.25 0.9 	dB
Group Delay vs Frequency	–10-dBm0 Input 500 Hz ≤ f ≤ 600 Hz 600 Hz < f ≤ 1 kHz 1 kHz < f ≤ 2.6 kHz 2.6 kHz < f < 2.8 kHz		 750 380 130 750	µs
Gain Tracking, CCITT Method 2	1020-Hz Input +3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	 –0.3 –0.6 –1.6	 0.3 0.6 1.6	dB
Signal to Total Distortion, CCITT Method 2	1020-Hz Input 0 to –30 dBm0 –40 dBm0 –45 dBm0	 35 29 24		dB
Idle Channel Noise	Transmitter Receiver		–70 –75	dBm0
Absolute Gain Tolerance	1020 Hz at 0 dBm0	–0.5	+0.5	dB
Transmitter out-of-band Signal Rejection, relative to 1 kHz	4.6 kHz at –25 dBm0 8.0 kHz at –25 dBm0	30 40		dB
Receiver Spurious Noise	0 dBm0, 300 Hz ≤ f ≤ 3.4 kHz		–35	dBm0

RSSI

Inputs above the full scale V_{FS} read as full scale. Inputs below the minimum code input voltage V_{ZERO} read as the minimum input code.

RSSI Characteristics

Parameter	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{ZERO}	RSSI Minimum Code Input Voltage		0.199	0.220	0.241	V
V_{FS}	RSSI Maximum Code Input Voltage		1.204	1.267	1.330	V
ERR_{LIN}	RSSI A/D Integral Linearity Error				±1	LSB
T_{CONV}	RSSI A/D Conversion Time			10		µs

I/Q Modulator

All spectral requirements apply to TXI and TXQ outputs referenced to MREF and filtered by single pole passive low pass filters with 3-dB frequency of 100 kHz. All dBV values are based on the assumption that –9 dBV at I and Q yields +10 dBm at the final RF output. Adjacent channel power and spurious emissions are measured during constant transmission of pseudo-random data. Spectral values are characterized for the device and are not production tested on every individual part.

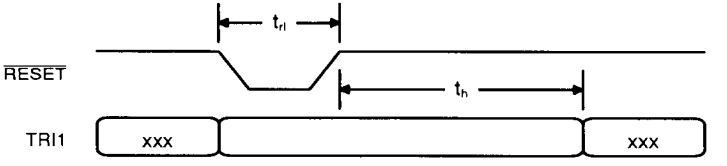
I/Q Modulator Characteristics (applies to TXI, TXQ, and MREF pins)

Parameter	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{MREF}	MREF Output Voltage		0.475 × V_{CC}	0.5 × V_{CC}	0.525 × V_{CC}	V_{dc}
ΔV_{DC1}	Differential Offset between TXI and TXQ				40	mV
ΔV_{DC2}	Differential Offset between MREF and TXI or TXQ				30	mV
R_{OZ}	Disabled State Output Impedance			25		kΩ
R_L	Load Resistance on TXI or TXQ		1			kΩ
C_L	Load Capacitance to AC Ground				100	pF
V_{FS}	Full Scale AC Output at TXI or TXQ	Digital data input is all 0s or all 1s (i.e., 18-kHz sinusoid)		0.5		V_{ac}
V_O	Output Level at TXI or TXQ	Driving full scale sinusoid	–10	–9	–8	dBV
V_{OI}/V_{OQ}	Relative Levels of TXI and TXQ	Digital data input is all 0s or all 1s	–0.5		+0.5	dB
Padj	Adjacent Channel Power	Random data integrated over a ±40-kHz band			–39	dBV
SE1	Spurious Emissions	150 kHz ≤ freq ≤ 2 MHz 2 MHz < freq < 10 MHz			–65 –79	dBV
Tdly	Absolute Delay from Digital Input to Analog Output			15.1		µs

Reset

Reset Timing

Parameter	Parameter Description		Test Conditions	Min	Typ	Max	Unit
t_{rl}	Reset Pulse Width (Low):	Input Output		2.6	 1.78		µs ms
t_h	TRI1 Hold after Reset				3.56		ms



17673A-011

Figure 18. Reset Timing

Microcontroller and Address Decoder

Am79C410 On-Chip Microcontroller (80C32T2) and Addresses Decoder Switching Characteristics

All units are in nanoseconds unless otherwise specified.

#	Parameter	Parameter Description	Variable Clock Rate Min	Variable Clock Rate Max	9.216-MHz Min	9.216-MHz Max
t1	1/TCLCL	CPUCLK Frequency	0 MHz	9.216 MHz	—	—
t2	TLHLL	ALE Pulse Width	2TCLCL – 40		177	
t3	TAVLL	Address Valid to ALE Low	TCLCL – 55		53	
t4	TLLAX	Address Hold after ALE Low	TCLCL – 35		73	
t5	TLLIV	ALE Low to Valid Instruction In		4TCLCL – 100		334
t6	TLLPL	ALE Low to $\overline{PSEN}$ Low (1)	3TCLCL – 40		68	
t7	TPLPH	$\overline{PSEN}$ Pulse Width (1)	2TCLCL – 45		280	
t8	TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		3TCLCL – 105		220
t9	TPXIX	Input Instruction Hold after $\overline{PSEN}$	0		0	
t10	TPXIZ	Input Instruction Float after $\overline{PSEN}$		TCLCL – 25		83
t11	TAVIV	Address to Valid Instruction In		5TCLCL – 105		437
t12	TPLAZ	$\overline{PSEN}$ Low to Address Float (1)		2TCLCL + 10		10
t13	TRLRH	$\overline{RD}$ Pulse Width	6TCLCL – 100		551	
t14	TWLWH	$\overline{WR}$ Pulse Width	6TCLCL – 100		551	
t15	TRLDV	$\overline{RD}$ Low to Valid Data In		5TCLCL – 165		377
t16	TRHDX	Data Hold after $\overline{RD}$	0		0	
t17	TRHDZ	Data Float after $\overline{RD}$		2TCLCL – 70		147
t18	TLLDV	ALE Low to Valid Data In		8TCLCL – 150		718
t19	TAVDV	Address to Valid Data In		9TCLCL – 165		811
t20	TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	3TCLCL – 50	3TCLCL + 50	275	375
t21	TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	4TCLCL – 130		304	
t22	TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL – 60		48	
t23	TQVWH	Data Valid to Write High	7TCLCL – 150		609	
t24	TWHQX	Data Hold after $\overline{WR}$	TCLCL – 50		58	
t25	TRLAZ	$\overline{RD}$ Low to Address Float		0		0
t26	TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	TCLCL – 40	TCLCL + 40	68	148
t27	TRWCS	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	TCLCL – 30	TCLCL + 10	78	118

Note:

1. *These parameters behave differently for the 9.216-MHz clock rate than for slower clock rates for power consumption considerations. Values listed under the Variable Clock Rate columns apply to all CPUCLK rates other than 9.216 MHz.*

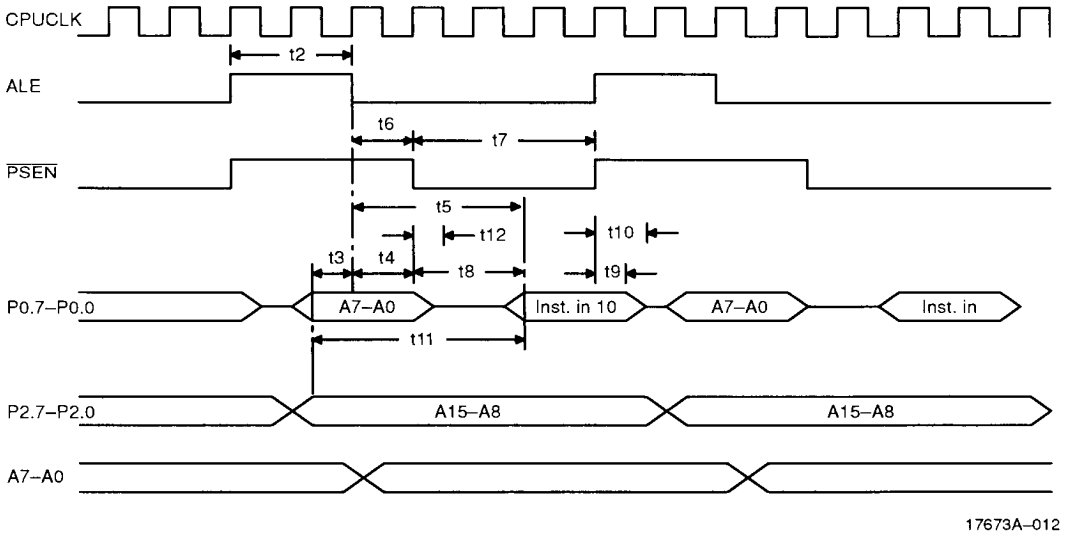


Figure 19. Microcontroller External Program Memory Read Cycle

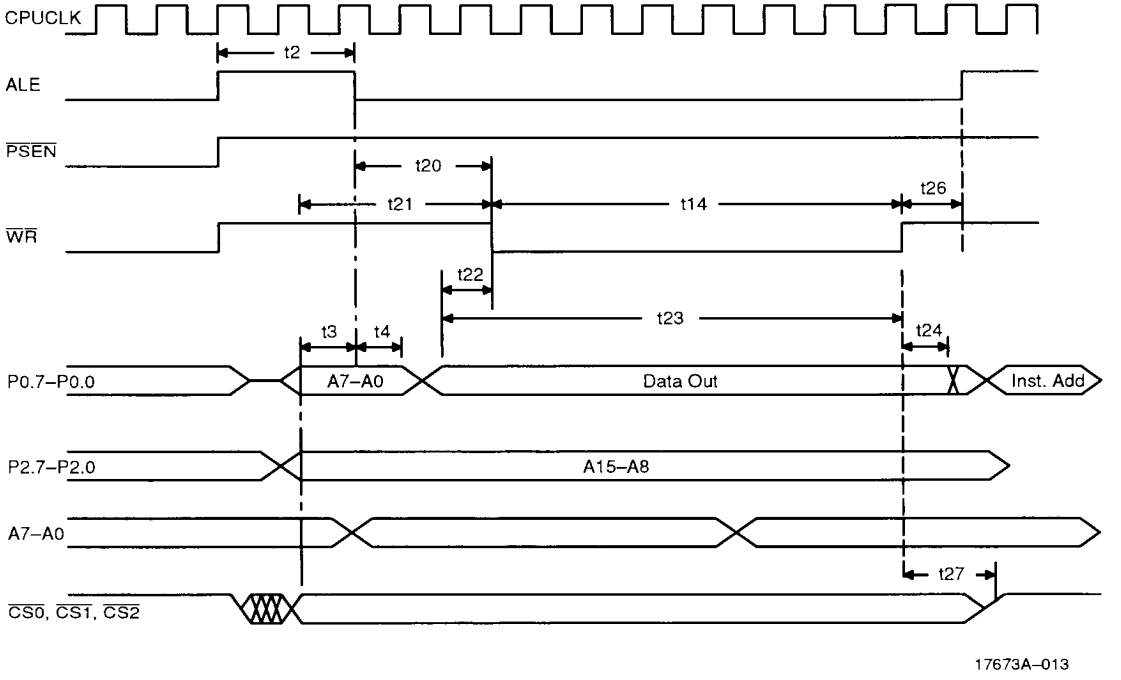


Figure 20. Microcontroller External Data Memory Write Cycle

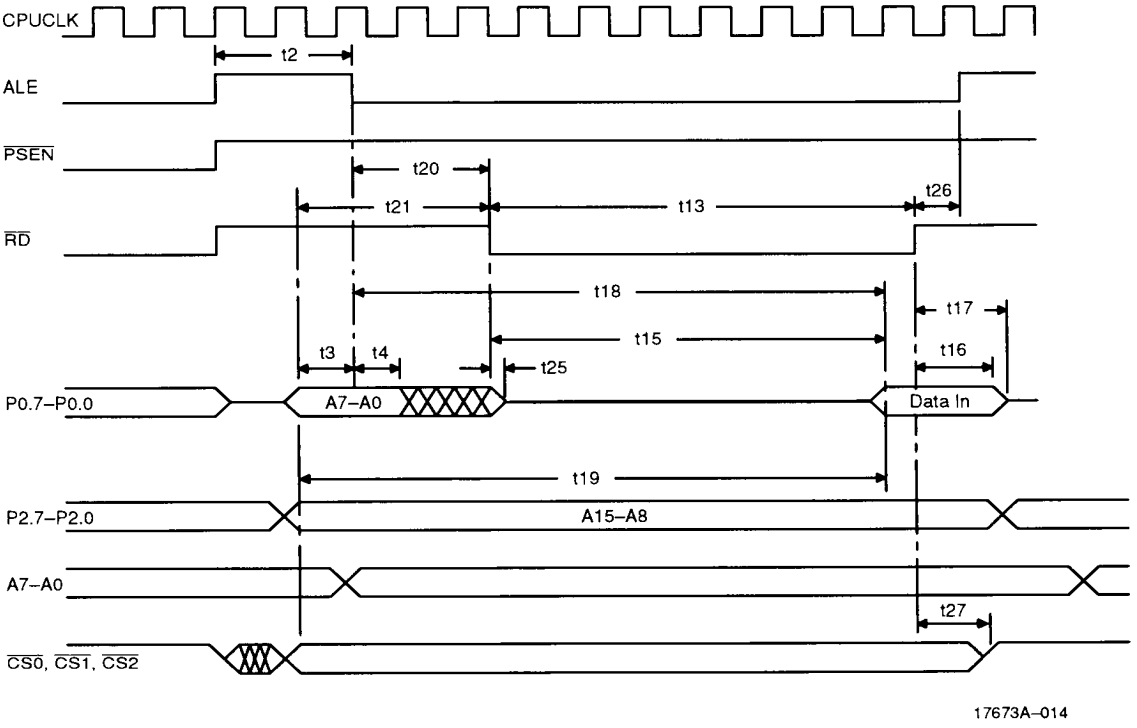


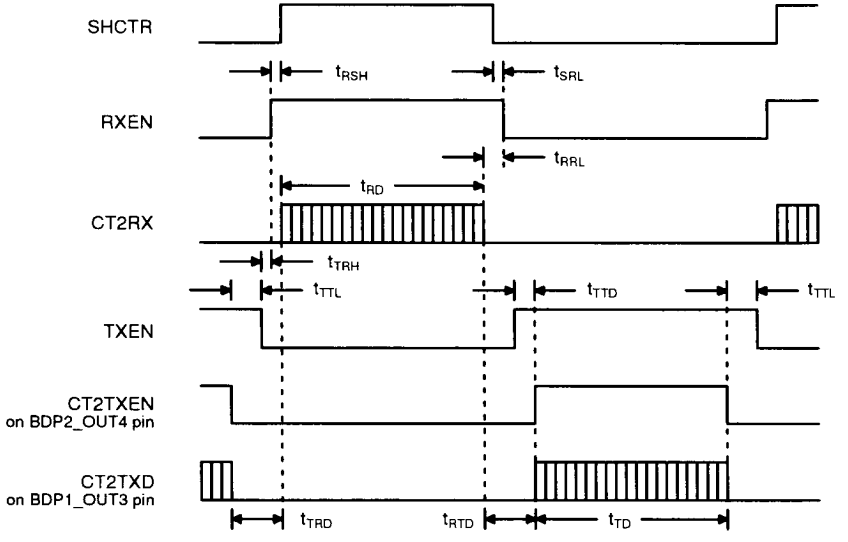
Figure 21. Microcontroller External Data Memory Read Cycle

CT2 FORMATTER

The waveform shows timing of the TXEN, RXEN, and SHCTR signals, relative to the receive and transmit data, assuming measured modem delay is zero. Values are tabulated for the various multiplexes in the *RF Interface Control Signal Switching Characteristics* table shown below. One bit period is nominally 13.88 µs (1/72 kHz).

RF Interface Control Signal Switching Characteristics
t_{MDM} = modem delay measurement adjustment

Parameter	Parameter Description	MUX1.2, MUX2 (typical)	MUX1.4 (typical)	MUX3 (typical)
t_{TTD}	TXEN High to Valid Transmit Data	4.3 µs	4.3 µs	4.3 µs
t_{TTL}	End of Data to TXEN Low	42.5 µs	42.5 µs	42.5 µs
t_{RTD}	Receive Data to Transmit Data	CFP: 6.5 – t_{MDM} bits CPP: 5.5 – t_{MDM} bits	CFP: 4.5 – t_{MDM} bits CPP: 3.5 – t_{MDM} bits	CFP: 6.5 – t_{MDM} bits CPP: 5.5 – t_{MDM} bits
t_{TRD}	Transmit Data to Receive Data	CFP: 5.5 + t_{MDM} bits CPP: 6.5 + t_{MDM} bits	CFP: 3.5 + t_{MDM} bits CPP: 4.5 + t_{MDM} bits	CFP: 5.5 + t_{MDM} bits CPP: 6.5 + t_{MDM} bits
t_{TD}	Transmit Data Length	66 bits	68 bits	CPP: 720 bits
t_{RD}	Receive Data Length	66 bits	68 bits	CFP: 144 bits CPP: N/A
t_{TRH}	TXEN Low to RXEN High	6.9 µs	6.9 µs	6.9 µs
t_{RSH}	RXEN High to SHCTR High	33.9 µs	6.11 µs	20.0 µs
t_{SRL}	SHCTR Low to RXEN Low	6.9 µs	6.9 µs	6.9 µs
t_{RRL}	End of Valid Data to RXEN Low	6.9 µs	6.9 µs	N/A



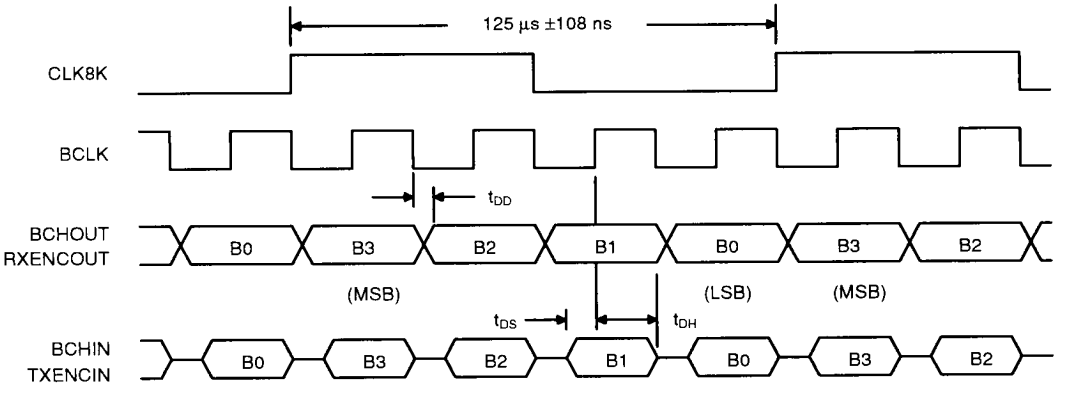
17673A–015

Figure 22. RF Interface Control Signal Timing

B-Channel Port

Switching Characteristics (all units in nanoseconds)

Parameter	Parameter Description	Min	Max
t_{DD}	BCLK Low to Output Data Valid	0	100
t_{DS}	Input Data Setup to BCLK High	150	
t_{DH}	Input Data Hold after BCLK High	0	



17673A–016

Figure 23. B-Channel Port Timing

Serial Port and A-law PCM Port

Switching Characteristics (all units in nanoseconds)

Parameter	Parameter Description	Min	Max
t_d	SCLK Low to Output Data Valid	0	100
t_{su}	Input Data Setup to Active SCLK Edge	150	
t_h	Input Data Hold after Active SCLK Edge	0	

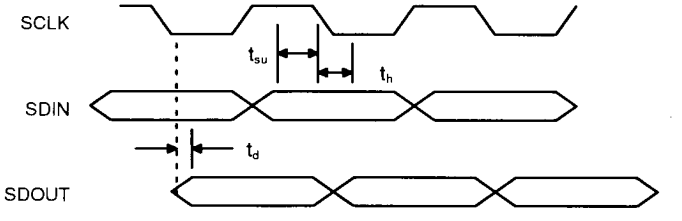


Figure 24. Serial Port Timing (SIOMODE[2] = 0)

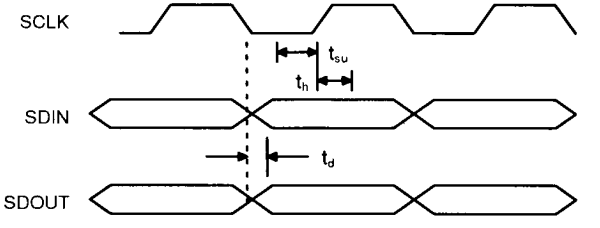


Figure 25. Serial Port Timing (SIOMODE[2] = 1)

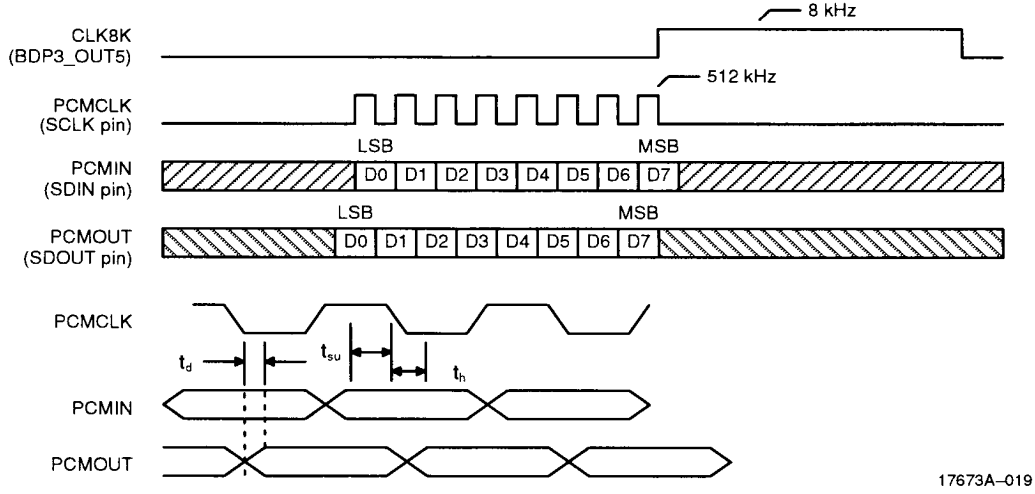


Figure 26. A-Law PCM Port Timing

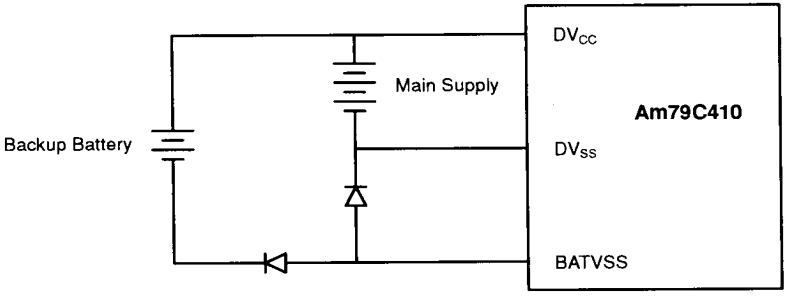
Battery Backup

BATVSS Pin DC Characteristics

Parameter	Parameter Description	Min	Max
V_{op}	Battery Backup Minimum Operation Voltage, DV_{CC}–BATVSS for $DV_{CC} - DV_{SS} < 2.7$ V	1.8 V	
V_{abs}	Absolute Maximum Rating, BATVSS–DV_{SS}		0.3 V

Battery Level Detector

Battery Level Detector absolute error: ±5% maximum.



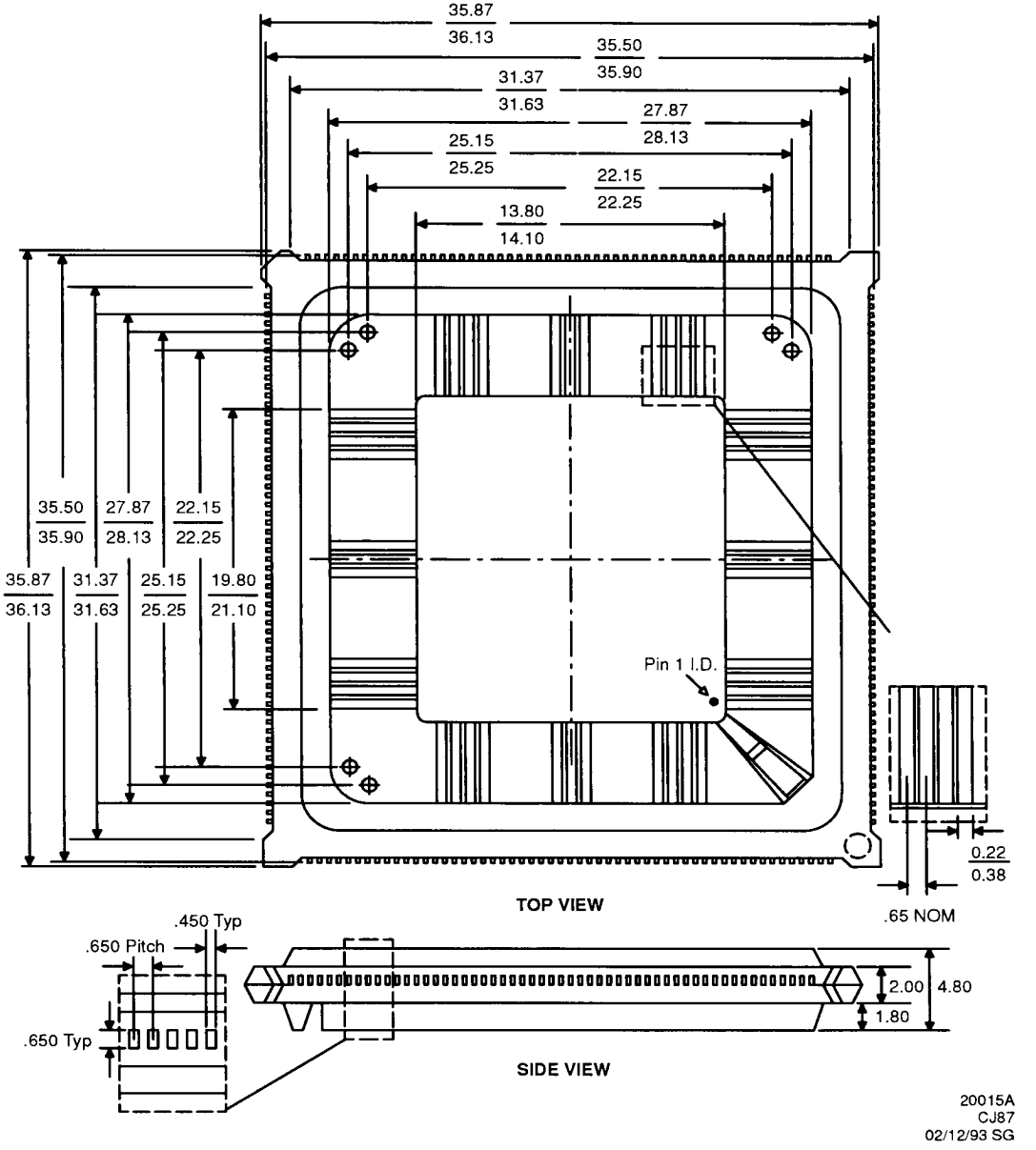
17673A–020

Figure 27. Battery Level Detector

PHYSICAL DIMENSIONS

PQR 100—Plastic Quad Flat Pack with Molded Carrier Ring

(All measurements in millimeters)



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