Am79C31

Digital Exchange Controller (DEC)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Digital customer access for ISDN.
- Compatible with CCITT I-Series recommendations at 'S' and 'T' reference points.
- Applications for PABX Line Cards.
- ISDN CCITT 'S' reference interface:
  - —Four-wire transceiver operation.
  - —Supports point-to-point and point-to-multipoint configurations.
  - —192 kbps bit rate—64 kbps: voice/data B1-channel.
    - —64 kbps: voice/data B2-channel
    - —16 kbps: control/data D-channel.
    - —48 kbps: framing and maintenance
- IDI for control of the Am79C33
- Dual PCM highway:
  - —Carries both B- and D-channels as programmable options.
  - —Compatible with the SLAC PCM port.
  - —Individual B- and D-channel time slot assignments.
- D-channel controller:
  - —Level 1 physical layer.
  - —Level 2 handling—Zero insertion/deletion.
    - —Flag generation/detection.
    - —CRC generation/checking.
  - —32 byte transmit and 32 byte receive FIFOs
- Parallel microprocessor interrupt-driven interface
- Test/maintenance loopbacks
- CMOS technology with single +5 V supply, TTL compatible

GENERAL DESCRIPTION

The Am79C31 Digital Exchange Controller (DEC) provides the exchange termination functions for one ISDN subscriber line. The Am79C31 is compatible with the CCITT I-Series recommendations at the 'S' reference point. The user of this device may design PABX line cards which conform to the CCITT ISDN standards. The 'S' reference point interface provided on the Am79C31 is fully programmable via a microprocessor interface. A dual PCM interface is provided on the Am79C31 to gain direct access to the PABX line card backplane.

The Am79C31 'S' reference point interface supports the 192 kbps four-wire path to the subscriber TEs operating in either the point-to-point or point-to-multipoint configurations. The Am79C31 separates and combines the 192 kbps data stream into separate D- and B-channels, and inserts or extracts these channels on or off the PCM highway in the programmed time slot.

The D-channel can be processed (level 1 and partial level 2) in the Am79C31 at 16 kbps or 64 kbps and then passed to the external microprocessor for higher level processing. The D-channel can also be passed over the dual PCM highway with the B-channel data for centralized handling (the DLC processor in the Am79C31 is bypassed using this option). The microprocessor can program the Am79C31 to route the D- and B-channels as desired and maintains supervision by interrogating status and interrupt registers contained within the Am79C31.

The Am79C31 dual PCM interface has independent control for the transmit and receive paths. The frame sync. signal identifies the beginning of the frame and all time slots are referenced to it. The PCM interface will operate up to 8.192 Mbps, thus allowing up to 128 possible time slots at 64 kbps without blocking. During each frame two 64 kbps B-channels (8-bit time slots) and one 16 kbps or 64 kbps D-channel (2- or 8-bit time slots) may be transferred to/from the PCM highway. Time slot assignment and PCM highway selection are under control of the microprocessor.

To aid in maintenance of the system, several facilities are provided. Loopback is available at the 'S' and PCM interfaces. The B-channels may be monitored via the micorprocessor interface.

Multiple Am79C31s under the control of one microprocessor can be contained on a single PABX line card. Thus multiple ISDN 'S' interface lines can be terminated on the one PABX line card with a microprocessor controlling the time slot assignments, activation and maintenance functions.

GENERAL DESCRIPTION

The IDPC integrates several major components of an ISDN terminal or workstation in one flexible, cost-effective device.

The IDPC also provides a reduced-cost, high-performance solution for many existing non-ISDN telecommunications applications such as IBM Systems Network Architecture (SNA), AT&T Digital Multiplexed Interface (DMI), and X.25 terminals and workstations.

As shown in the Block Diagram, the IDPC is composed of several major functions: the Data Link Controller (DLC), the Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Microprocessor Interface (MPI), and the Dual-Port Memory Controller (DPMC).

Data Link Controller (DLC)

The DLC is a high-speed synchronous serial port supporting bit-oriented protocols such as HDLC, SDLC, LAPB, LAPD and DMI. The DLC supports CRC-CCITT recognition and generation, bit insertion and deletion, address recognition, abort recognition and detection, bit residue, and flag recognition and generation.

The DLC serial bus port can work in either a multiplexed or a non-multiplexed mode. In the non-multiplexed mode, the DLC performs like a standard serial communications controller supporting full-duplex transfers up to 2.048 Mbits/sec.

In the multiplexed mode, the DLC works with the serial bus port on the Am79C30 Digital Subscriber Controller (DSC) or Am79C32 ISDN Data Controller (IDC). The DLC provides access to any of the 64 Kbit/sec time slots in the Am79C30/Am79C32's 192 Kbit/sec serial bus. The DSC or IDC can then assign the time slots to any of the 64 Kbit/sec channels on the 2B + D 'S' interface. The DLC can support logical connection to any of 31 time slots on the serial bus port.

The DLC supports data transfers via DMA, interrupts, or polled I/O. The DLC transmitter contains a 16-byte FIFO and the receiver contains a 32-byte FIFO to minimize interrupt latency and frequency of interrupts. The DLC provides both local loopback and a remote echo to support system testing.

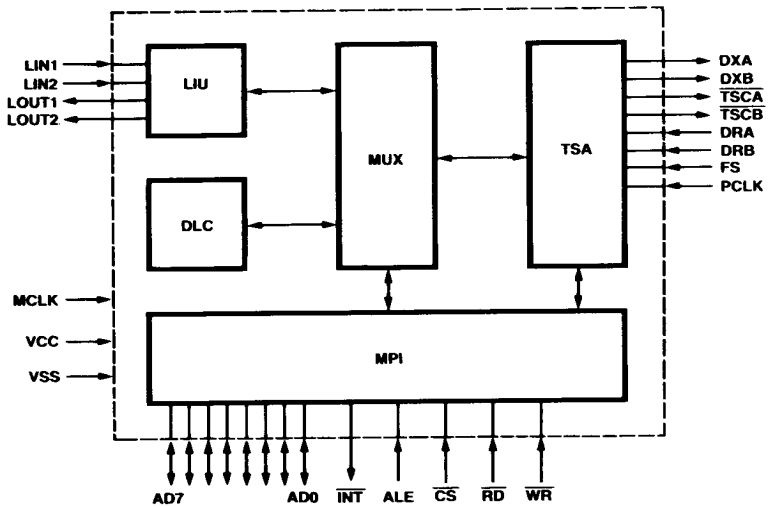
Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART contains a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART can operate full-duplex at speeds up to 56 Kbit/sec using the internal programmable baud rate generator or via external clock sources.

The USART supports break recognition and generation, parity generation/checking, and special character recognition. The USART supports 1, 1.5, or 2 stop bits. Modem control/handshake lines are provided for RTS, CTS, DSR, and DTR. For testing purposes, the USART contains a local loopback mode and "stick" parity.

Dual-Port Memory Controller (DPMC)

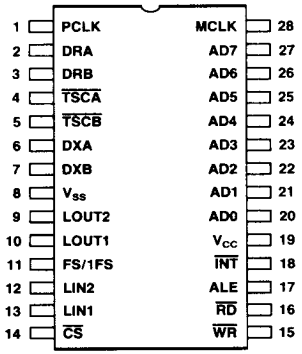
The DPMC provides an on-board bus arbitration/controller to support the use of shared memory in multiprocessing applications such as intelligent communications controllers. The DPMC allows the implementation of shared memory using inexpensive static RAM. Interprocessor interrupts can be generated under software control.



Am79C31 DEC Block Diagram

LIU = Line Interface Unit
DLC = Data Link Controller
MUX = Multiplexer
TSA = Time Slot Assigner
MPI = Microprocessor Interface

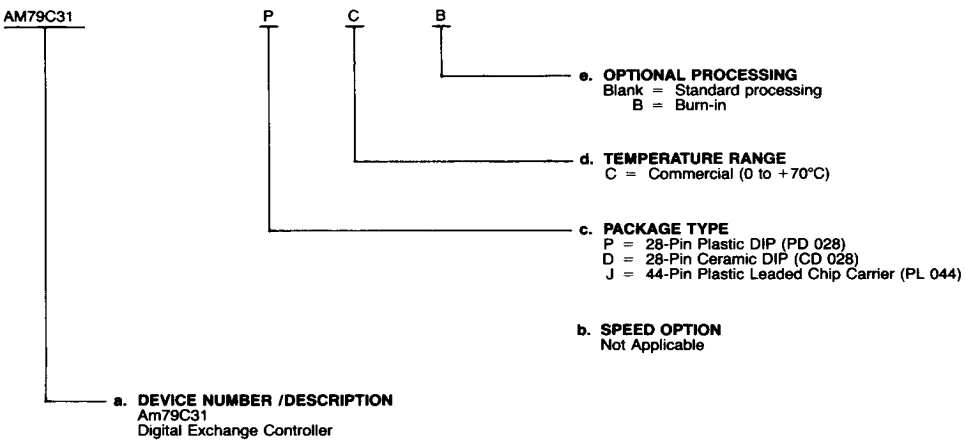
CONNECTION DIAGRAM



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is form
by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C31	PC, PCB, DC, DCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supporte
in volume for this device. Consult the local AMD sales office t
confirm availability of specific valid combinations, to check c
newly released combinations, and to obtain additional data c
AMD's standard military grade products.