www.DataSheet4U.com

Rockwell

R6500/1
One-Chip Microcomputer

SECTION 1
INTRODUCTION

SUMMARY

The Rockwell R6500/1 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-channel silicon gate MOS process. The R6500/1 complements an established and growing line of R6500 products and has a wide range of microcomputer applications.

The R6500/1 consists of an R6502 Central Processing Unit (CPU), 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R6500/1 a leading candidate for microcomputer applications.

To facilitate system and program development for the R6500/1, Rockwell has developed a 64-pin R6500/1E Emulator device, as well as a pin-compatible R6500/1EB Backpack Emulator device. For more information, refer to the data sheets for the R6500/1E (Order No. D51S) and the R6500/1EB (Order No. D60).

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer Systems Programming Manual (Document Order No. 202).

ORDERING INFORMATION

Part Number:
R6500/1

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

Frequency
No Letter = 1 MHz
A = 2 MHz

FEATURES

- Single-chip microcomputer
- R6502 software compatible
- Eight-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- Thirteen addressing modes
- 1 or 2 MHz clock operation, with the following options:
  — External single clock input
  — RC time base input
  — Crystal time base input
- Single +5V power supply
- 500 mw operating power
- Separate power pin for RAM with standby power only 10% of operating power
- 2K x 8 ROM on chip
- 64 x 8 RAM on chip
- 40-pin DIP and 44-pin PLCC
- 64-pin R6500/1E Emulator part available, with 40 signals identical to production part
- 40-pin R6500/1EB Backback Emulator part available, pin compatible with an R6500/1
- Pipeline architecture
- 32 bidirectional TTL compatible I/O lines
  — 1 positive edge sensitive I/O lines
  — 1 negative edge sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit timer/counter
- Four timer/counter modes
  — Internal timer
  — Pulse generator
  — Event counter
  — Pulse width measurement
- Three maskable interrupts
  — 1 counter overflow
  — 2 I/O edge detect
- NMI and Reset interrupts

www.DataSheet4U.com

www.DataSheet4U.com

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R6500/1 single chip microcomputer. Figure 2-1 is the Interface Diagram for the R6500/1. Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R6500/1.

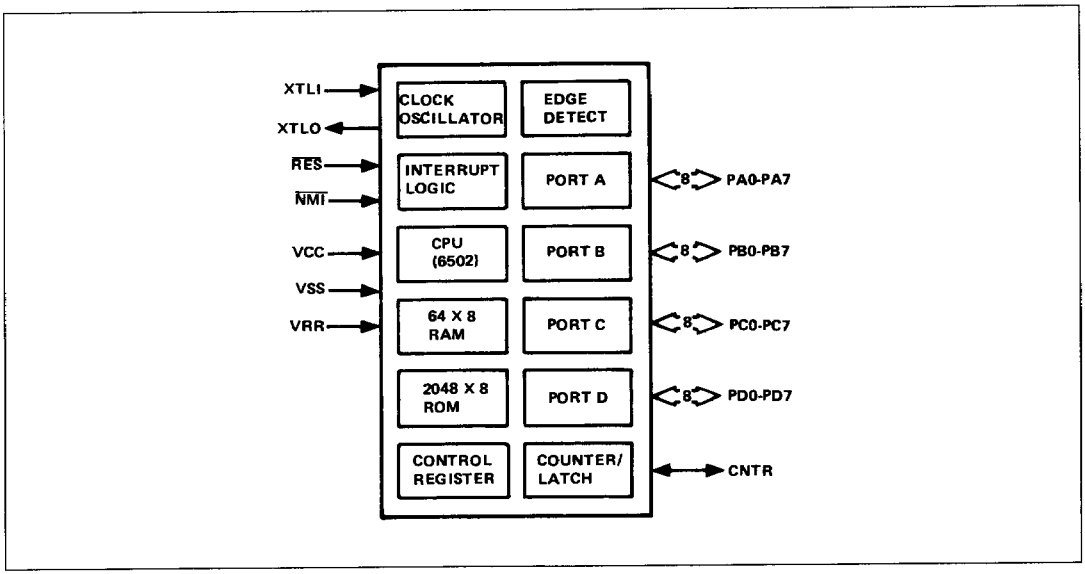


Figure 2-1. R6500/1 Interface Diagram

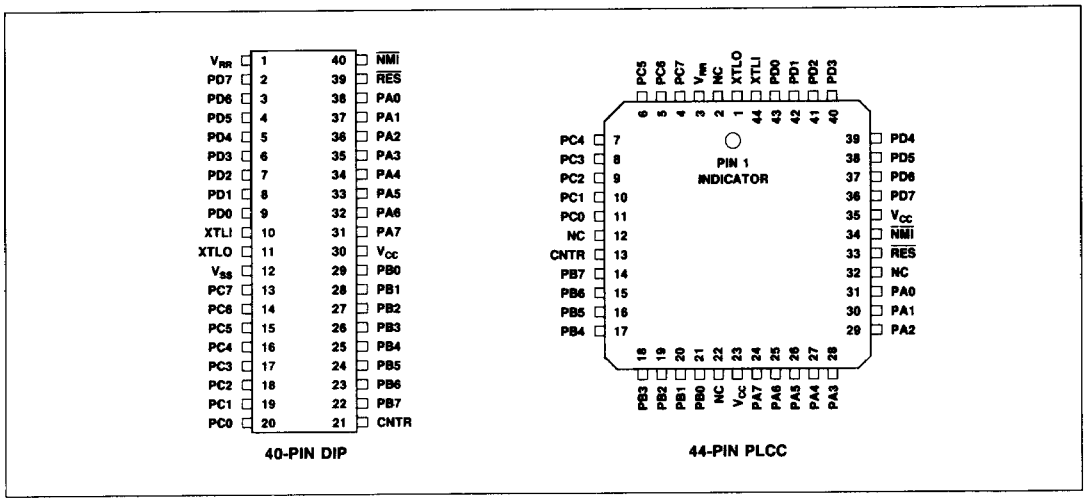


Figure 2-2. R6500/1 Pin Assignments

www.DataSheet4U.com

www.DataSheet4U.com

Table 2-1. R6500/1 Pin Description

Signal Name	I/O	Description
VCC		**Power.** Main power supply +5V.
VRR		**RAM Retention Power.** Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data +5V.
VSS		**Ground.** Signal and power ground (0V).
XTLI	I	**Crystal In.** Crystal or clock input for internal clock oscillator.
XTLO	O	**Crystal Out.** Crystal output from internal clock oscillator.
$\overline{RES}$	I	**Reset.** The Reset input is used to initialize the R6500/1. The signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized (see Section 5).
$\overline{NMI}$	I	**Non-Maskable Interrupt.** A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	I/O I/O I/O I/O	**Port A.** General purpose I/O Port A. **Port B.** General purpose I/O Port B. **Port C.** General purpose I/O Port C. **Port D.** General purpose I/O Port D. Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and an optional passive pull-up to VCC. The two lower bits of the PA port (PA0-PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	I/O	**Counter I/O.** This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes. It consists of an active transistor to VSS and an optional passive pull-up to VCC.

www.DataSheet4U.com

www.DataSheet4U.com

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R6500/1. A block diagram of the R6500/1 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address — the sum of the program counter contents and the and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions or the interrupt lines $\overline{NMI}$ and $\overline{IRQ}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers

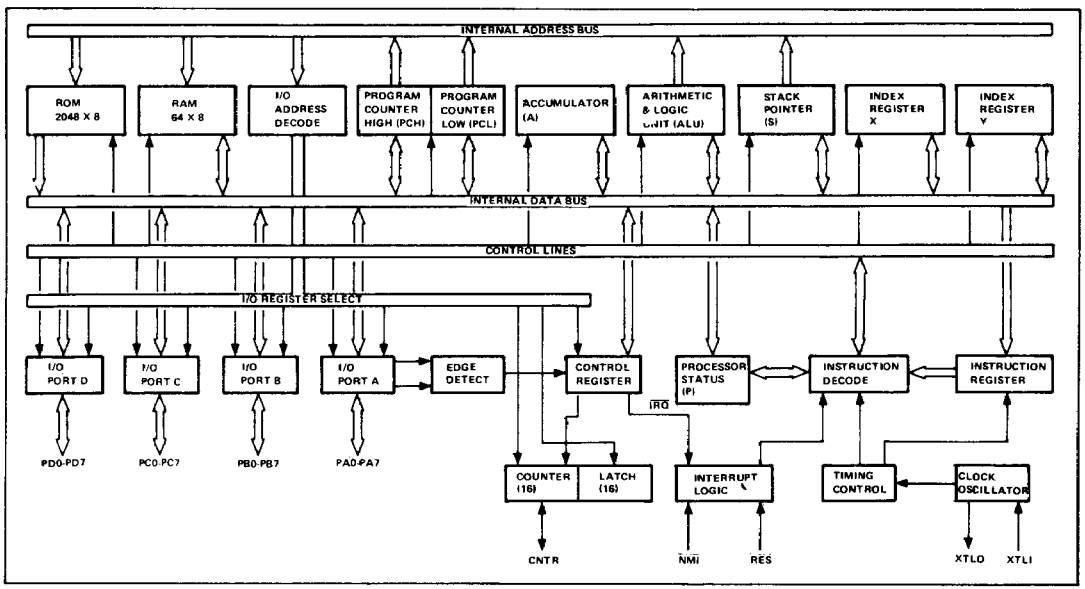


Figure 3-1. R6500/1 Block Diagram

www.DataSheet4U.com

www.DataSheet4U.com

(except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 4 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 TIMING CONTROLS

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.8 INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.

3.9 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal or clock. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 ($\phi 2$) frequency is one-half the external reference frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-2.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value, 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

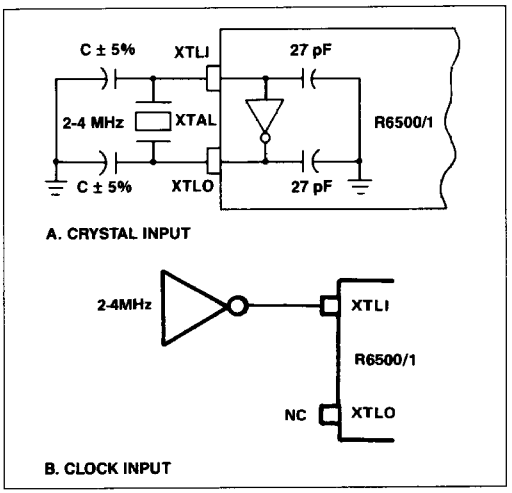


Figure 3-2. Clock Oscillator Input Options

3.10 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-3, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction

www.DataSheet4U.com

www.DataSheet4U.com

set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.10.1 CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.10.2 ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.10.3 INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt (CLI) instruction, the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (providing the Interrupt Disable Bit was cleared prior to the interrupt). The Interrupt Disable Bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

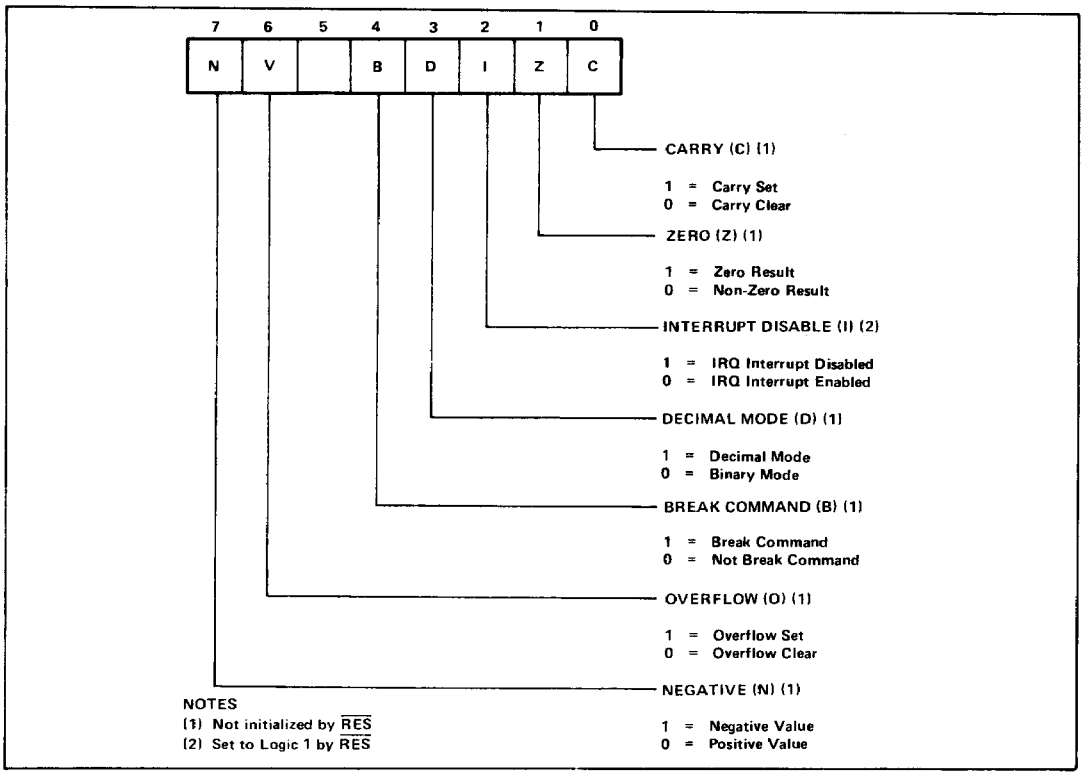


Figure 3-3. Processor Status Register

www.DataSheet4U.com

www.DataSheet4U.com

3.10.4 DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to R6500/1. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.10.5 BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.10.6 OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. Durliing a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.10.7 NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation s positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.11 2K × 8 ROM

The R6500/1 2048 byte × 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

3.12 64 × 8 RAM

The 64 byte × 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. A standby power pin, V_{RR} allows RAM memory to be maintained on 10% of the operating power. In the event that VCC power is lost and execution stops, this standby power retains RAM data until execution resumes.

In order to take advantage of zero page addressing capabilities, the R6500/1 RAM is assigned page zero memory address 0 to 03F.

3.13 CONTROL REGISTER

The Control Register (CR), shown in Figure 3-4, is located at address 08F. The CR contains five control signals and three status signals.

The control signals are summarized in Table 3-1. The control signals are set to logic 1 by writing logic 1 into the respective bit positions and cleared to logic 0 either by writing logic 0 into the respective bit position or by the occurrence of a $\overline{RES}$ signal.

Table 3-1. CR Control Signals

Control Signal Name	Bit Number
Counter Mode Control 0 (CMC0)	0
Counter Mode Control 1 (CMC1)	1
PA1 Interrupt Enabled (A1IE)	2
PA0 Interrupt Enabled (A0IE)	3
Counter Interrupt Enabled (CIE)	4

The three status signals are summarized in Table 3-2.

www.DataSheet4U.com

www.DataSheet4U.com

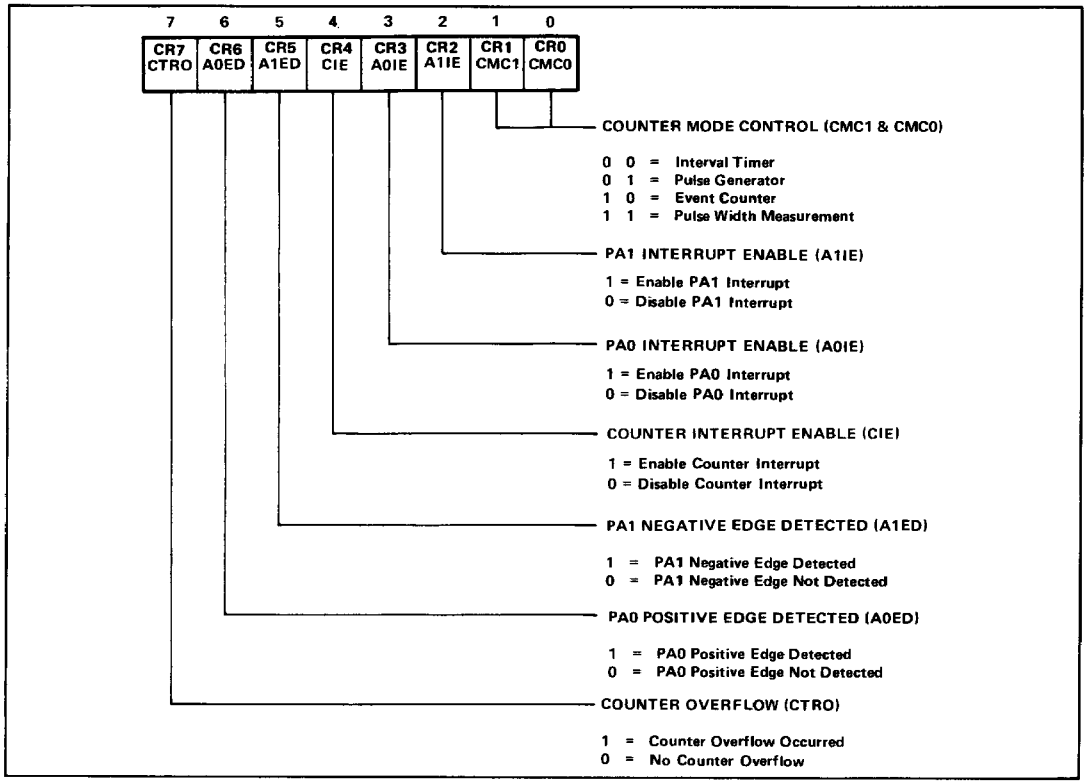


Figure 3-4. Control Register (CR)

Table 3-2. CR Status Signals

Status Signal Name	Bit Number
PA1 Negative Edge Detected (A1ED)	5
PA0 Positive Edge Detected (A0ED)	6
Counter Overflow (CTRO)	7

The status signals are read-only information. The status bits are set to logic 1 by hardware monitoring logic and cleared to logic 0 by the occurrence of $\overline{RES}$ signal or by specific address commands. Each of these signals is described in the following sections.

3.13.1 COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are summarized in Table 3-3.

These modes are controlled by writing the appropriate bit values into the Counter Mode Control bits.

Table 3-3. Counter Mode Control Selection

CMC1 (Bit 1)	CMC0 (Bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generator
1	0	Event Counter
1	1	Pulse Width Measurement

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated or if the user program stores logic 0 into Bits 0 and 1 of the Control Register. A complete description of each of the Counter modes is given in Section 3.14.1.

3.13.2 PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable Bit (CR2) is set to logic 1, an $\overline{IRQ}$ interrupt request signal will be generated when the PA1 Negative Edge Detected Bit (CR5) is set.

www.DataSheet4U.com

www.DataSheet4U.com

3.13.3 PA0 INTERRUPT ENABLE BIT (A0IE)

If the PA0 Interrupt Enable Bit (CR3) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when the PA0 Positive Edge Detected Bit (CR6) is set.

3.13.4 COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (CR4) is set to logic 1, the $\overline{IRQ}$ interrupt request signal will be generated when Counter Overflow (CR7) is set.

3.13.5 PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected Bit (CR5) is set to logic 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 08A.

The edge detecting circuitry is active when PA1 is used either as an input or as an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a logical 1 to 0 transition.

When PA1 is used as an input and the negative edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and when the PA1 Negative Edge Detected $\overline{IRQ}$ processing is completed.

3.13.6 PA0 POSTIIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected Bit (CR6) is set to logic 1 whenever a positive (rising) edge is detected on PA0. The bit is cleared to logic 0 by $\overline{RES}$ or by writing to address 089.

The edge detecting circuitry is active when PA0 is used either as an input or as an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a logical 0 to 1 transition.

When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected $\overline{IRQ}$ processing.

3.13.7 COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow Bit (CR7) is set to logic 1 whenever a counter overflow occurs in any of the four counter operating modes. Overflow occurs when the counter is decremented one count from 0000. This bit is cleared to logic 0 by $\overline{RES}$ or by reading from address 087 or writing to address 088.

This bit should be cleared by the user program upon initialization and upon completion of Counter Overflow $\overline{IRQ}$ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address 086 and the Lower Count (LC) in address 087 are reset to the values contained in the Upper Latch (UL) in address 084 and in the Lower Latch (LL) in address 085, respectively. Therefore, it is important to load the Lower Latch value prior to executing the Write to Upper Latch and Transfer Latch to Counter (address 088) in order to prevent an unpredicted reoccurrence of Counter Overflow and, if enabled, an $\overline{IRQ}$ interrupt request.

3.14 COUNTER/LATCH

The Counter/Latch consists of a 16-bit Counter and a 16-bit Latch. The Counter resides in two 8-bit registers: address 086 contains the Upper Count value (bits 8-15 of the Counter) and address 087 contains the Lower Count value (bits 0-7 of the Counter). The Counter contains the count of either ø2 clock periods or external events depending on which counter mode is selected in the Control Register (Section 3.13.1).

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address 084 contains the Upper Latch value (bits 8-15 of the Latch) and address 085 contains the Lower Latch value (bits 0-7 of the Latch). The 16-bit Latch can hold values from 0 to 65535.

The Latch registers can be loaded at any time by executing a write to the Upper Latch Address (084) and the Lower Latch Address (085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch can be loaded independently; it is not required to load both registers at the same time or sequentially. The Upper Latch can also be loaded by writing to address 088.

The Counter can be initialized at any time by writing to address 088. The contents of the Accumulator will be copied into the Upper Latch before the value in the Upper Latch is transferred to the Upper Counter.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0000, the next Counter value will be the Latch value, not FFFF.

Whenever the Counter overflows, the Counter Overflow Bit (CR7) is set to logic 1. This bit is cleared whenever the lower eight bits of the counter are read from address 087 or by writing to address 088.

3.14.1 COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

Mode	CMC1	CMC0
Interval Timer	0	0
Pulse Generator	0	1
Event Counter	1	0
Pulse Width Measurement	1	1

www.DataSheet4U.com

www.DataSheet4U.com

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).
2. When a write operation is performed to the Load Upper Latch and Transfer Latch to counter address (088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the ϕ2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535ms at the 1 MHz ø2 clock rate or 0.5μs to 32.768ms at the 2 MHz ϕ2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When the Counter decrements from 0000, the Counter Overflow (CR7) is set to logic 1 at the next ø2 clock pulse. If the Counter Interrupt enable bit (CR4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Overflow bit in the Control Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Overflow.

While the timer is operating in the Interval Timer Mode, the Counter Out/Event line is held in the high (output disabled) state.

A timing diagram of the Interval Timer Mode is shown in Figure 3-5.

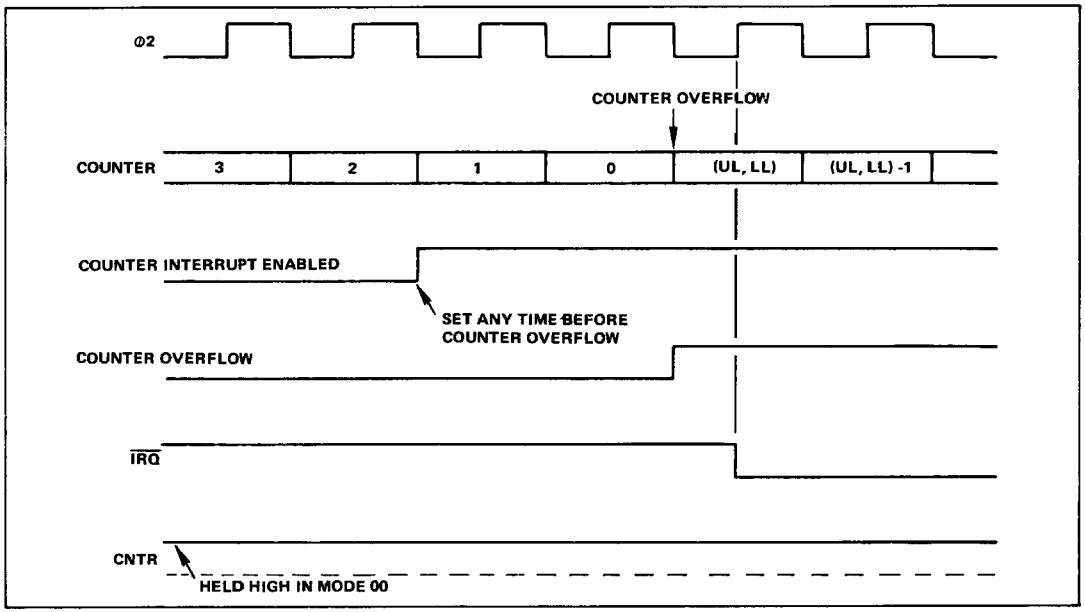


Figure 3-5. Interval Timer (Mode 0) Timing Diagram

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the Counter Out/Event In line (CNTR) operates as a Counter Out. The CNTR line toggles from low to high or from high to low whenever a Counter Overflow occurs, or a write is performed to address 088.

Either a symmetric or asymmetric output waveform can be output on the CNTR line in this mode. The CNTR output is initialized high by a $\overline{RES}$ since the Interval Timer mode is established by $\overline{RES}$.

A one-shot waveform can be easily generated by changing from Mode 1 Pulse Generator to Mode 0 (Interval Timer) after only one occurrence of the output toggle condition.

www.DataSheet4U.com

www.DataSheet4U.com

Event Counter Mode (Mode 2)

In this mode the CNTR line is used as an Event Counter. The Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to logic 1 if the overflow occurs.

Figure 3-6 is a timing diagram of the Event Counter Mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event In capacity. The Counter decrements by one count at the ϕ2 clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high (>2.0V) state.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 3-7.

3.15 INPUT/OUTPUT PORTS

The R6500/1 provides four 8-bit Input/Output (I/O) ports (PA, PB, PC, PD). These 32 I/O lines are completely bidirectional. All lines may be used either for input or output in any combination; that is, there are no line grouping or port association restrictions.

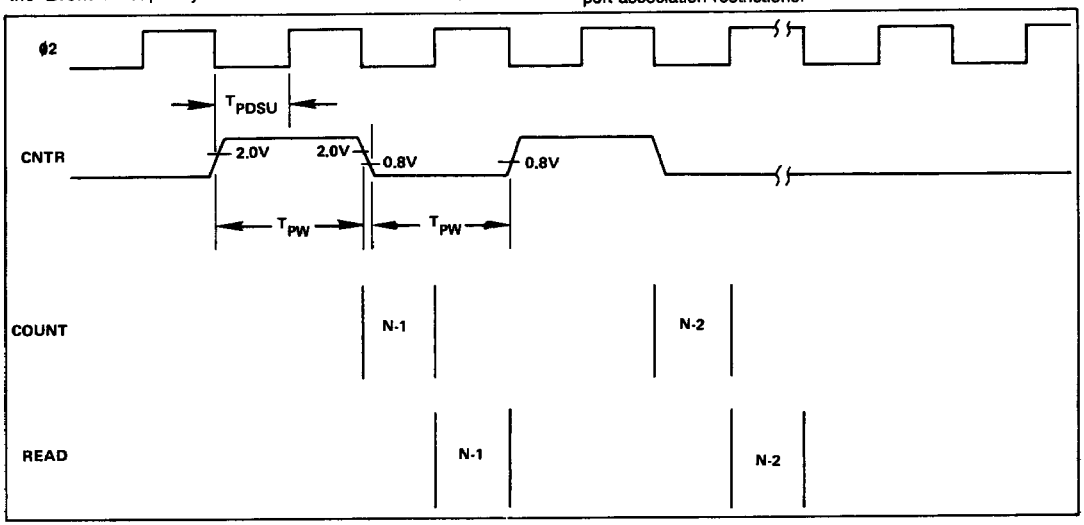


Figure 3-6. Event Counter Mode (Mode 2)

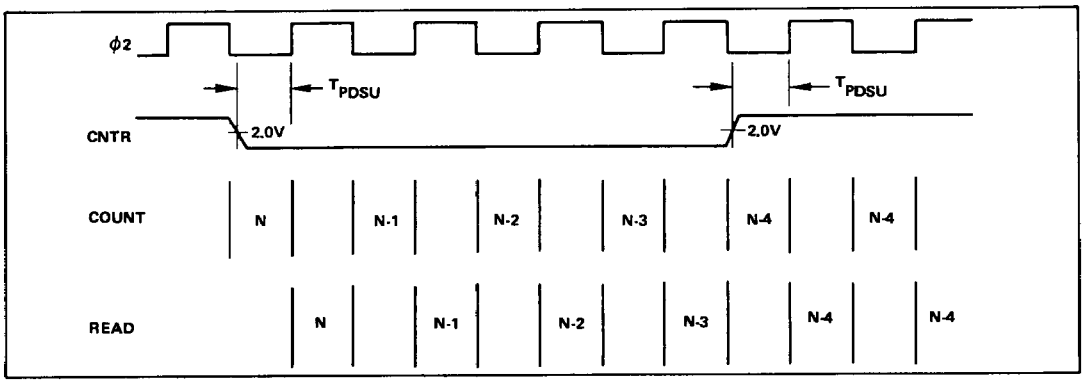


Figure 3-7. Pulse Width Measurement (Mode 3)

www.DataSheet4U.com

www.DataSheet4U.com

The direction of the 32 I/O lines are controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3-4.

Table 3-4. I/O Port Addresses

Port	Address
A	080
B	081
C	082
D	083

Figure 3-8 shows the I/O Port Timings.

3.15.1 INPUTS

Inputs are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

3.15.2 OUTPUTS

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

3.15.3 EDGE DETECTION CAPABILITY

Ports PA0 and PA1 have an edge detection capability. Figure 3-9 shows the edge detection timing.

PA0 Positive Edge Detecting Capability

In addition to its normal I/O function, PA0 will detect an asynchronous positive (rising) edge signal and set the PA0 Positive Edge Detected signal (CR6) to logic 1. The maximum rate at which this positive edge can be detected is one-half the Ø2 clock rate.

If the PA0 Interrupt Enable Bit (CR3) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA0 Positive Edge Detected signal can be cleared by writing to address 089.

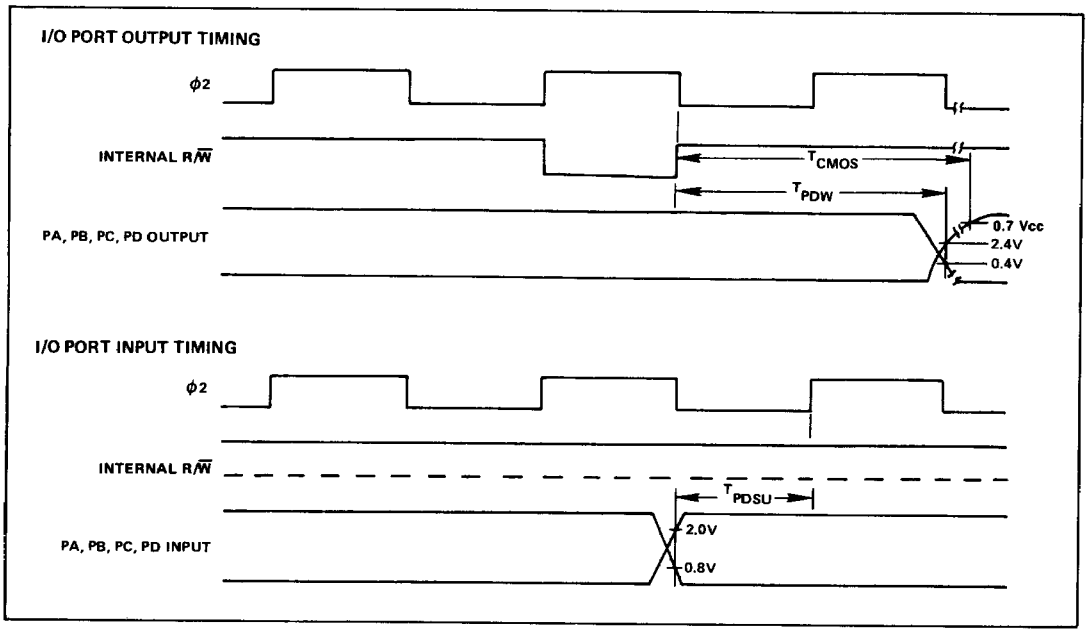


Figure 3-8. I/O Port Timing

www.DataSheet4U.com

www.DataSheet4U.com

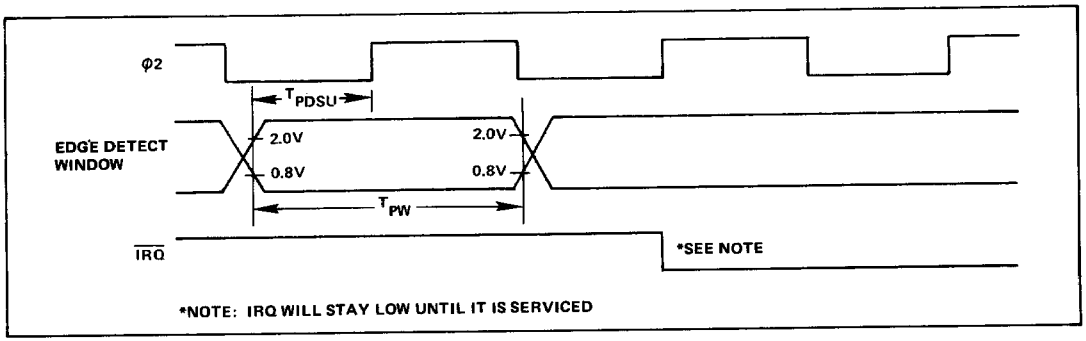


Figure 3-9. PA0 and PA1 Edge Detection Timing

PA1 Negative Edge Detecting Capability

In addition to its normal I/O function, PA1 will detect an asynchronous negative (falling) edge signal and set the PA1 Negative Edge Detected signal (CR5) to logic 1. The maximum rate at which this negative edge can be detected is one-half the Ø2 clock rate.

If the PA1 Interrupt Enable signal (CR2) is set, an $\overline{IRQ}$ interrupt request will also be generated. The PA1 Negative Edge Detected signal may be cleared by writing to address 08A.

3.16 MASK OPTIONS

An option is provided to delete the internal pull-up resistance from PA, PB, PC and/or PD ports at mask time. This option is available for 8-bit port groups only, not for individual port lines. This option may by used to aid interface with CMOS drivers, or in order to interface with external pull-up devices.

An option is also provided to delete the internal pull-up resistance on the CNTR line.

www.DataSheet4U.com

www.DataSheet4U.com

SECTION 4
$\overline{IRQ}$ INTERRUPT REQUEST GENERATION

An $\overline{IRQ}$ interrupt request can be initiated by any or all of three possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Control Register.

The first source of $\overline{IRQ}$ is Counter Overflow. The $\overline{IRQ}$ interrupt request will be driven low whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second source of $\overline{IRQ}$ is detection of a positive edge on PA0. The $\overline{IRQ}$ inerrupt request will be driven low whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third source of $\overline{IRQ}$ is detection of a negative edge on PA1. The $\overline{IRQ}$ interrupt request will be driven low whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

CAUTION

If the same data, i.e., the same RAM, counter/latch or I/O addresses, are operated on asynchronously by a normal processing routine and by an interrupt service routine, care must be taken to prevent loss of data due to the interrupt routine altering the data during update of the data by the normal processing routine. This situation can be prevented by disabling the $\overline{IRQ}$ interrupt with the SEI instruction before starting the data update in the normal processing and then enabling the interrupt with the CLI instruction upon completion of data update.

3

www.DataSheet4U.com

www.DataSheet4U.com

SECTION 5
POWER ON/OFF CONSIDERATIONS

5.1 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R6500/1 to set the Interrupt Mask Bit — bit 2 of the Processor Status Register — and initiate a reset vector fetch at address FFE and FFF to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR will be forced to the high (logic 1) state. All bits of the Control Register will be cleared to logic 0 causing the Interval Timer counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

5.2 POWER ON/OFF TIMING

After application of VCC power to the R6500/1, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after VCC reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input VCC voltage and performance of the crystal, clock, or RC network input circuit. The clock oscillator output can be monitored on XTLO (pin 11).

Figure 5-1 illustrates the power turn-on waveforms.

5.3 RAM DATA RETENTION — VRR REQUIREMENTS

For the RAM to retain data upon loss of VCC, VRR must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before VCC falls out of operating range. $\overline{RES}$ must then be held low while VCC is out of operating range and until at least eight Ø2 clock cycles after VCC is again within operating range and the internal Ø2 oscillator is stabilzed. VRR must remain within VCC operation range during normal R6500/1 operation. When VCC is out of operating range, VRR must remain within the VRR retention range in order to retain data. Figure 5-2 shows typical waveforms.

5.4 RAM DATA RETENTION OPERATION

The requirement for R6500/1 RAM data retention and restart operation is application dependent. If R6500/1 RAM data retention is not required during loss of VCC, then VRR can be connected to the same power source as VCC. With this configuration a complete initialization of R6500/1 program variables in RAM is required upon VCC and VRR power application.

If the R6500/1 RAM is to retain data during loss of VCC, the following is required:

1. Connection of VCC and VRR to separate power supplies or to the same primary power supply with isolation diodes and battery or other backup power for VRR.
2. VCC power monitor hardware with power loss and cold/warm start indications to the R6500/1.
3 Power loss detection as well as cold and warm start initialization in the R6500/1 program.

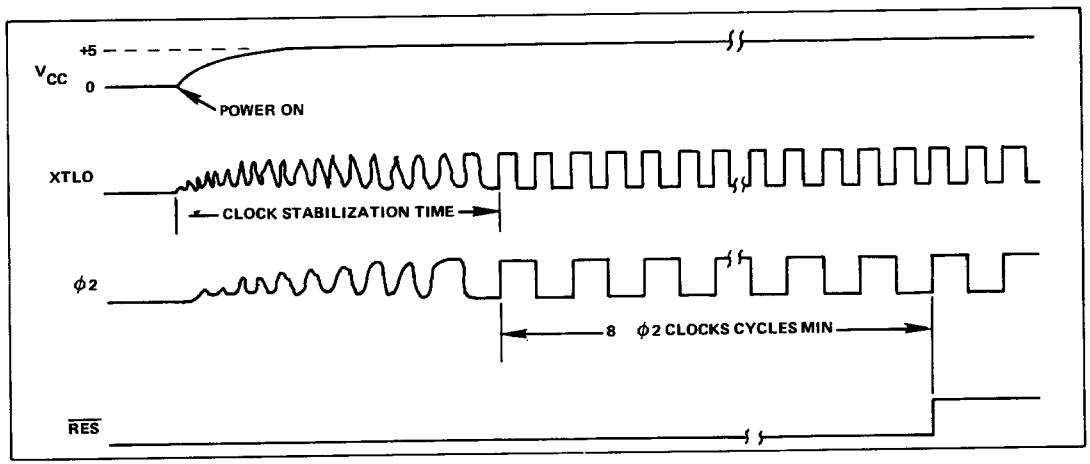
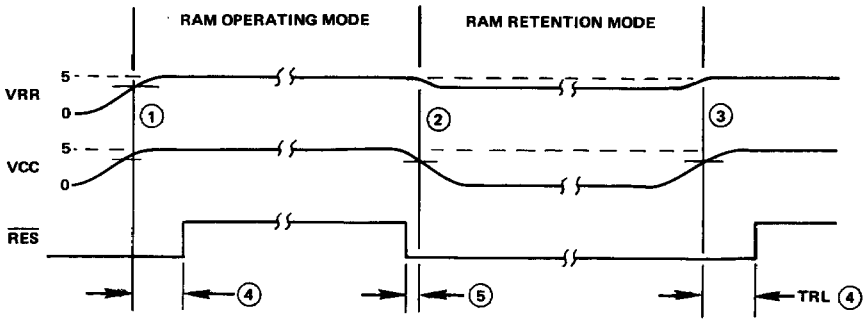


Figure 5-1. Power Turn-On Timing Detail

www.DataSheet4U.com

www.DataSheet4U.com



(1) INITIAL APPLICATION OF VCC AND VRR.

(2) LOSS OF VCC, RAM ON STANDBY POWER.

(3) REAPPLICATION OF VCC.

(4) ≥8 ϕ2 CLOCK PULSES AFTER ϕ2 OSCILLATOR STABILIZATION.

(5) ≥8 ϕ2 CLOCK PULSES.

Figure 5-2. RAM Retention Mode Timing

The power monitor hardware must sense the loss of VCC power in sufficient time to allow the R6500/1 to save required CPU register data in RAM. The power loss indication line can be connected to the $\overline{NMI}$ interrupt input in order to cause an immediate R6500/1 interrupt upon power loss detection.

The power monitor hardware should also provide an indication of cold start (initial VCC and VRR power application) or warm start (VCC power re-application while VRR is retained on backup power) provided as input on a data I/O pin.

A level indication is sufficient. The R6500/1 program can then initialize all, or partial, program variables upon initialization then jump to any other starting address as required depending upon cold/warm start condition.

Upon power loss detection, the R6500/1 should save all required CPU register data in either the stack or dedicated RAM. The stack may be preferred if dedicated RAM is not available. If the program is to restart at the interrupted address, then all CPU registers must be saved, i.e., S, P, PC, A, X, and Y. The stack pointer must be saved in a dedicated RAM address. Note that processor status P and the program counter, PC, are already saved on the stack by the NMI interrupt R6500/1 hardware processing. If the warm start can be performed at a specific address, then the saving of the register data at power loss detection may not be required. Figure 5-3 shows top level flowcharts of typical power down and power-up processing.

www.DataSheet4U.com

www.DataSheet4U.com

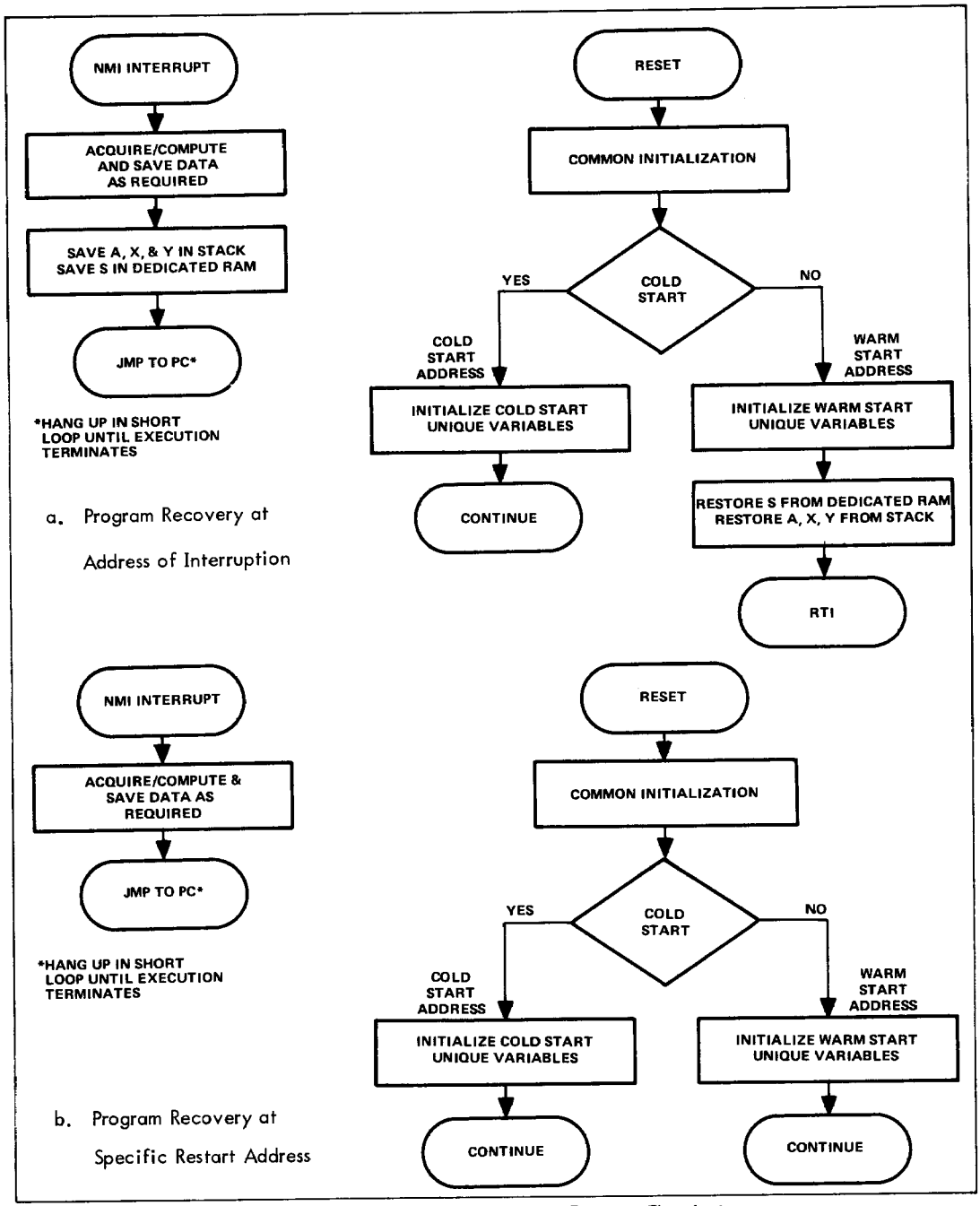
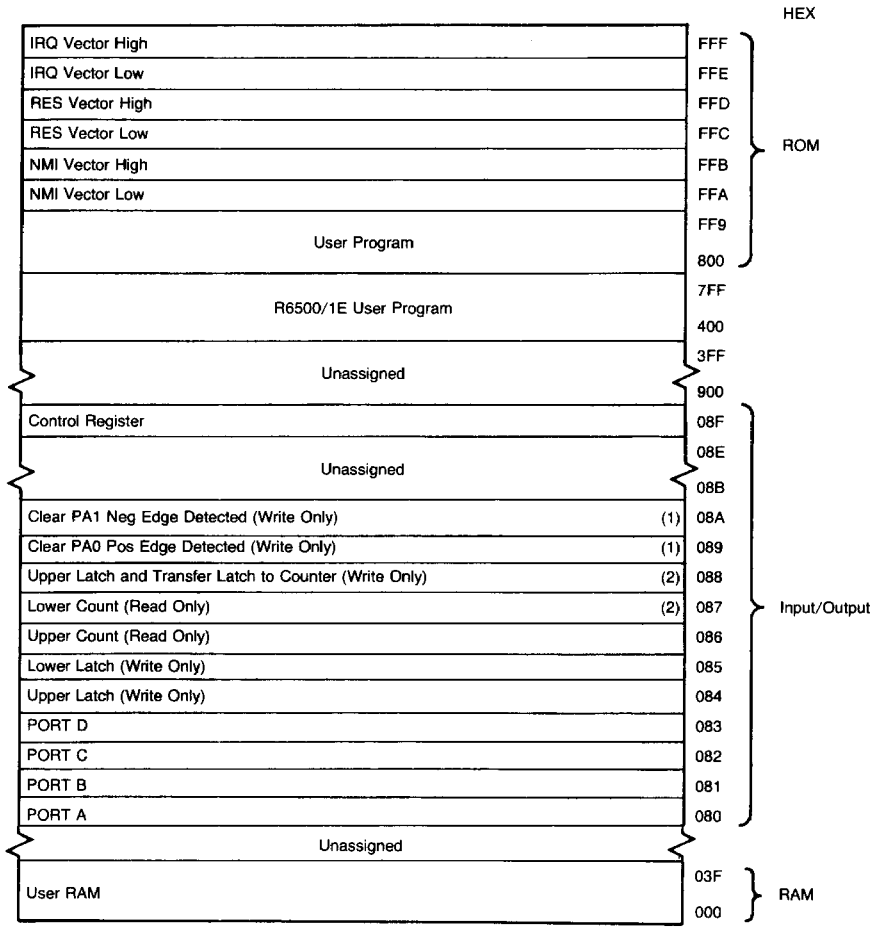


Figure 5-3. Typical R6500/1 Power Loss Recovery Flowcharts

www.DataSheet4U.com

www.DataSheet4U.com

APPENDIX A — SYSTEM MEMORY MAP



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow — Bit 7 in Control Register.

www.DataSheet4U.com

www.DataSheet4U.com

APPENDIX B — R6500 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document Order No. 202.

B.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero	PHA	Push Accumulator on Stack
BPL	Branch on Result Plus	PHP	Push Processor Status on Stack
BRK	Force Break	PLA	Pull Accumulator from Stack
BVC	Branch on Overflow Clear	PLP	Pull Processor Status from Stack
BVS	Branch on Overflow Set		
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
CPX	Compare Memory and Index X	SEC	Set Carry Flag
CPY	Compare Memory and Index Y	SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
INC	Increment Memory by One	TSX	Transfer Stack Pointer to Index X
INX	Increment Index X by One	TXA	Transfer Index X to Accumulator
INY	Increment Index Y by One	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

www.DataSheet4U.com

www.DataSheet4U.com

B2. INSTRUCTION SET SUMMARY TABLE

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V - B D I Z C	MNEMONIC
ADC	A + M + C → A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V . . . . Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N . . . . . Z .	AND
ASL	C ← [7 … 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N . . . . . Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							. . . . .	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							. . . . .	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							. . . . .	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																															M_7 M_6 . . . . Z .	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							. . . . .	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							. . . . .	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							. . . . .	BPL
BRK	BREAK													00	7	1																									. . 1 . 1 . .	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							. . . . .	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							. . . . .	BVS
CLC	0 → C													18	2	1																									 0	CLC
CLD	0 → D													D8	2	1																									. . . . 0 . .	CLD
CLI	0 → I													58	2	1																									. . . . 0 . .	CLI
CLV	0 → V													B8	2	1																									. 0	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N . . . . . Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N . . . . . Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N . . . . . Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2																DE	7	3													N . . . . . Z .	DEC
DEX	X − 1 → X													CA	2	1																									N . . . . . Z .	DEX
DEY	Y − 1 → Y													88	2	1																									N . . . . . Z .	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N . . . . . Z .	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N . . . . . Z .	INC
INX	X + 1 → X													E8	2	1																									N . . . . . Z .	INX
INY	Y + 1 → Y													C8	2	1																									N . . . . . Z .	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				. . . . .	JMP
JSR	JUMP SUB				20	6	3																																		. . . . .	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N . . . . . Z .	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							96	4	2	N . . . . . Z .	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N . . . . . Z .	LDY
LSR	0 → [7 … 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 . . . . . Z C	LSR
NOP	NO OPERATION													EA	2	1																									. . . . .	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N . . . . . Z .	ORA
PHA	A → Ms S − 1 → S													48	3	1																									. . . . .	PHA
PHP	P → Ms S − 1 → S													08	3	1																									. . . . .	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N . . . . . Z .	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[7 … 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N . . . . . Z C	ROL
ROR	→ [C] → [7 … 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N . . . . . Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									. . . . .	RTS
SBC	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V . . . . Z C (3)	SBC
SEC	1 → C													38	2	1																									 1	SEC
SED	1 → D													F8	2	1																									. . . . 1 . .	SED
SEI	1 → I													78	2	1																									. . . . . 1 .	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										. . . . .	STA
STX	X → M				8E	4	3	86	3	2																															96	4	2	. . . . .	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	. . . . .	STY
TAX	A → X													AA	2	1																									N . . . . . Z .	TAX
TAY	A → Y													A8	2	1																									N . . . . . Z .	TAY
TSX	S → X													BA	2	1																									N . . . . . Z .	TSX
TXA	X → A													8A	2	1																									N . . . . . Z .	TXA
TXS	X → S													9A	2	1																									. . . . .	TXS
TYA	Y → A													98	2	1																									N . . . . . Z .	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER
+ ADD
- SUBTRACT
∧ AND
∨ OR
∀ EXCLUSIVE OR
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO. CYCLES
NO. BYTES

www.DataSheet4U.com

www.DataSheet4U.com

APPENDIX C — SYSTEM SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial Industrial	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±10% for R6500/1, V_{CC} = 5.0V ±5% for R6500/1A, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	V	
RAM Standby Current (Retention Mode) Commercial Industrial	I_{RR}	 — —	 10 12	 — —	mA	
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	±1.0	±2.5	μA	V_{IN} = 0 to 5.0V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	—	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC} − 30%	—	—	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OUT} = 2.4V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
Input Capacitance XTLI, XTLO PA, PB, PC, PD, CNTR	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	600	990	mW	V_{CC} = +5.5V

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

www.DataSheet4U.com

www.DataSheet4U.com

AC CHARACTERISTICS

(V_{CC} = 5V ±10% for R6500/1, V_{CC} = 5V ±5% for R6500/1A)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	µsec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		µsec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		µsec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		µsec

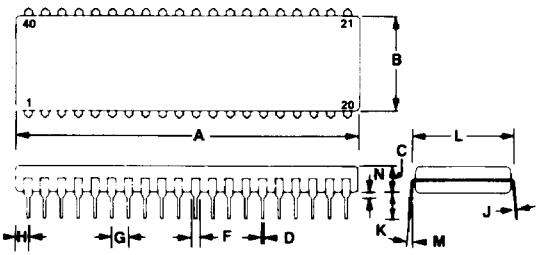
3

www.DataSheet4U.com

www.DataSheet4U.com

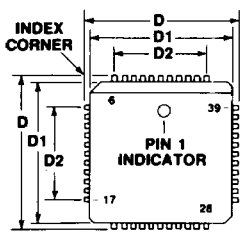
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP

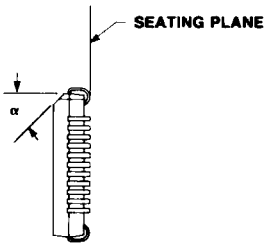


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

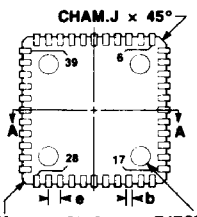
44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



TOP VIEW



SIDE VIEW

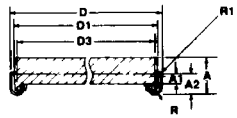


CHAM. h x 45° 3 PLCS

11 PINS PER SIDE EQUALLY SPACES

EJECTOR PIN MARKS 4 PLCS BOTTOM OF PACKAGE ONLY (TYPICAL)

BOTTOM VIEW



SECTION A-A

TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

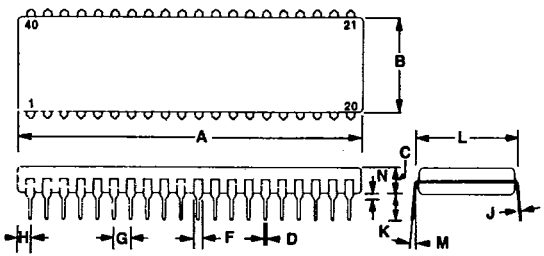
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

www.DataSheet4U.com

PACKAGE DIMENSIONS

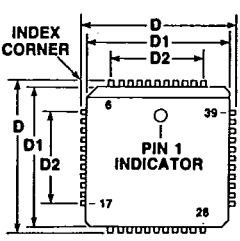
T-49-19-05

40-PIN PLASTIC DIP

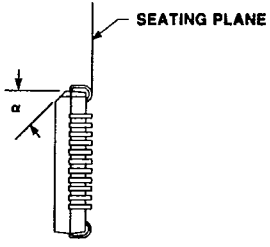


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

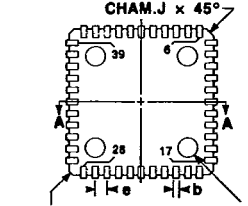
44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



TOP VIEW



SIDE VIEW

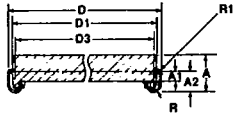


CHAM. h x 45° 3 PLCS

11 PINS PER SIDE EQUALLY SPACES

EJECTOR PIN MARKS 4 PLCS BOTTOM OF PACKAGE ONLY (TYPICAL)

BOTTOM VIEW



SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

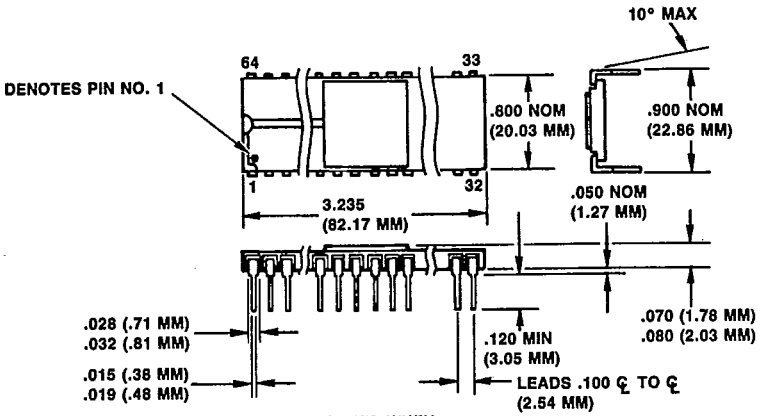
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

www.DataSheet4U.com

T-49-19-59

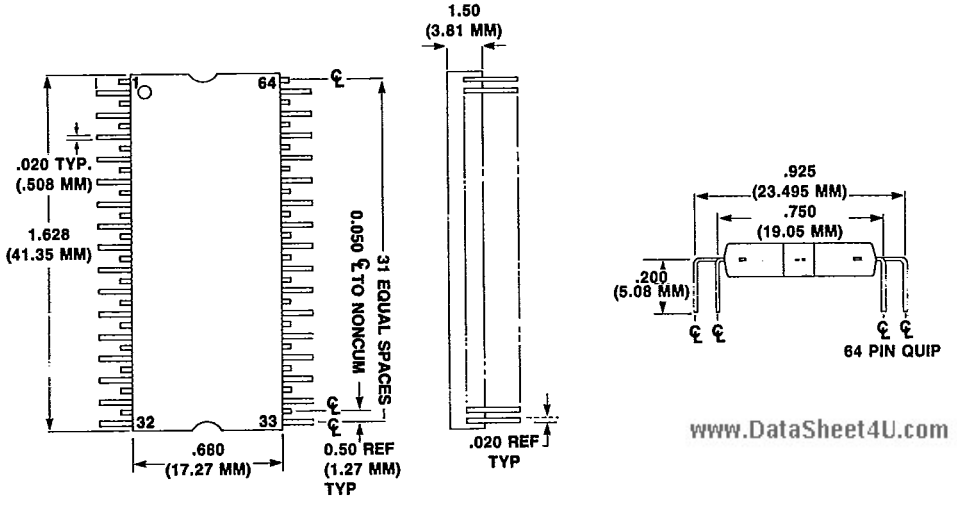
PACKAGE DIMENSIONS

R6500/1EC 64-PIN DIP CERAMIC



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

R6500/1EQ 64-PIN QUIP PLASTIC

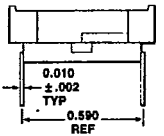


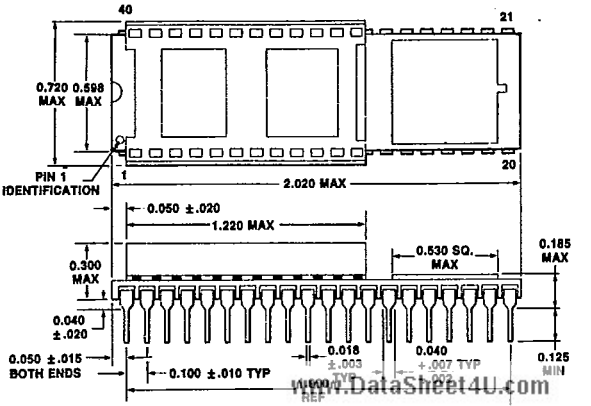
www.DataSheet4U.com

T-49-19-59

PACKAGE DIMENSIONS

40-PIN BACKPACK





www.DataSheet4U.com