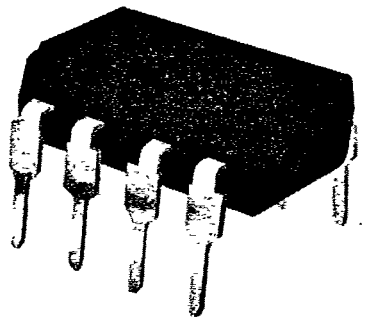
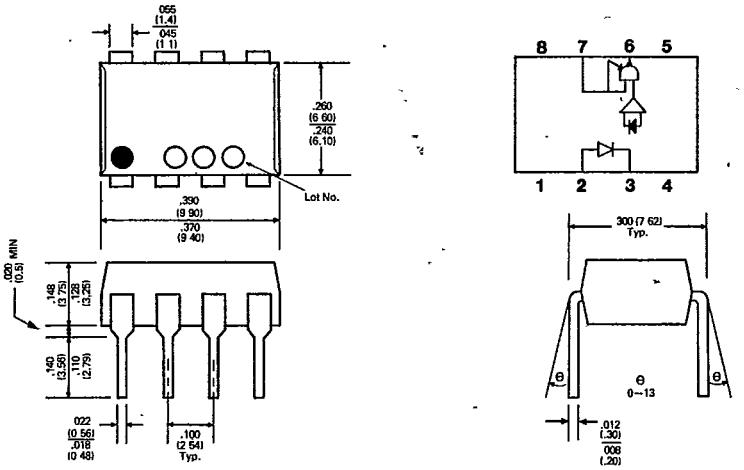
# IL100 IL101

## High Speed Opto Isolators



**PACKAGE DIMENSIONS IN INCHES (MM)**




### FEATURES

- Very High Speed — 65 ns (IL100)
- Typical Propagation Delay Time
- DTL/TTL Compatible — 5 V Supply
- Three State Output Logic for Multiplexing
- Built-in Schmitt Trigger to Avoid Oscillation
- Faraday Shielded Photodetector for Improved Common Mode Rejection
- U.L. Recognised (File No. E91231)

### DESCRIPTION

The IL100 and IL101 are optically coupled pairs consisting of a Gallium Arsenide Phosphide LED and a silicon monolithic integrated circuit including a photodetector. High speed digital information can be transmitted by the device while maintaining a high degree of electrical isolation between input and output. They can be used to replace pulse transformers in many digital interface applications. A built-in Schmitt Trigger provides hysteresis to reduce the possibility of oscillation.

### ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise noted)

| | |
|---|---|
| Storage Temperature | −55°C to +125°C |
| Operating Temperature | 0°C to +70°C |
| Lead Solder Temperature | 260°C for 10s (1.6 mm below seating plane) |
| Input-to-Output Isolation Voltage IL100 | ±2500 V |
| IL101 | ±1500 V |

#### Input Diode

| | |
|---|---|
| Forward Current | 10 mA |
| Reverse Voltage | 5 V |
| Enable Voltage | 5.5 V (Not to exceed $V_{CC}$ by more than 500 mV) |

#### Output Transistor

| | |
|---|---|
| Supply Voltage — $V_{CC}$ | 7 V |
| Current — $I_O$ | 100 mA |
| Collector Power Dissipation | 100 mW |
| Voltage — $V_O$ | 7 V |

### RECOMMENDED OPERATING CONDITIONS

| | Sym. | Min. | Max. | Units |
|---|---|---|---|---|
| Input Current, High Level | $I_{in}$ (1) | | 10 | mA |
| Supply Voltage, Output | $V_{CC}$ | 4.5 | 5.0 | V |
| Fan Out (TTL Load) | N | | 10 | |
| Operating Temperature | $T_A$ | 0 | 70 | °C |

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**ELECTRICAL CHARACTERISTICS** (Over recommended temperature 0°C to 70°C unless specified).



| Parameter | | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| $V_{OUT}$ (0): Logic (0) Output Voltage | IL101 | | 0.4 | 0.6 | V | $V_{CC}$ = 5.5V, $V_G$ = 2.4V, $I_{in}$ = 10 mA, $I_{out}$ (sinking) = 16 mA | | |
| | IL100 | | 0.4 | 0.6 | V | $V_{CC}$ = 5.5V, $V_G$ = 2.4V, $I_{in}$ = 5 mA, $I_{out}$ (sinking) = 16 mA | | |
| $I_G$ (0): Logic (0) Gate Current | | | −1.6 | −2.0 | mA | $V_{CC}$ = 5.5 V, $V_G$ = 0.5 V | | |
| $I_G$ (1): Logic (1) Gate Current | | | 0 | | mA | $V_{CC}$ = 5.5 V, $V_G$ = 0.5 V | | |
| $I_{CC}$ (1): Logic (1) Supply Current | | | 18 | 22 | mA | $V_{CC}$ = 5.5 V, $V_G$ = 0.5 V, $I_{in}$ = 0 | | |
| $I_{CC}$ (0): Logic (0) Supply Current | | | 18 | 22 | mA | $V_{CC}$ = 5.5 V, $V_G$ = 0.5 V, $I_{in}$ = 10 mA | | |
| $I_{CC}$ | | | 13 | 16 | mA | $V_{CC}$ = 5.5 V, $V_G$ = 2.4 V, $I_{in}$ = 0 | | |
| $I_{CC}$ | | | 17 | 21 | mA | $V_{CC}$ = 5.5 V, $V_G$ = 2.4 V, $I_{in}$ = 10 mA | | |
| $BV_{IO}$: Insulation Voltage (Input to Output) | IL101 | 1500 | | | V | | | |
| | IL100 | 2500 | | | V | $T_A$ = 25°C | | 5 |
| $R_{IO}$: Resistance | | 10 | | | ohm | $V_{IO}$ = 500 V, $T_A$ = 25°C | | 5 |
| $C_{IO}$: Capacitance | | | 0.6 | 0.8 | pF | f = 1 MHz, $T_A$ = 25°C | | 5 |
| CMRV (1): Common Mode Rejection Voltage to Logical (0) Level | | | 60 | | VACpp | f = 10 MHz, $R_L$ = 350 ohm, $T_A$ = 25°C $V_{out}$ (min.) = 2 V, $I_{in}$ = 0 mA | | 6 |
| CMRV (0): Common Mode Rejection Voltage to Logical (1) Level | | | 60 | | VACpp | f = 10 MHz, $R_L$ = 350 ohm, $T_A$ = 25°C, $V_{out}$ (max.) = 0.6 V, $I_{in}$ = 7.5 mA | | 6 |
| CTR: Current Transfer Ratio | | | 1000 | | % | $I_{in}$ = 5.0 mA, $V_{CC}$ = 5 V, $R_L$ = 100 ohms, $T_A$ = 25°C | | 7 |
| $V_F$: Forward Voltage | | 1.2 | 1.5 | 1.75 | V | $I_{in}$ = 10 mA, $T_A$ = 25°C | 1 | 8 |
| $BV_R$: Reverse Breakdown Voltage | | 5 | | | V | $I_R$ = 10 µA, $T_A$ = 25°C | | |
| $C_{IN}$: Capacitance | | | 25 | | pF | V = 0, f = 1 MHz, $T_A$ = 25°C | | |
| $I_{in}$ (1): Logic (1) Input Current to Ensure Logic (0) Output | | 5 | | | mA | | 1, 2 | |
| $I_{in}$ (0): Logic (0) Input Current to Ensure Logic (1) Output | | | | 250 | µA | | 1, 2 | |
| $V_G$ (1) : Logic (1) Gate Voltage | | 2.0 | | | V | | | |
| $V_G$ (0) : Logic (0) Gate Voltage | | | | 0.8 | V | | | |
| $I_{out}$ (off) | | −100 | | +100 | µA | $V_{CC}$ = 5.5 V, $V_O$ = 1.5 V, $V_G$ = 0, $I_{in}$ = 0, 10 mA | | |

**SWITCHING CHARACTERISTICS** (at $T_A$ = 25°C, $V_{CC}$ = 5 V)

| Parameter | | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ (1): Propagation Delay Time to Logical (1) Level | IL100 | 65 | 75 | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 7.5 mA | | 1 |
| | IL101 | 100 | 200 | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 10 mA | | 1 |
| $t_{pd}$ (0): Propagation Delay Time to Logical (0) Level | IL100 | 65 | 75 | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 7.5 mA | | 2 |
| | IL101 | 100 | 200 | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 10 mA | | 2 |
| $t_r$ − $t_f$: Output Rise-Fall Time (10-90%) | IL100 | 15 | | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 7.5 mA | | |
| $t_G$ (1): Propagation Delay Time of Gate $V_G$ (1) to $V_G$ (0) | IL100 | 15 | | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 7.5 mA. $V_G$ (1) = 2 V, $V_G$ (0) = 0.5 V | | 3 |
| $t_G$ (0): Propagation Delay Time of Gate $V_G$ (0) to $V_G$ (1) | IL100 | 15 | | ns | $R_L$ = 350 Ω, $C_L$ = 15 pF, $I_{in}$ = 7.5 mA, $V_G$ (1) = 2 V, $V_G$ (0) = 0.5 V | | 4 |

**OPERATING PROCEDURES AND DEFINITIONS:**

Logic Convention — The IL100 and IL101 are defined in terms of positive logic.

Bypassing — A ceramic capacitor (.01 µF min.) should be connected from pin 8 to pin 5. Its purpose is to stabilize the operation of the switching amplifier. Failure to provide the bypassing may impair the switching properties.

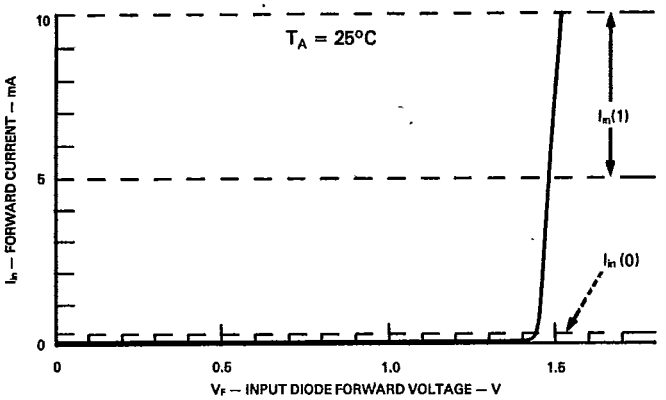
Polarities — All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Gate Input — No external pull-up required for a logic (1).

**NOTES:**

1. The $t_{pd}$ (1) propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V trailing edge of the output pulse.
2. The $t_{pd}$ (0) propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V leading edge of the output pulse.
3. The $t_G$ (1) gate propagation delay is measured from the 1.5 V point of the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
4. The $t_G$ (0) gate propagation delay is measured from the 1.5 V point on the input pulse to the 1.5 V point on the leading edge of the output pulse. The input diode is DC biased to 10 mA ($I_{in}$ (1)).
5. Pins 2 and 3 shorted together, and pins 5, 6, 7 and 8 shorted together.
6. CMRV (1) is the maximum tolerable common mode voltage to assure that the output will remain in a logic (1) state ($V_{out}$ > 2.0V). CMRV (0) is the maximum tolerable common mode voltage to assure that the output will remain in a logic (0) state ($V_{out}$ < 0.6V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10 mA $V_F$ decreases with increasing temperature at the rate of 1.6 mV/°C.

## 1. INPUT DIODE FORWARD CHARACTERISTICS

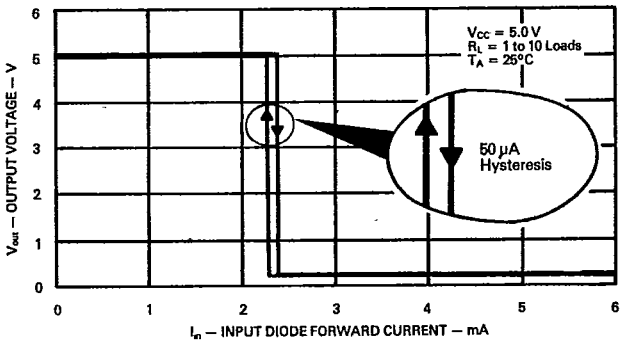


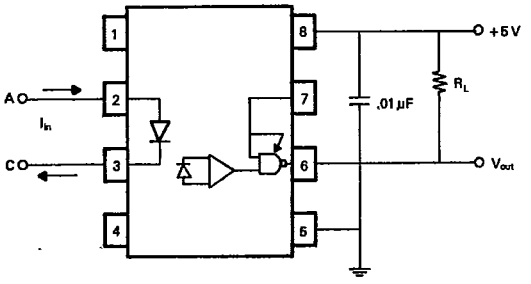

## 2. INPUT-OUTPUT CHARACTERISTICS

Truth Table
(positive Logic)

| Input* | Enable | Output |
|---|---|---|
| 1 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | Off |
| 0 | 0 | Off |

*See definition of terms for logic state

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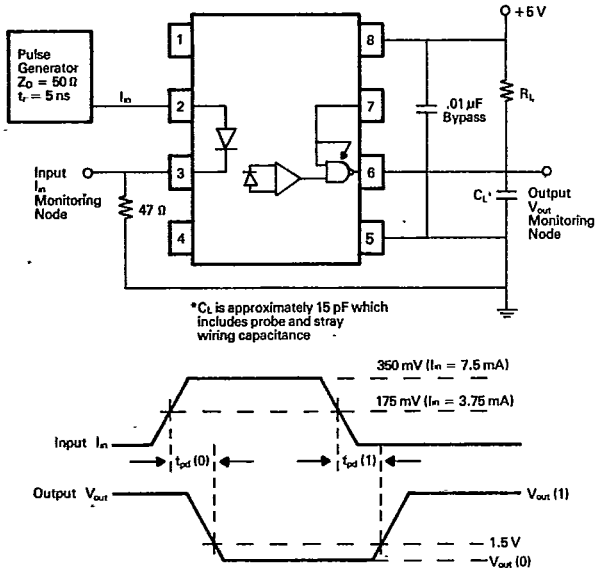
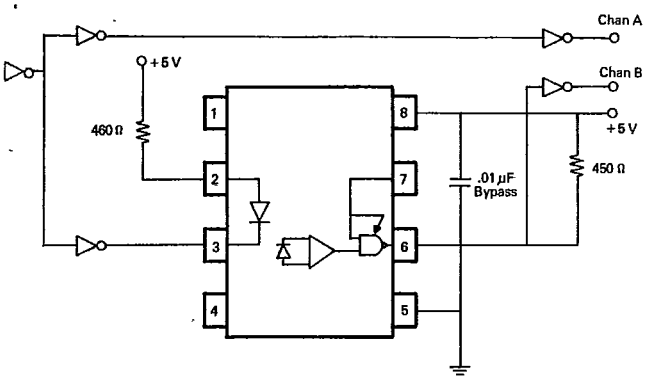
### 3. TEST CIRCUIT FOR $T_{pd}$ (0) AND $t_{pd}$ (1)

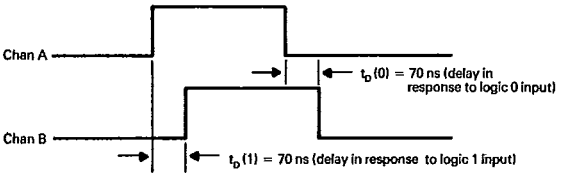




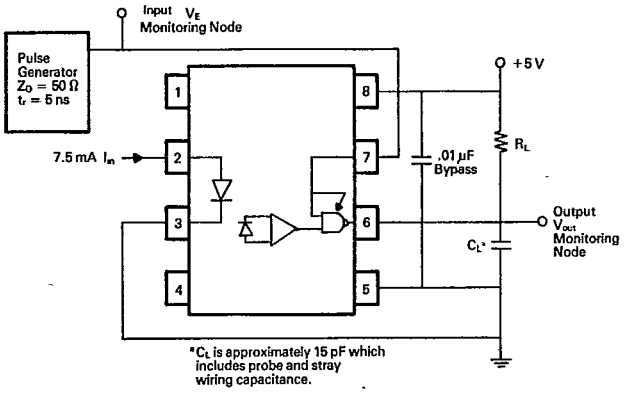


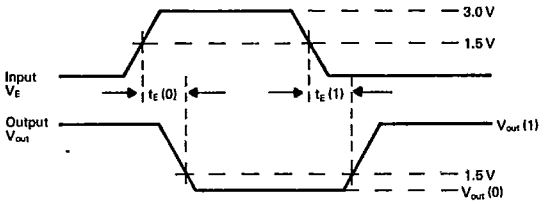
### 4. RESPONSE DELAY BETWEEN TTL GATES




### 5. TEST CIRCUIT FOR $t_E$ (0) AND $t_E$ (1)




### 6. TYPICAL COMMON MODE REJECTION CHARACTERISTICS AND CIRCUIT