S3455

SONET/SDH/ATM OC-48 4-Bit Transceiver with CDR

Product Brief

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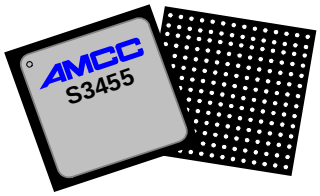

Description

The S3455 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-48 (2.488 Gbps – 2.670 Gbps) interface device. The S3455 receives an OC-48 scrambled Non-Return to Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Locked Loop (PLL) on the S3455 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz (or 166.62 MHz) reference clock in support of existing system clocking schemes.

The low jitter LVDS interface is compliant with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3455 is packaged in a 196 Pin PBGA, offering designers a small package outline.

Overview

The S3455 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. The block diagram in Figure 2 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end. The table below shows the suggested interface devices for the S3455.

AMCC Suggested Interface Devices

S19202	STS-192 POS/ATM SONET/SDH Mapper

– At a Glance –

General Features

- CMOS 0.18 micron technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports OC-48 (2488.32 Mbps) with FEC
- Reference frequency of 155.52 MHz to 166.62 MHz
- Interface to LVDS and LVCMOS logic
- 4-bit LVDS data path
- 196 Pin PBGA
- Diagnostic loopback mode
- Supports line timing
- Lock detect
- Signal detect input
- Low jitter LVDS interface
- Internal FIFO to decouple transmit clocks
- Single 1.8 V supply
- Typical power under 1.0 W

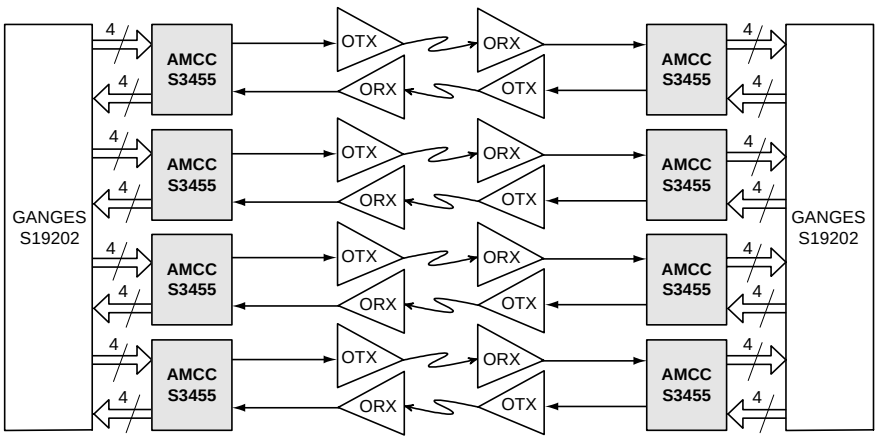

Figure 1. System Block Diagram

The S3455 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations

1. 4-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations For One Channel

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 4-bit parallel output

Internal clocking and control functions are transparent to the user.

Prefix	Device	Package
S – Integrated Circuit	3455	PB - 196PBGA

X	XXXX	XX
Prefix	Device	Package (S3455 PB)

Figure 2. S3455 Ordering Information

Applications

- Wavelength Division Multiplexing (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

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