ADS-111
12-Bit, 500 KHz, LowPower Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **500 KHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 1.4 Watts**
- **Three-state output buffers**

GENERAL DESCRIPTION

DATEL's ADS-111 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 500 KHz is achieved while only dissipating 1.4 Watts.

Manufactured using thick-film and thin-film hybrid technology, the ADS-111's exclusive performance is based upon a digitally-corrected subranging architecture.

DATEL further enhances this technology by using a proprietary chip and unique laser trimming schemes. Figure 1 is a simplified block diagram of the ADS-111.

The ADS-111 features two pin-programmable analog input voltage ranges: 0 to +10V and ±5V. The input impedance is specified at 15 M Ohms. The ADS-111 is also guaranteed to have no missing codes over the operating temperature range.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary.

The power requirements are ±15V dc and +5V dc. The ADS-111 is available in the commercial 0 degrees Celsius to +70 degrees Celsius and military -55 degrees Celsius to +125 degrees Celsius operating temperature range.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on high reliability screening, contact DATEL.

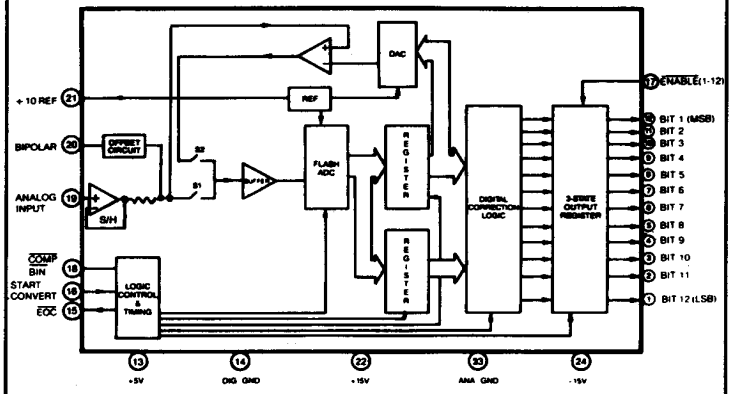
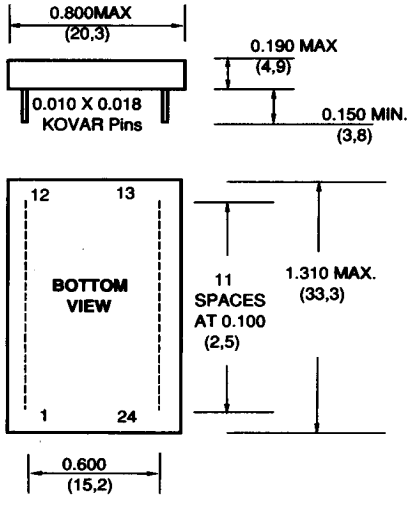


Figure 1. ADS-111 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, 0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LSB)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	+5V
14	DIGITAL GROUND
15	$\overline{EOC}$
16	START CONVERT
17	$\overline{ENABLE}$ (1-12)
18	$\overline{COMP\ BIN}$
19	ANALOG INPUT
20	BIPOLAR
21	+10V REF
22	+15V
23	ANALOG GROUND
24	-15V

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-111	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	5.0	15.0	–	M Ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA
A/D PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±3	LSB
Integral Non-Lin. Tempco	–	±5	±10	ppm/ °C
Differential Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±1	LSB
Differential Non-Lin. Tempco	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±5	±10	LSB
0 °C to +70 °C	–	±6	±18	LSB
-55 C to +125 °C	–	±10	±32	LSB
Unipolar Zero Error, +25 °C (See Tech Note 1)	–	±3	±5	LSB
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)	–	±3	±5	LSB
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±4	±8	LSB
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±4	±8	LSB
Gain Tempco	–	±20	±40	ppm/ °C
Conversion Times				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 °C to +125 °C	–	–	1.15	µSec.
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	12 Bits			
Output Coding				
(Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary Complementary offset binary			
SAMPLE/HOLD PERFORMANCE				
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty	–	±100	–	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec.
0 °C to +70 °C	–	–	765	nSec.
-55 °C to +125 °C	–	–	900	nSec.
(Sinusoidal Input)	–	–	465	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.5	+5.0	+5.5	Volts dc
Power Supply Current				
+15V dc Supply	–	+38	+43	mA
-15V dc Supply	–	-36	-44	mA
+5V dc Supply*	–	+66	+75	mA
Power Dissipation	–	1.4	1.75	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 4. Remove system errors or adjust the small initial errors of the ADS-111 to zero using the optional external circuitry shown in Figure 3. The external adjustment circuit has no affect on the throughput rate.

2. When the optional external adjustment circuitry is used, additional input ranges are available. Refer to Figure 3 and Table 4.

3. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane).

   Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

4. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

5. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

6. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "1" (high).

THEORY OF OPERATION

This theory of operation describes the ADS-111's function in conjunction with its internal sample-and-hold amplifier for digitizing sinusoidal signals. The ADS-111 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADS-111 guarantees a 500 KHz throughput rate over the temperature range when the START CONVERT pulse of 200 nanoseconds is provided at a 500 KHz rate. The 500 KHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or DC level signals is longer and listed under the acquisition specifications (10V step).

The ADS-111 is in the sample mode when the internal S/$\overline{\text{H}}$ CONTROL is high (S/$\overline{\text{H}}$ is in the high state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/$\overline{\text{H}}$ CONTROL low. This assures the sample-hold has the minimum required acquisition time for the particular application mode. Sinusoidal inputs being digitized by utilizing a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 225 nanosecond delay before $\overline{\text{EOC}}$ goes high and the A/D conversion begins. This consists of the remaining 190 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to $\overline{\text{EOC}}$ high. The hold mode settling time and input settling time requirements required for the first pass of the A/D conversion are met when observing this time.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. $\overline{\text{EOC}}$ goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{\text{EOC}}$ going low). The sample/hold control output goes high shortly before $\overline{\text{EOC}}$ goes low, indicating that the S/$\overline{\text{H}}$ is back sampling the input. This feature improves the overall throughput rate of the ADS-111.

Data from the previous conversion is valid and capable of being latched 20 nanoseconds after the falling edge of $\overline{\text{EOC}}$ and remains valid for 1300 nanoseconds. Data from the new conversion is valid a minimum of 20 nanoseconds after the next $\overline{\text{EOC}}$ low transition. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput rate over temperature of the ADS-111 for sinusoidal inputs consists of 465 nanoseconds for the acquisition time, 225 nanoseconds for the START CONVERT and min-max propagation delays, and 1150 nanoseconds for the A/D conversion. An internal function reduces this cumulative time by 30 nanoseconds by putting the sample/hold back into the sample mode 30 nanoseconds before $\overline{\text{EOC}}$ goes low. A throughput time of 1810 nanoseconds is obtained and the minimum throughput rate of 500 KHz is easily met.

Combining the A/D and S/H in one device allows the ADS-111 to guarantee a throughput rate of 500 KHz over the -55 degrees Celsius to +125 degrees Celsius temperature range for the complete system. Retriggering of the START CONVERT pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.

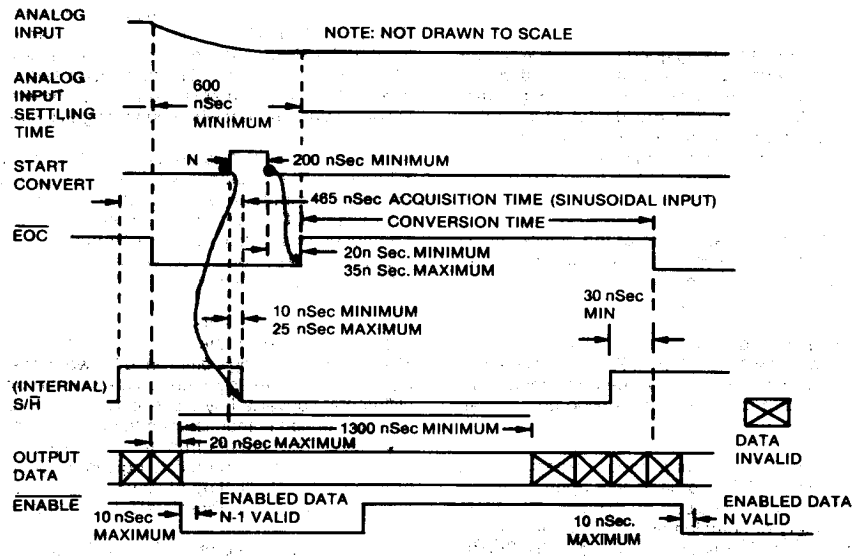


Figure 2. ADS-111 Timing Diagram

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 1. Signal Timing Summary

LINE	DURATION
START CONVERT Pulse Width	200 nSec. minimum
Analog Input Settling Time	600 nSec. minimum
START CONVERT Low to $\overline{EOC}$ High Propagation Delay	35 nSec. maximum
$\overline{EOC}$ Low to Previous Output Data Invalid	1320 nSec. minimum
Data Valid After $\overline{EOC}$ goes Low	20 nSec. maximum
$\overline{ENABLE}$ to Output Data Valid Propagation Delay	10 nSec. maximum
$\overline{EOC}$ Low to START CONVERT High (Sinusoidal Inputs)	425 nSec. minimum

INPUT CONNECTIONS

Table 2. ADS-111 Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to PIN 21
0 to +10V dc	Pin 19	Pin 20 to GROUND

Table 3a. Zero and Gain Adjust, Unipolar Operation

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc

Table 3b. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±5V dc	+1.22mV dc	+4.9963V dc

CALIBRATION PROCEDURE

Should removal of system errors or the small initial errors be desired, adjustment is accomplished as follows:

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Calibration con't.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ 1/2 LSB) or the bipolar zero adjustment (zero +1/2 LSB). For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 18) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the $\overline{\text{COMP BIN}}$ (pin 18) tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 18) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with $\overline{\text{COMP BIN}}$ (pin 18) tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for $\overline{\text{COMP BIN}}$ (pin 18) tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 6 and 7.

Table 4. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

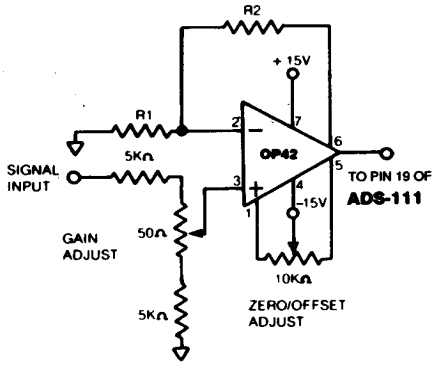


Figure 3. Optional Calibration Circuit

The performance characteristics shown in Table 5 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

Table 5. Dynamic Performance

Throughput Rate (Changing Inputs)	MIN	TYP	MAX	UNITS
+25 °C	500	600	–	KHz
0 °C to +70 °C	500	600	–	KHz
-55 C to +125 °C	500	–	–	KHz
A/D Conversion Time				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 C to +125 °C	–	–	1.15	µSec.
Total Harmonic Distortion				
DC to 100 KHz at Vin ≤5V p-p	-65	-70	–	dB
DC to 60 KHz at Vin = 10V p-p	-65	-70	–	dB

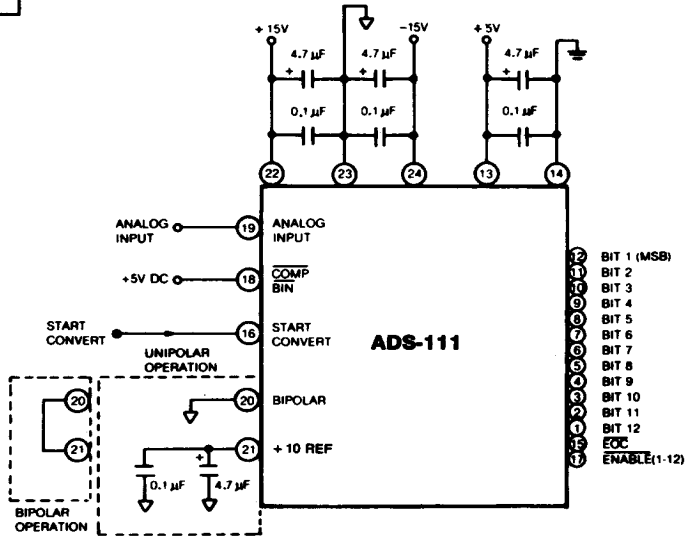


Figure 4. Typical ADS-111 Connection Diagram

Table 6. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE (Volts dc) ±5V	OUTPUT CODING OFFSET BINARY MSB LSB	COMP. OFFSET BINARY MSB LSB
+FS -1 LSB	+4.9976V	1111 1111 1111	0000 0000 0000
+3/4 FS	+3.7500V	1110 0000 0000	0001 1111 1111
+1/2 FS	+2.5000V	1100 0000 0000	0011 1111 1111
0	0.0000V	1000 0000 0000	0111 1111 1111
-1/2 FS	-2.5000V	0100 0000 0000	1011 1111 1111
-3/4 FS	-3.7500V	0010 0000 0000	1101 1111 1111
-FS +1 LSB	-4.9976V	0000 0000 0001	1111 1111 1110
-FS	-5.0000V	0000 0000 0000	1111 1111 1111

Table 7. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGE (Volts dc) 0 to +10V	OUTPUT CODING STRAIGHT BINARY MSB LSB	COMP. BINARY MSB LSB
+FS-1LSB	+9.9976V	1111 1111 1111	0000 0000 0000
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111
1/4 FS	+2.5000V	0100 0000 0000	1011 1111 1111
1/8 FS	+1.2500V	0010 0000 0000	1101 1111 1111
1 LSB	+0.0024V	0000 0000 0001	1111 1111 1110
0	0.0000V	0000 0000 0000	1111 1111 1111

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-111MC	0 °C to +70 °C	Hermetic
ADS-111MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

Part Number	Description
TP10K *	Trimming Potentiometer
TP50*	Trimming Potentiometer

* Only required if optional external calibration circuitry is used.

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For high reliability versions of the ADS-111 contact DATEL.