Index of /ds/LM/

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LM79XX_A.pdf 22-Dec-99 00:12 194K

FAIRCHILD
SEMICONDUCTOR™

LM101A/LH2101A

General Purpose Operational Amplifier

Features

- Input offset voltage 0.7 mV
- Input bias current 30 nA
- Input offset current 1.5 nA
- Full frequency compensation 30pF
- Supply voltage ±5.0V to ±20V

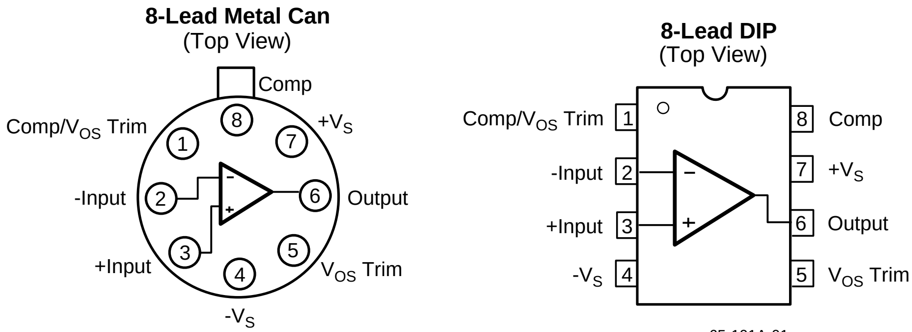
Description

The LM101A/LH2101A is a general purpose high performance operational amplifier fabricated monolithically on a silicon chip by an advanced epitaxial process. The LH2101A consists of two LM101A ICs in one 16-lead DIP. The units may be fully compensated with the addition of a 30 pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

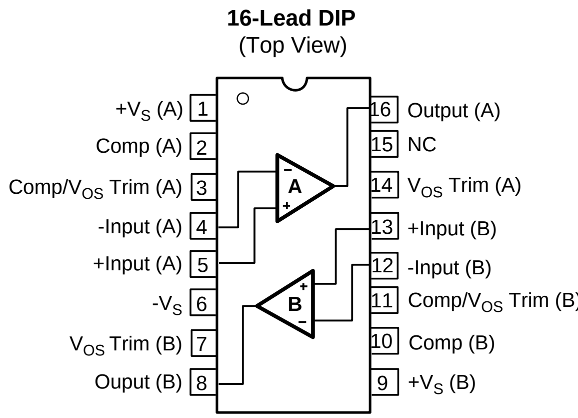
The device may be operated as a comparator with a differential input as high as 30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

The LM101A and LH2101A operate over the full military temperature range from -55°C to +125°C.

Pin Assignments



65-101A-01



65-101A-02

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage		±22	V
Differential Input Voltage		30	V
Input Voltage[1]		±15	V
Output Short-Circuit Duration[2]	Indefinite		
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	°C
Lead Soldering Temperature (60 sec)		+300	°C

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

Parameter	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Maximum P_D T_A <50°C	833 mW	658 mW	1042 mW
Thermal Resistance, θ_{JC}	45°C/W	50°C/W	60°C/W
Thermal Resistance, θ_{JA}	150°C/W	190°C/W	120°C/W
For T_A > 50°C Derate at	8.33 mW/°C	5.26 mW/°C	8.33 mW/°C

Electrical Characteristics

C = 30pF; ±5.0V ≤ V_S ≤ ±20V; -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameters	Test Conditions	LM101A/LH2101 A			Units
		MIn.	Typ.	Max.	
Input Offset Voltage	T_A = +25°C, R_S ≤ 50 kΩ		0.7	2.0	mV
Input Offset Current	T_A = +25°C		1.5	10	nA
Input Bias Current	T_A = +25°C		30	75	nA
Input Resistance	T_A = +25°C	1.5	4.0		MΩ
Supply Current	T_A = +25°C V_S = ±20V		1.8	3.0	mA
Large Signal Voltage Gain	T_A = +25°C, V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 KΩ	50	160		V/mV
Input Offset Voltage	R_S ≤ 50 KΩ			3.0	mV
Average Input Offset Voltage Drift	R_S ≤ 50 KΩ		3.0	15	µV/°C
Input Offset Current				20	nA
Average Input Offset Current Drift	+25°C ≤ T_A +125°C		0.01	0.1	nA/°C
	-55°C ≤ T_A +25°C		0.02	0.2	
Input Bias Current				100	nA
Supply Current	T_A = +125°C, V_S = ±20V		1.2	2.5	mA
Large Signal Voltage Gain	V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 KΩ	25			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 KΩ	±12	±14		V
	R_L = 2 KΩ	±10	±13		
Input Voltage Range	V_S = ±20V	±15			V
Common Mode Rejection Ratio	R_S ≤ 50 KΩ	80	96		dB
Power Supply Rejection Ratio	R_S ≤ 50 KΩ	80	96		dB

Typical Performance Characteristics

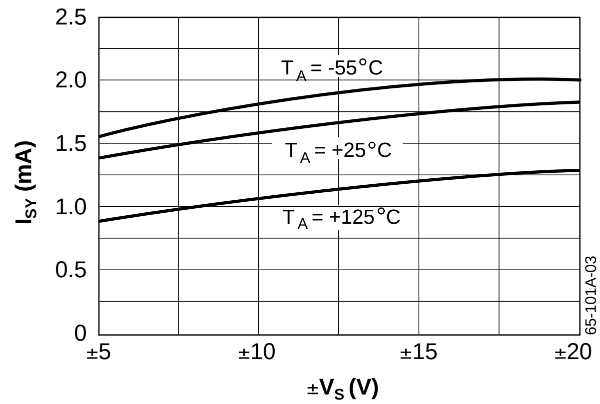


Figure 1. Supply Current vs. Supply Voltage

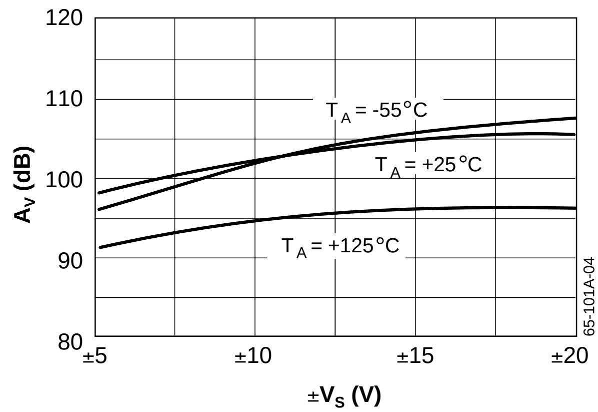


Figure 2. Voltage Gain vs. Supply Voltage

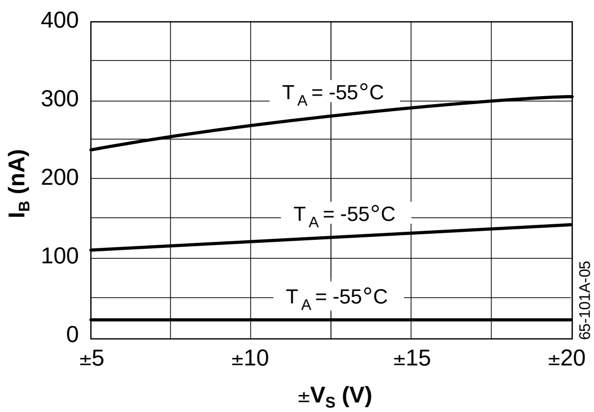


Figure 3. Input Bias Current vs. Supply Voltage

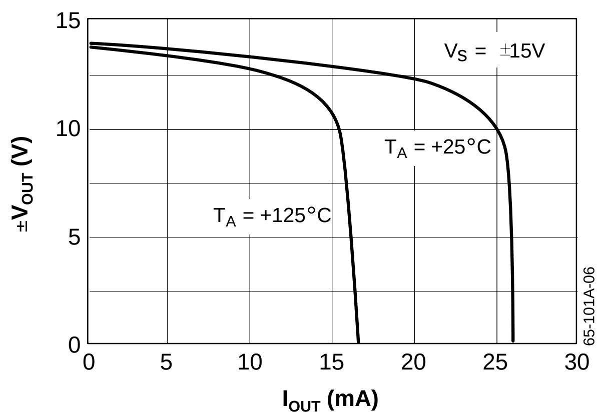


Figure 4. Current Limiting Output Voltage vs. Output Current

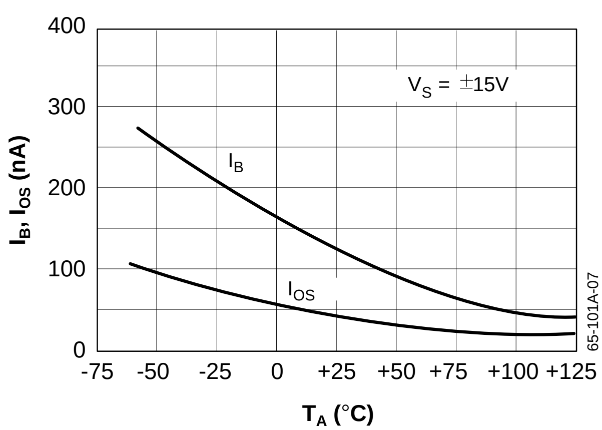


Figure 5. Input Bias, Offset Current vs. Temperature

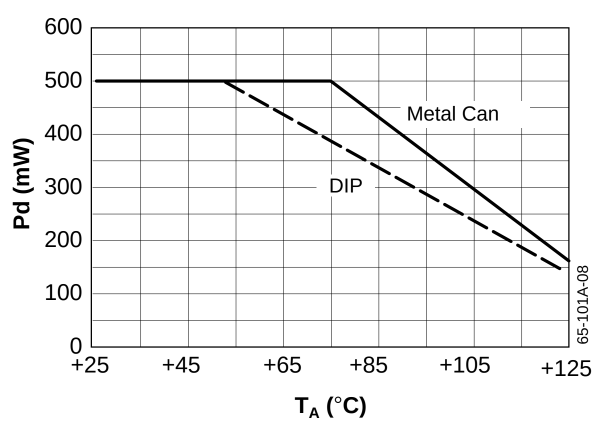


Figure 6. Maximum Power Dissipation vs. Temperature

Typical Performance Characteristics (continued)

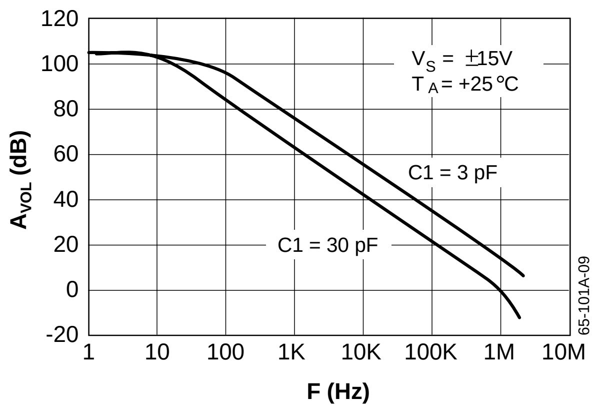


Figure 7. Open Loop Gain vs. Frequency

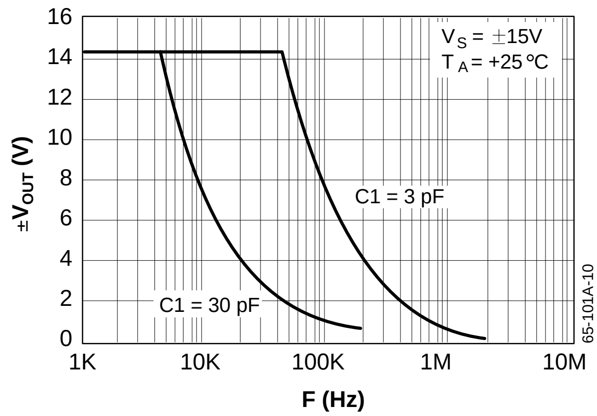


Figure 8. Output Voltage Swing vs. Frequency

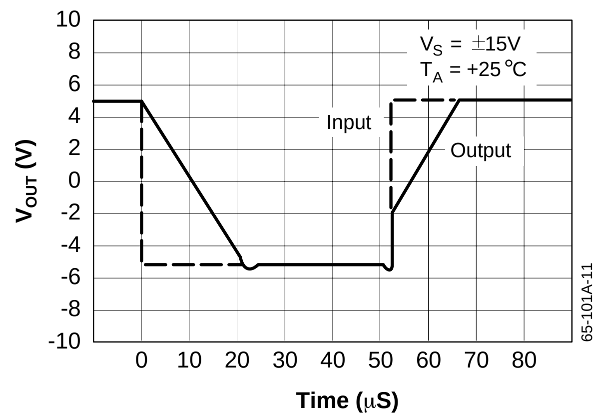
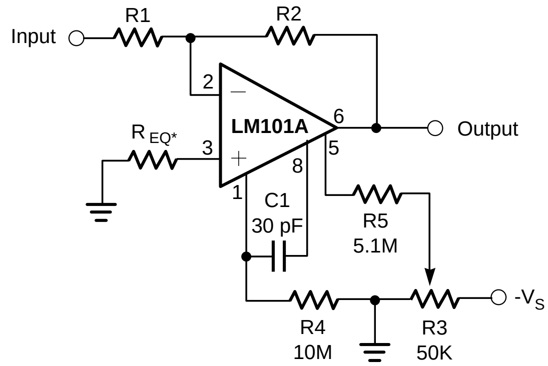


Figure 9. Follower Large Signal Pulse Response Output Voltage vs. Time

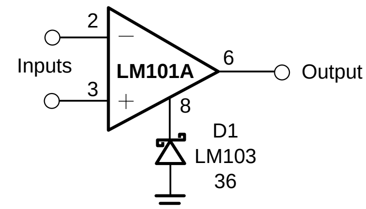
Typical Applications



*May be zero or equal to parallel combination of R1 and R2 for minimum offset.

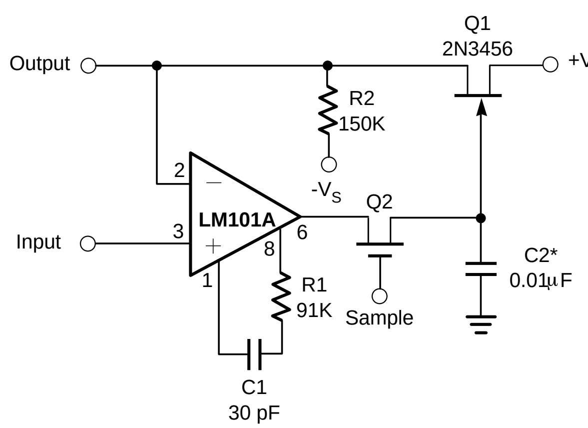
65-101A-12

Figure 10. Inverting Amplifier with Balancing Circuit



65-101A-13

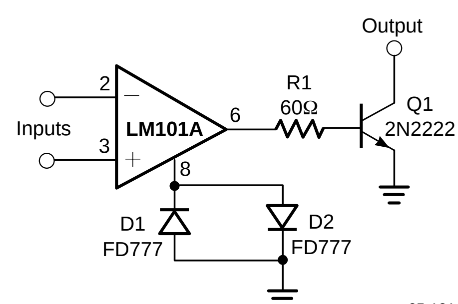
Figure 11. Voltage Comparator for Driving DTL or TTL ICs



*Polycarbonate dielectric capacitor

65-101A-14

Figure 12. Low Drift Sample and Hold



65-101A-15

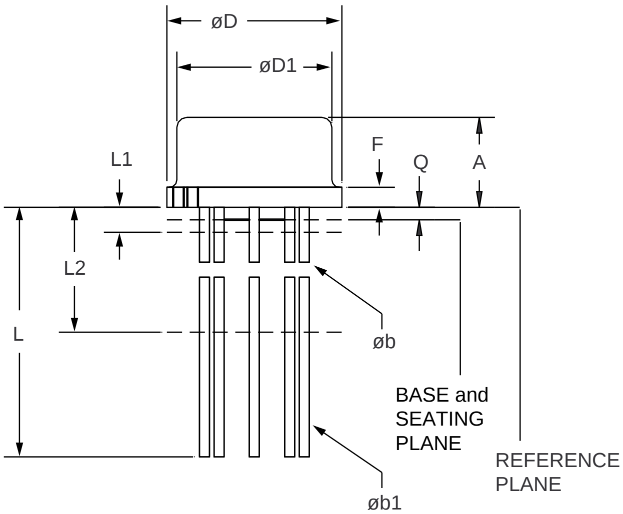
Figure 13. Voltage Comparator for Driving RTL Logic or High Current Driver

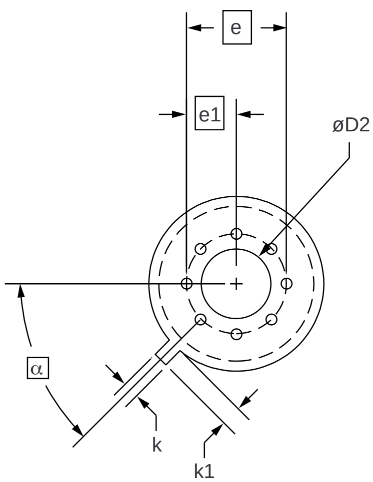
Notes:

Notes:

Mechanical Dimensions

8-Lead TO-99 Metal Can





Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

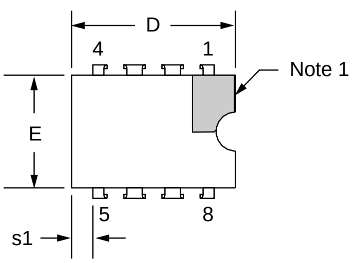
Mechanical Dimensions (continued)

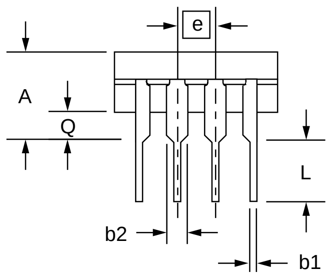
8-Lead Ceramic DIP

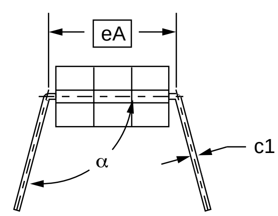
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







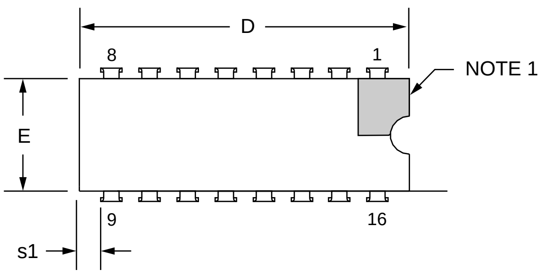
Mechanical Dimensions (continued)

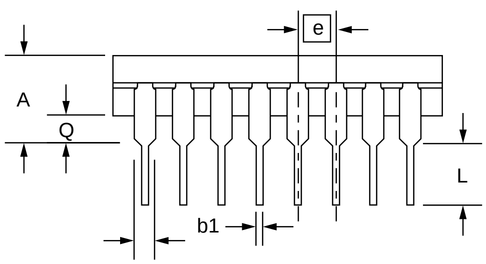
16-Lead Ceramic DIP

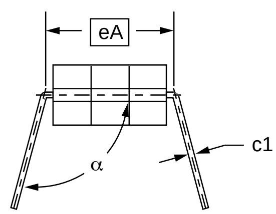
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.050	.065	1.27	1.65	2
c1	.008	.015	.20	.38	8
D	.745	.840	18.92	21.33	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.115	.160	2.92	4.06	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Fourteen spaces.







Ordering Information

Part Number	Package	Operating Temperature Range
LM101AD	8-Lead Ceramic DIP	-55°C to +125°C
LM101AD/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM101AT	8-Lead Metal Can	-55°C to +125°C
LM101AT/883B	8-Lead Metal Can	-55°C to +125°C
LH2101AD	16-Lead Ceramic DIP	-55°C to +1 25°C
LH2101AD/883B	16-Lead Ceramic DIP	-55°C to +125°C

Notes:
1. /883B suffix denotes Mil-Std-883. Level B processing.
2. Contact a Fairchild Semiconductor sales office or representative for ordering information on special package/ temperature range combinations.

5/20/98 0.0m 001
Stock#DS3000101A

LM108A/LH2108A

Precision Operational Amplifiers

Features

- Low input bias current — 2 nA
- Low input offset current — 200 pA
- Low input offset voltage — 500μV
- Low input offset drift — 5 μV/°C
- Wide supply range — ±3V to ±20V
- Low supply current — 0.6 mA
- High PSRR — 96 dB
- High CMRR — 96 dB
- MIL-STD-883B available

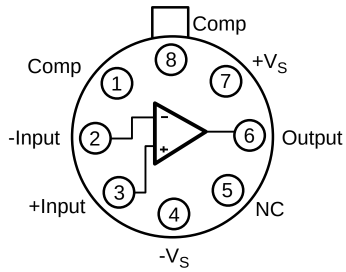
Description

The LM108A operational amplifiers features low input bias current combined with the advantages of bipolar transistor construction; input offset voltages and currents are kept low over a wide range of temperature and supply voltage. Fairchild Semiconductor's superbeta bipolar manufacturing process includes extra treatment at epitaxial growth to ensure low input voltage noise.

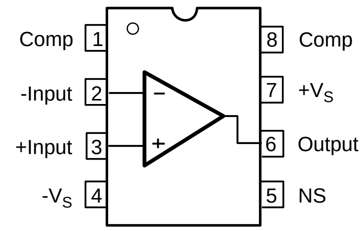
The LH2108 consists of two LM108 ICs in one 16-lead DIP. The "A" versions meet tighter electrical specifications than the plain versions. All types are available with 883B military screening.

Pin Assignments

8-Lead Metal Can
(Top View)

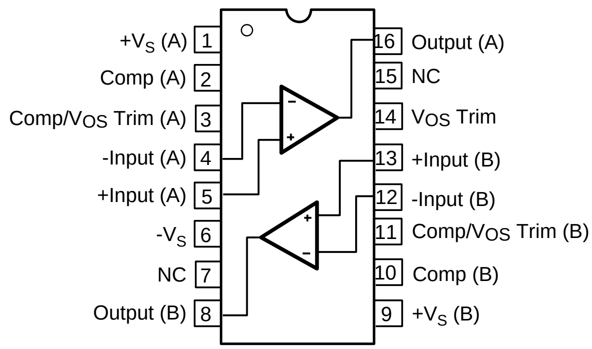


8-Lead DIP
(Top View)



65-108A-01

16-Lead DIP
(Top View)



65-108A-02

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage		±20	V
Differential Input Current[1]		±10	mA
Input Voltage[2]		±15	V
Output Short-Circuit Duration[2]	Continuous		
Operating Temperature Range	-55	+125	°C
Storage Temperature Range	-65	+150	°C
Lead Soldering Temperature (60 seconds)		+300	°C

Notes:

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Thermal Characteristics

Parameter	8-Lead Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Max. $P_D T_A$ < 50°C	658 mW	833 mW	1042 mW
Thermal Resistance, θ_{JC}	50°C/W	45°C/W	60°C/W
Thermal Resistance, θ_{JA}	190°C/W	150°C/W	120°C/W
For T_A > 50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

Electrical Characteristics

±5V, ≤ V_S ≤ ±20V and T_A ≤ +25°C unless otherwise noted

Parameters	Test Conditlons	LM108A/LH2108A			LM108/LH2108			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			0.3	0.5		0.7	2.0	mV
Input Offset Current			0.05	0.2		0.05	0.2	nA
Input Bias Current			0.8	2.0		0.8	2.0	nA
Input Resistance1		30	70		30	70		MΩ
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} ±10V, R_L ≥ 10KΩ	80	300		50	300		V/mV
Supply Current	Each Amplifier		0.3	0.6		0.3	0.6	mA
±5V, ≤ V_S ≤ ±20V; -55°C ≤ T_A ≤ +25°C unless otherwise noted								
Input Offset Voltage			0.4	1.0		1.0	3.0	mV
Avg. Input Offset Voltage Drift[2]			1.0	5.0		3.0	15	μV/°C
Input Offset Current			0.1	0.4		0.1	0.4	nA
Avg. Input Offset Current Drift[2]			0.5	2.5		0.5	2.5	pA/°C
Input Bias Current			1.0	3.0		1.0	3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L ≥ 10 KΩ	40	200		25	200		V/mV
Output Voltage Swing	R_L ≥ 10 KΩ, V_S = ±20V	±16	±18		±16	±18		V
Input Voltage Range	V_S = ±15V	±13.5			±13.5			V
Common Mode Rejection Ratio	V_{CM} = ±13.5V, V_S = ±15V	96	110		85	100		dB
Power Supply Rejection Ratio	V_S = ±15V	96	110		80	96		dB
Supply Current	Each Amplifier			0.6			0.6	mA

Notes:

1. Guaranteed by input bias current specification.
2. Sample tested.

Typical Applications

The LM108 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the LM108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

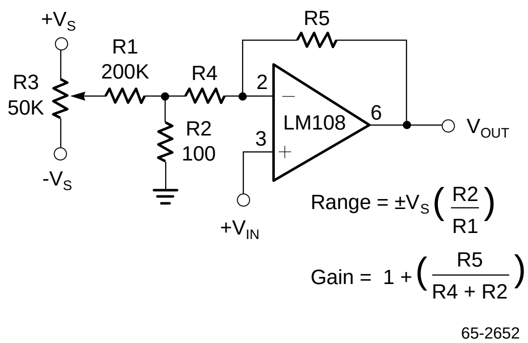


Figure 1. Offset Adjustment for Non-Inverting Amplifiers

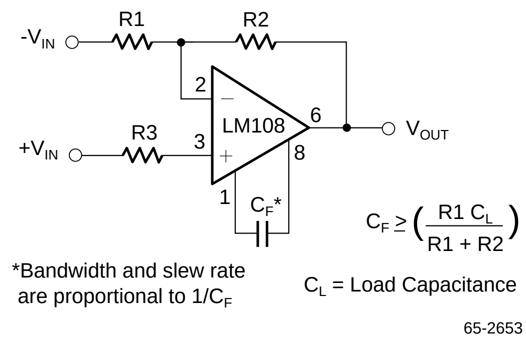


Figure 2. Standard Compensation Circuit

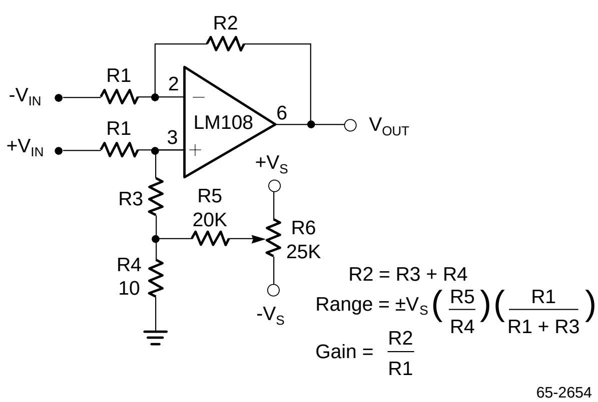


Figure 3. Offset Adjustment for Differential Amplifiers

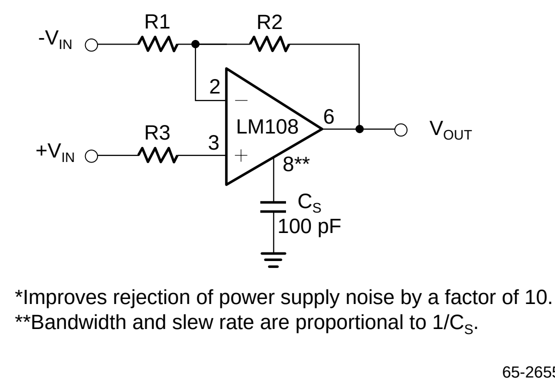


Figure 4. Alternate Frequency Compensation

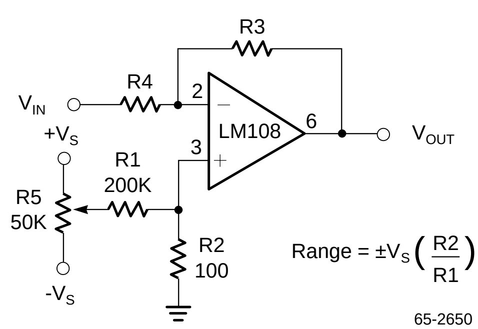


Figure 5. Offset Adjustment for Inverting Amplifiers

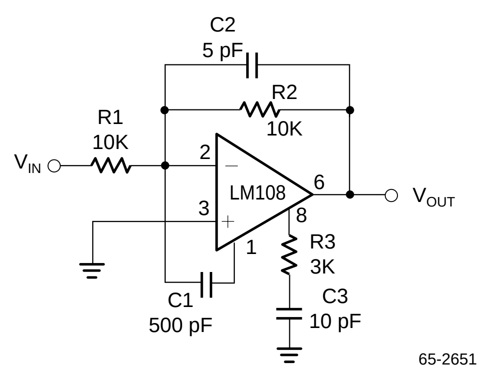
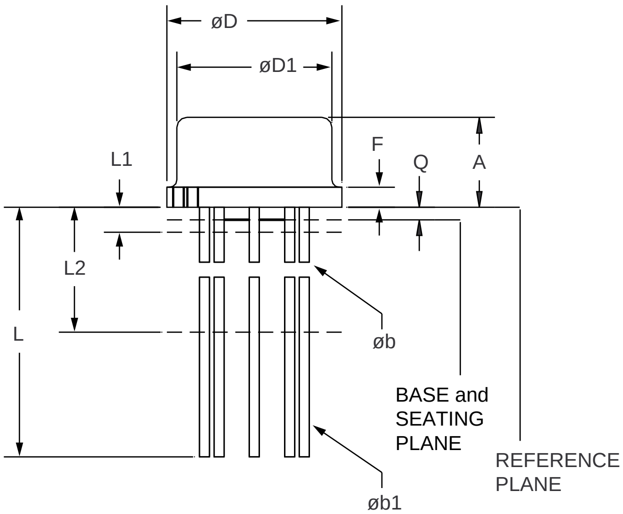
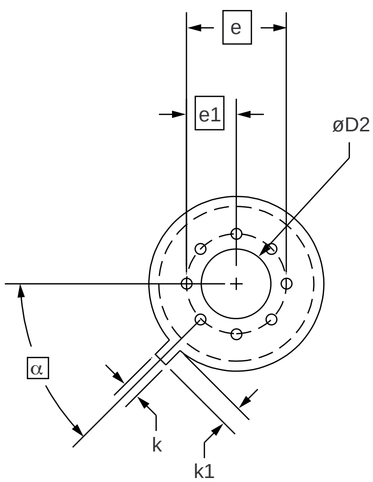


Figure 6. Feedforward Compensation

Mechanical Dimensions

8-Lead TO-99 Metal Can





Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

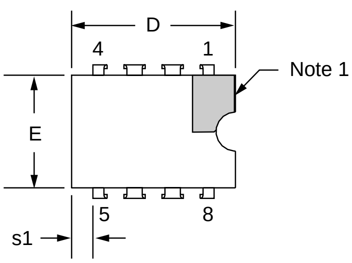
Mechanical Dimensions (continued)

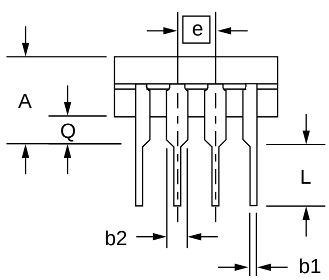
8-Lead Ceramic DIP

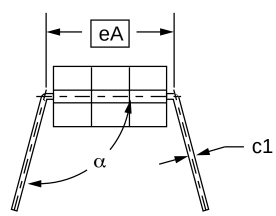
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







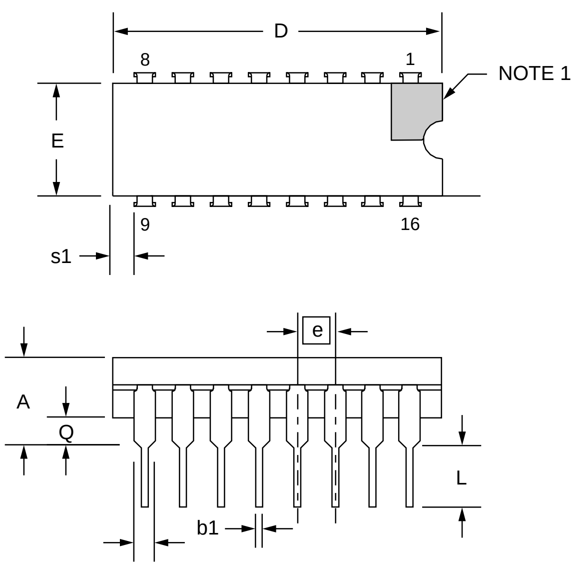
Mechanical Dimensions (continued)

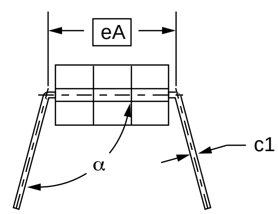
16-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.050	.065	1.27	1.65	2
c1	.008	.015	.20	.38	8
D	.745	.840	18.92	21.33	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.115	.160	2.92	4.06	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Fourteen spaces.





Ordering Information

Part Number	Package	Operation Temperature Range
LM108D	8-Lead Ceramic DIP	-55°C to +125°C
LM108D/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM108AD	8-Lead Ceramic DIP	-55°C to +125°C
LM108AD/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM108T	8-Lead Metal Can TO-99	-55°C to +125°C
LM108T/883B	8-Lead Metal Can TO-99	-55°C to +125°C
LM108AT	8-Lead Metal Can TO-99	-55°C to +125°C
LM108AT/883B	8-Lead Metal Can TO-99	-55°C to +125°C
LH2108D	16-Lead Ceramic DIP	-55°C to +125°C
LH2108D/883B	16-Lead Ceramic DIP	-55°C to +125°C
LH2108AD	16-Lead Ceramic DIP	-55°C to +125°C
LH2108AD/883B	16-Lead Ceramic DIP	-55°C to +125°C

Note:

1. /883B suffix denotes Mil-Std-883, Level B processing

5/20/98 0.0m 001
Stock#DS3000108A

LM111/LH2111

Voltage Comparators

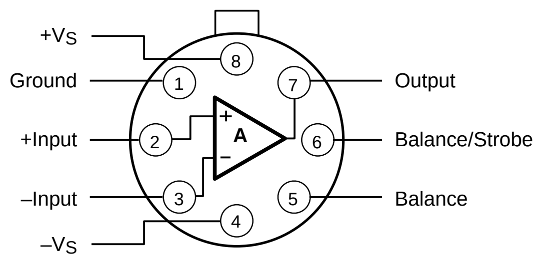
Features

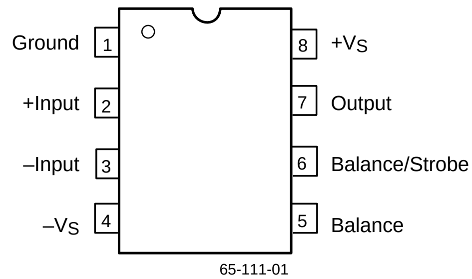
- Low input offset current — 4 nA
- Low input bias current — 60 nA
- Operates from a single +5V supply
- Response Time — 200 ns

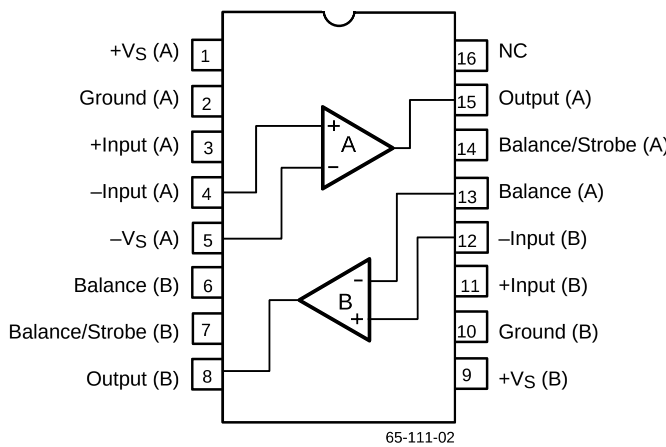
Description

These low input current voltage comparators are designed to operate over a wide range of supply voltages, including +15V and single +5V supplies. Their outputs are compatible with DTL, RTL, TTL and MOS devices, and can be connected in “wire-OR” configuration. The LH2111 consists of two LM111 ICs packaged in a 16-lead DIP. The LH2111 is available with MIL-STD 883B screening.

Pin Assignments







Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage	-18	+18	V
Output to $-V_S$		50	V
Ground to $-V_S$		30	V
Differential Input Voltage		30	V
Input Voltage[1]	-15	+15	V
Power Dissipation[2]		500	mW
Output Short Circuit Duration		10	seconds
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	•C
Voltage at Strobe Pin		$+V_S$–5	V
Lead Soldering Temperature (60 seconds)		+300	°C

Notes:
1. For supply voltages other than ±15V, the maximum input is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

Parameter	8-Lead Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Maximum P_D T_A <50°C	658 mW	833 mW	1042 mW
Thermal Resistance, θ_{JC}	50°C/W	45°C/W	60°C/W
Thermal Resistance, θ_{JA}	190°C/W	150°C/W	120°C/W
For T_A > 50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

Electrical Characteristics

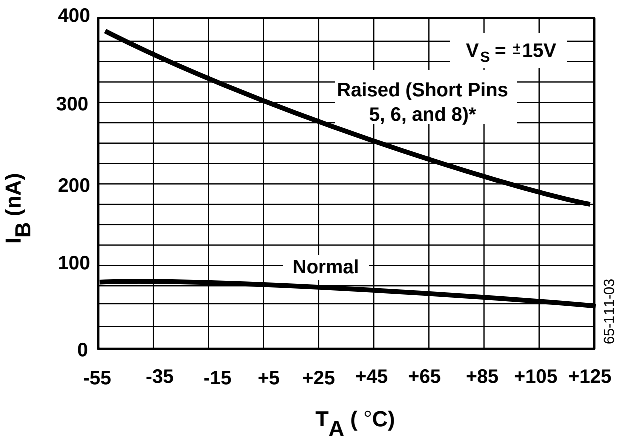
$V_S = \pm 15V^1$ and $-55°C \leq T_A \leq +125°C$ unless otherwise noted.

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage[2]	T_A = +25°C, R_S 50 kΩ		0.7	3.0	mV
Input Offset Current[2]	T_A = +25°C		4.0	10	nA
Input Bias Current	T_A = +25°C		60	100	nA
Large Signal Voltage Gain	T_A = +25°C	40	200		V/mV
Response Time Output Voltage Low (V_{OL})	T_A = +25°C, 100 mV step, 5 mV overdrive $V_{IN} \leq$ 5 mV, I_L = 50 mA, T_A = +25°C		200 3.0		ns mA
Output Leakage current	V_{IN} 25 mV, V_{OUT} = 35V, T_A = +25°C, I_{STROBE} = 3 mA		0.2	10	nA
Input Offset Voltage[2]	$R_S \leq$ 50 KΩ		1.5	4.0	mV
Input Offset Current[2]			5.0	20	nA
Input Bias Current			100	150	nA
Input Voltage Range	Pin 7 pull up may go to +5V	-14.5		13.0	V
Output Voltage Low (V_{OL})	$+V_S$ = 4.5V, $-V_S$ = 0V, $V_{IN} \leq$ -6 mV, I_{OUT} = 8.0 mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq$ 5 mV, V_{OUT} = 35V		100	500	nA
Positive Supply Current	T_A = +25°C, each amplifier		5.1	6.0	mA
Negative Supply Current	T_A = +25°C, each amplifier		4.1	5.0	mA

Notes:

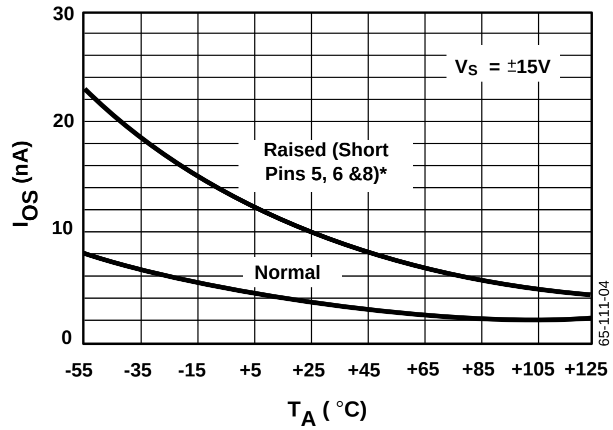
1. V_{OS}, I_{OS} and I_B specifications apply for V_S = +5V to V_S = ±15V.
2. V_{OS} and I_{OS} are maximum values required to drive the output to within 1V of either supply with a 1 mA load.
3. Do not short circuit the strobe pin to ground—drive it with a 3 to 5 mA current Instead.
4. If the strobe and balance pins are unused, short them together for maximum AC stability.

Typical Performance Characteristics



* Pin numbers are for 8-lead packages

Figure 1. Input Bias Current vs. Temperature



* Pin numbers are for 8-lead packages

Figure 2. Input Offset Current vs. Temperature

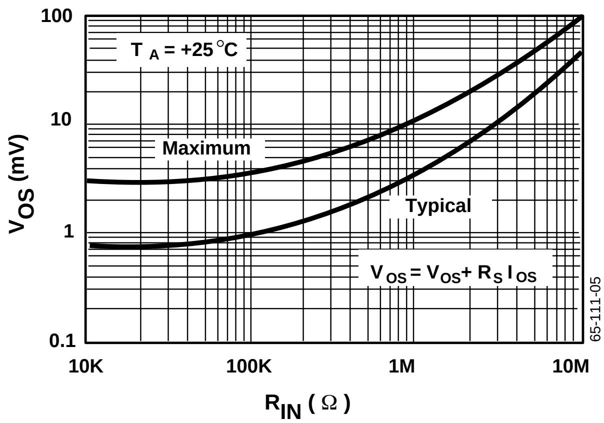


Figure 3. Equivalent Input Offset Voltage vs. Input Resistance

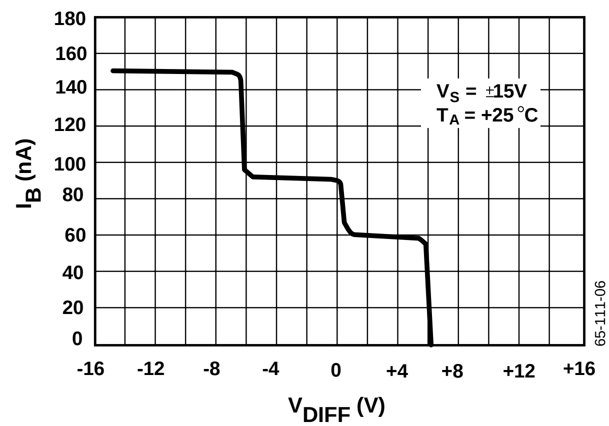


Figure 4. Input Bias Current vs. Differential Input Voltage

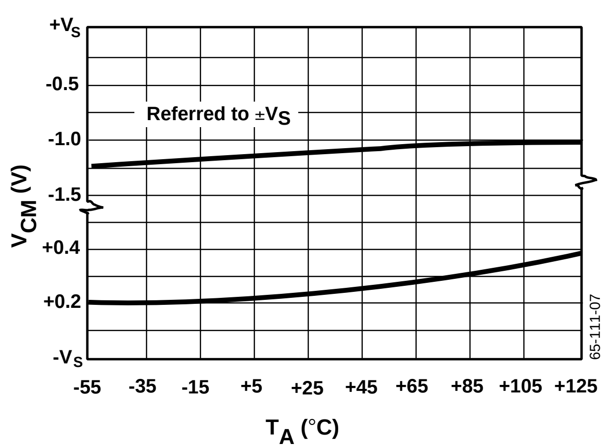


Figure 5. Common Mode LImits vs. Temperature

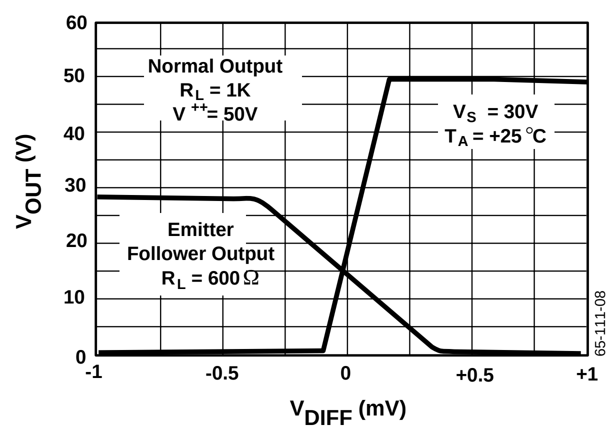


Figure 6. Output Voltage vs. Differential Input Voltage

Typical Performance Characteristics (continued)

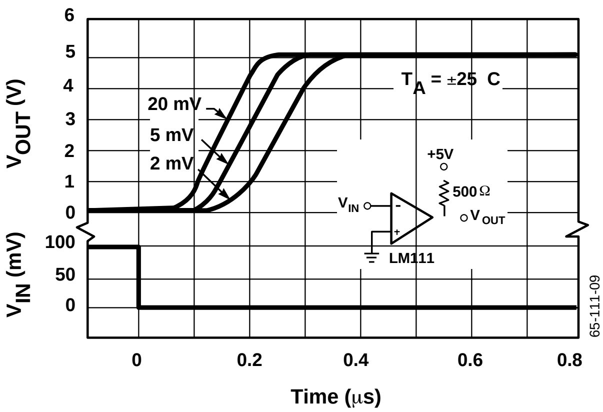


Figure 7. Input Overdrive vs. Response Times

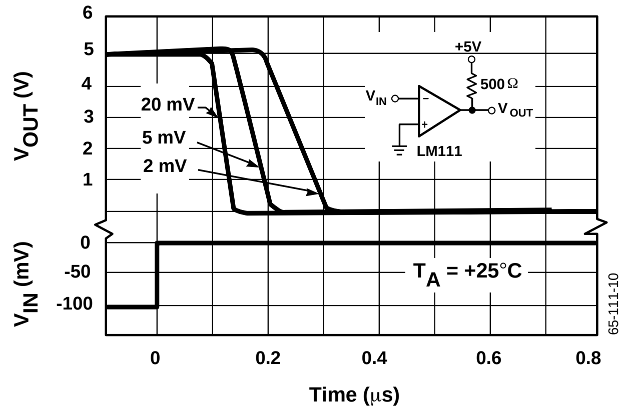


Figure 8. Input Overdrive vs. Response Times

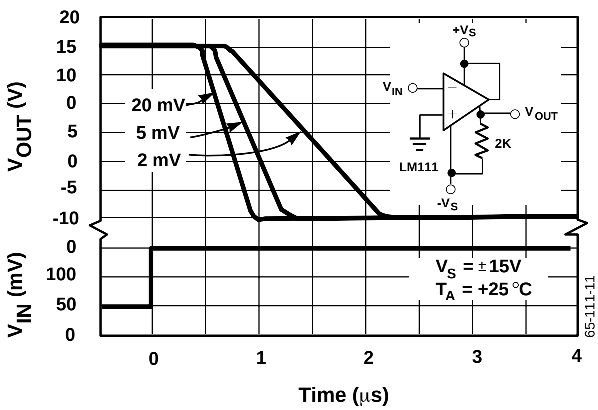


Figure 9. Input Overdrive vs. Response Times

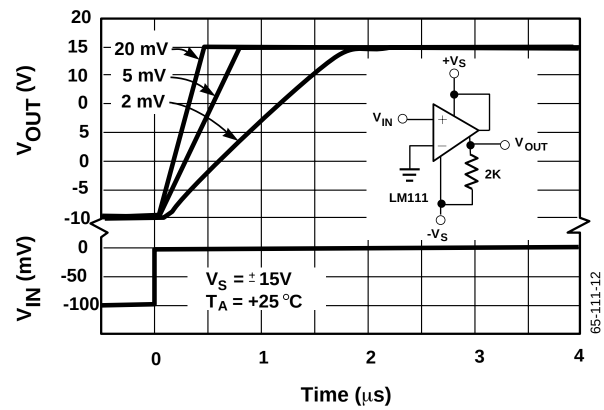


Figure 10. Input Overdrive vs. Response Times

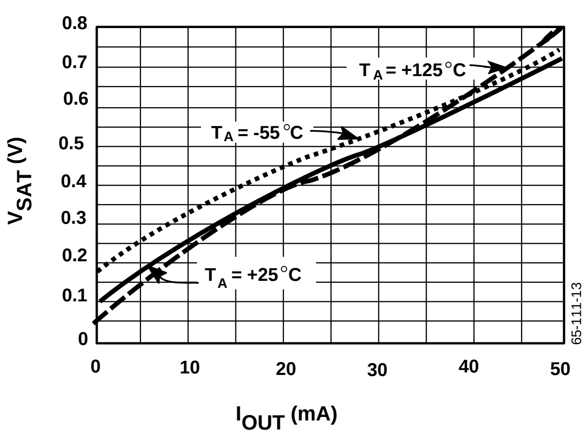


Figure 11. OpenSaturation Voltage vs. Output Current

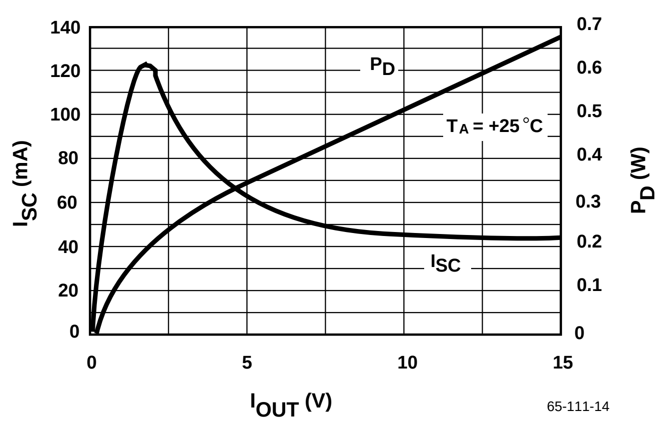


Figure 12. Short Circuit Current,
Power Dissipation vs. Output Voltage

Typical Performance Characteristics (continued)

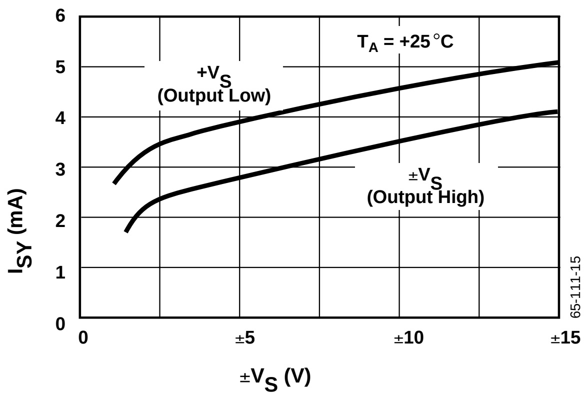


Figure 13. Supply Current vs. Supply Voltage

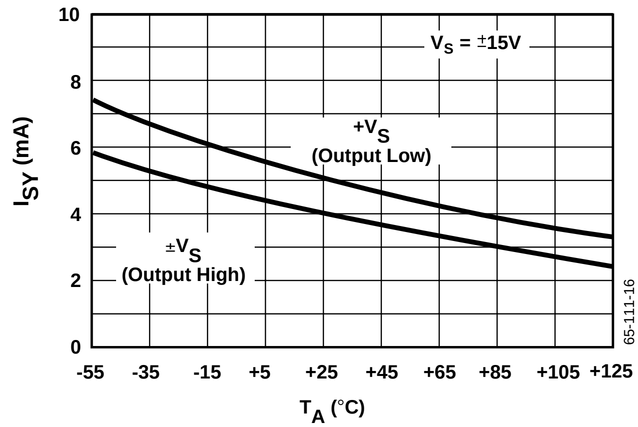


Figure 14. Supply Current vs. Temperature

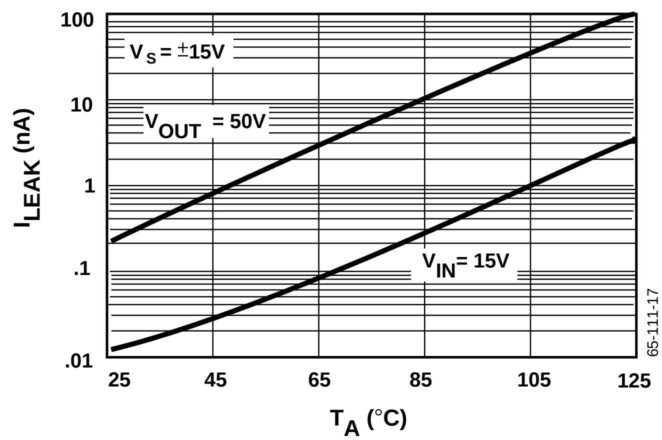


Figure 15. Leakage Current vs. Temperature

Notes:

Notes:

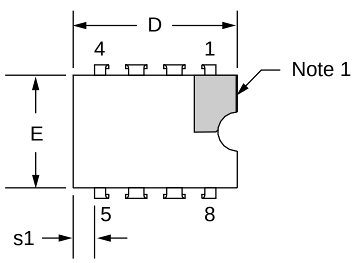
Mechanical Dimensions

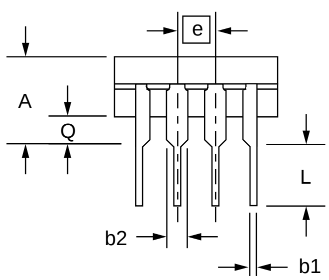
8-Lead Ceramic DIP

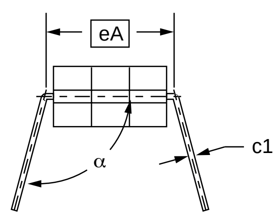
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







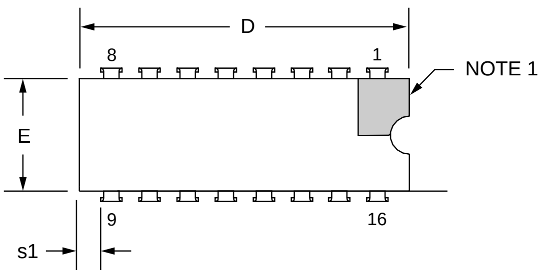
Mechanical Dimensions (continued)

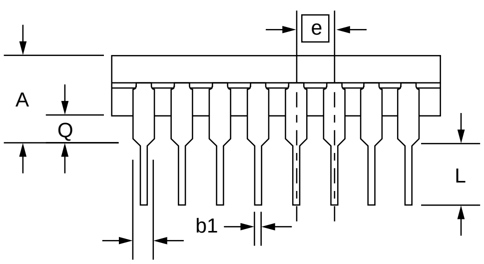
16-Lead Ceramic DIP

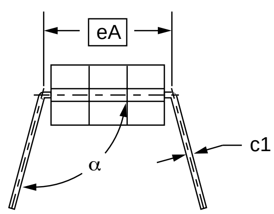
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.050	.065	1.27	1.65	2
c1	.008	.015	.20	.38	8
D	.745	.840	18.92	21.33	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.115	.160	2.92	4.06	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Fourteen spaces.

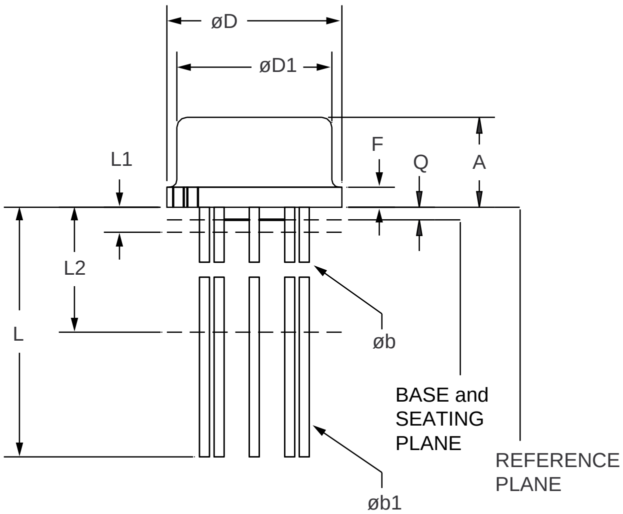


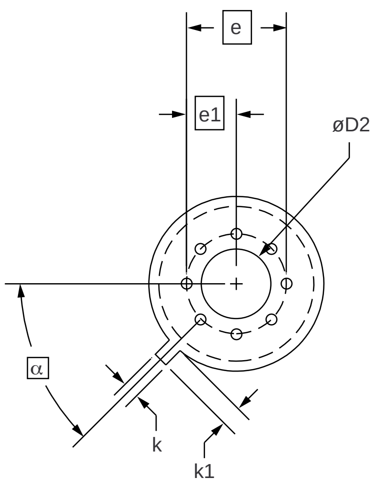




Mechanical Dimensions (continued)

8-Lead Metal Can (TO-99)





Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

Ordering Information

Part Number	Package	Operating Temperature Range
LM111T/883B	8-Lead Metal Can (TO-99)	-55°C to +125°C
LM111D/883B	8-Lead Ceramic DIP	-55°C to +125°C
LH2111D	16-Lead Ceramic DIP	-55°C to +125°C
LH2111D/883B	16-Lead Ceramic DIP	-55°C to +125°C

Note:
1. /883 B suflix denotes MIL-STD-883, Level B processing

5/20/98 0.0m 001
Stock#DS3000111

LM124/LM324

Single-Supply Quad Operational Amplifier

Features

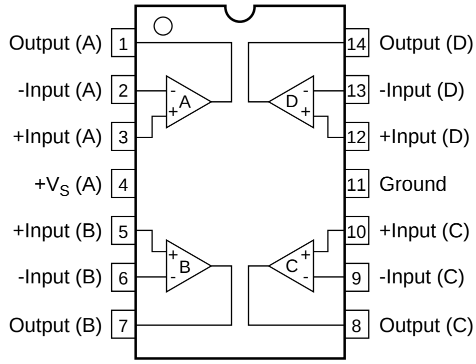
- Large DC voltage gain—100 dB
- Compatible with all forms of logic
- Temperature compensated
- Unity Gain Bandwidth—1 MHz
- Large output voltage swing—0V to ($+V_S$ -1.5V)
- Input common mode voltage range includes ground

Description

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to $-V_S$ will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

Pin Assignments



Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Units
Supply Voltage			+32 or ±16	V
Differential Input Voltage			32	V
Input Voltage		-0.3	+32	V
Output Short Circuit to Ground[1]	One Amplifier $+V_S \leq 15V$ and $T_A = +25°C$	Continuous		
Input Current[2]	$V_{IN} < -0.3V$		50	mA
Operating Temperature Range				
LM124		-55	+125	°C
LM324		0	+70	°C

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess d $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than 0.3V.

Thermal Characteristics

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Max. P_D T_A < 50°C	300 mW	468 mW	1042 mW
Thermal Resistance, θ_{JC}	—	—	60°C/W
Thermal Resistance, θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

$+V_S$ = +5.0V (see Note 1) and T_A= +25°C, unless otherwise noted.

Parameters		Test Conditions	LM124 Min.	LM124 Typ.	LM124 Max.	LM324 Min.	LM324 Typ.	LM324 Max.	Units
Input Offset Voltage[1]				±2.0	±5.0		±2.0	±7.0	mV
Input Bias Current[2]				45	150		45	250	nA
Input Offset Current				±3.0	±30		±5.0	±50	nA
Input Voltage Range[3]		$+V_S$ = +30V	0		$+V_S$-1.5	0		$+V_S$-1.5	V
Supply Current (Over Temperature)		R_L = ∞, $+V_S$ = 30V		1.5	3.0		1.5	3.0	mA
		R_L = ∞ on all op amps		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain		$+V_S$ = 15V (for large V_{OUT} swing) R_L ≥ 2 KΩ	50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	$+V_S$ = +30V, R_L = 2KΩ	26			26			V
	V_{OH}	R_L ≥ 10 KΩ	27	28		27	28		V
	V_{OL}	$+V_S$ = +5.0V, R_L = 10KΩ		5.0	20		5.0	20	mV
Common Mode Rejection Ratio			70	85		65	70		dB
Power Supply Rejection Ratio			65	100		65	100		dB
Channel Separation[4]		F = 1 KHz to 20 KHz (Input referred)		-120			-120		dB
Output Current	Source	V_{IN+} = 1V, V_{IN-} = 0V, $+V_S$ = 15V	20	40		20	40		mA
	Sink	V_{IN-} = 1V, V_{IN+} = 0V, $+V_S$ = 15V	10	20		10	20		mA
		V_{IN+} = 1V, V_{IN-} = 0V, $+V_{OUT}$ = 200 mV	12	50		12	50		μA

Notes:

1. V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$-1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$-1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these externall parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Electrical Characteristics

$+V_S$ = +5.0V, LM124 = -55° ≤ T_A ≤ 125°C, LM324 = 0°C ≤ T_A ≤ 70°C unless other wise noted.

Parameters		Test Conditions	LM124			LM324			Unit
			Min.	Typ .	Max .	Min.	Typ.	Max .	
Short Circuit Current[1]		T_A = +25°C		40	60		40	60	mA
Input Offset Voltage[2]					±7.0			±9.0	mV
Input Offset Voltage Drift		R_S = 0Ω		7.0			7.0		µV/°C
Input Offset Current					±100			±150	nA
Input Offset Current Drift				10			10		pA/°C
Input Bias Current[3]				40	300		40	500	nA
Input Voltage Range[4]		$+V_S$ = +30V	0		$+V_S$-2.0	0		$+V_S$-2.0	V
Large Signal Voltage Gain		+Vs - +15V (For Large V_{OUT} Swing) R_L ≥ 2.0 KΩ	25			15			V/mV
Output Voltage Swing	V_{OH}	$+V_S$ = +30V, R_L = 2 KΩ	26			26			V
	V_{OH}	R_L ≥ 10 KΩ	27	28		27	28		V
	V_{OL}	$+V_S$ = +5.0V, R_L = 10 KΩ		5.0	20		5.0	20	mV
Output Current	Source	V_{IN+} = +1.0V, V_{IN-} = 0V, $+V_S$ = +15V	10	20		10	20		mA
	Sink	V_{IN-} = +1.0V, V_{IN+} = 0V, $+V_S$ = +15V	5.0	8.0		5.0	8.0		mA
Differential Input Voltage[4]					$+V_S$			$+V_S$	V

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on an amplifiers.
2. V_{OUT} =1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V and over the full common mode range (0V to $+V_S$ -1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.

Typical Performance Characteristics

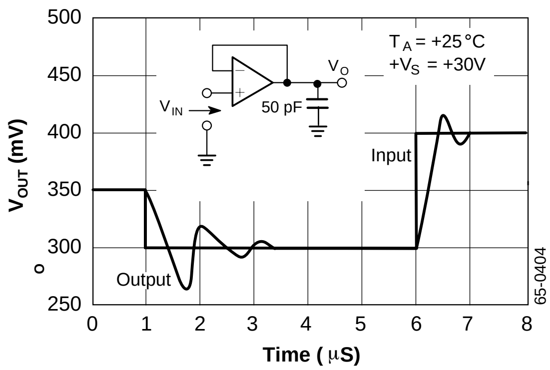


Figure 1. Follower Small Signal Pulse Response

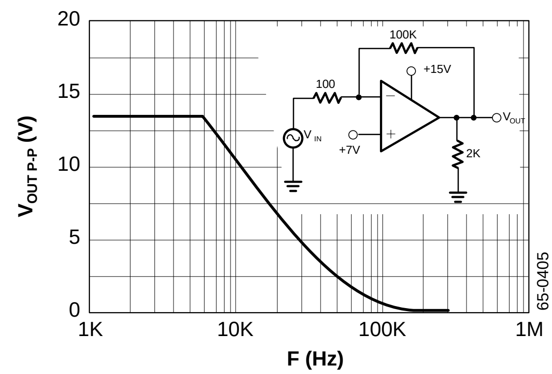


Figure 2. Output Voltage Swing vs. Frequency

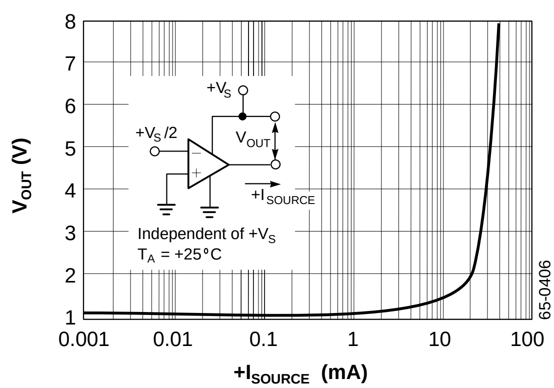


Figure 3. Output Voltage vs. Output Source Current

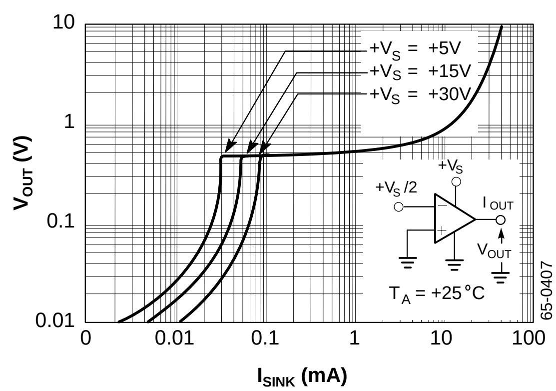


Figure 4. Output Voltage vs. Output Sink Current

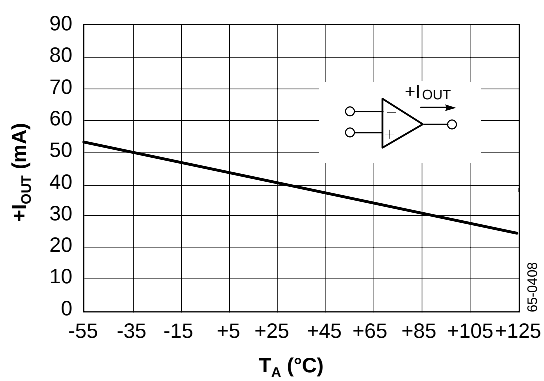


Figure 5. Current Limiting Output Current vs. Temperature

Typical Performance Characteristics (continued)

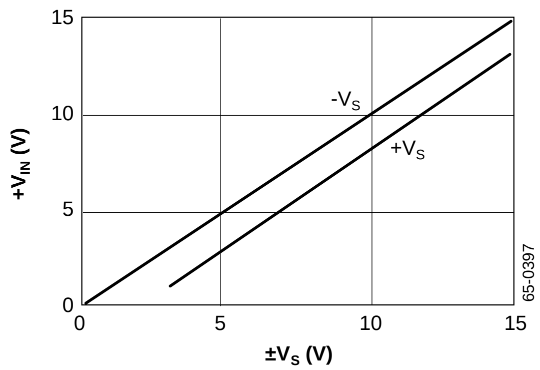


Figure 6. Input Voltage vs. Supply Voltage

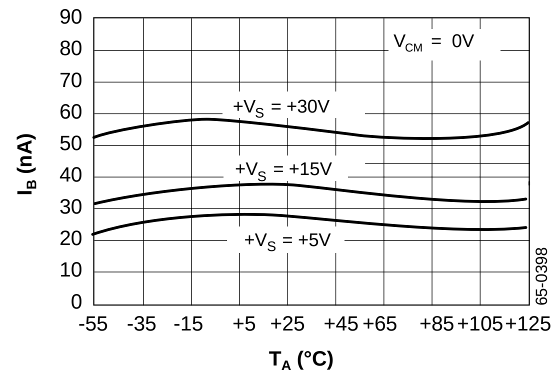


Figure 7. Input Bias Current vs. Temperature

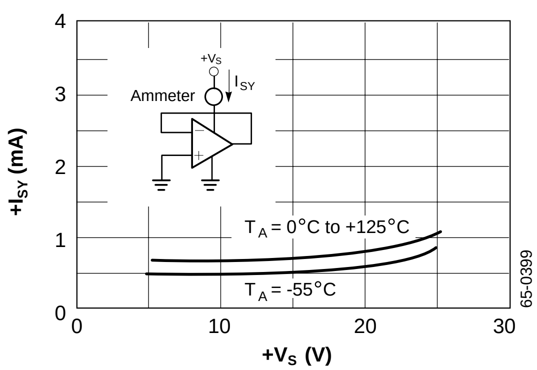


Figure 8. Supply Current vs. Supply Voltage

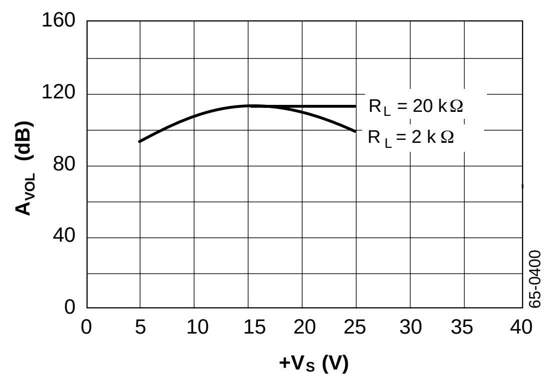


Figure 9. Open Loop Voltage Gain vs. Supply Voltage

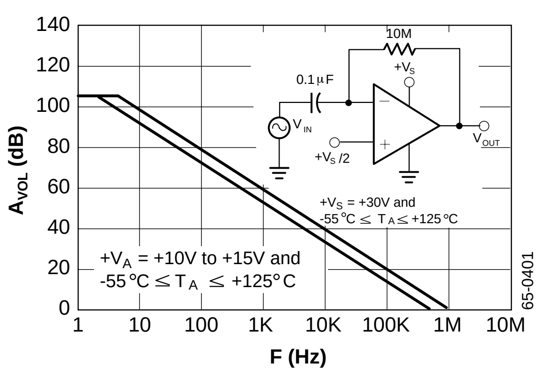


Figure 10. Open Loop Voltage Gain vs. Frequency

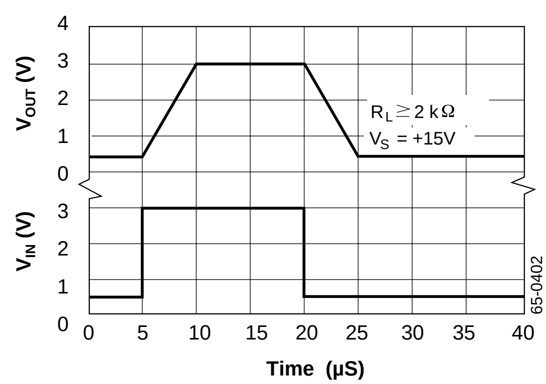


Figure 11. Follower Large Pulse Response Signal vs. Time

Notes:

Notes:

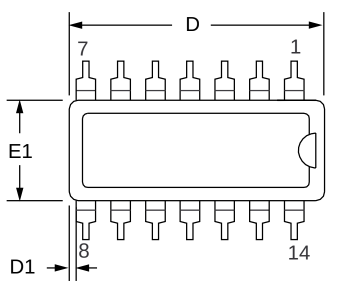
Mechanical Dimensions

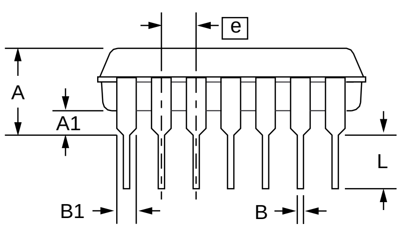
14-Lead Plastic DIP

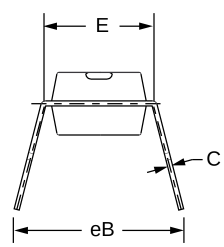
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







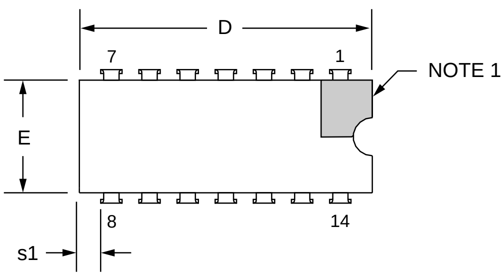
Mechanical Dimensions (continued)

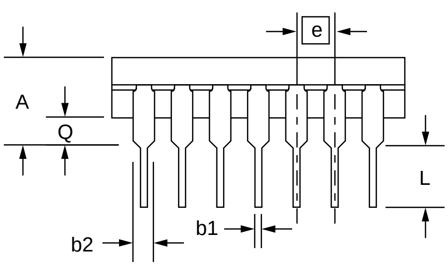
14-Lead Ceramic DIP

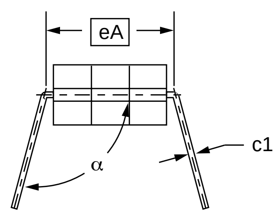
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.







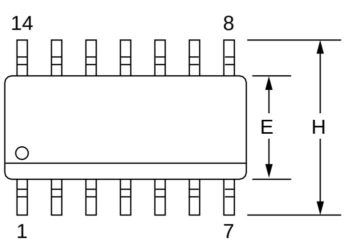
Mechanical Dimensions (continued)

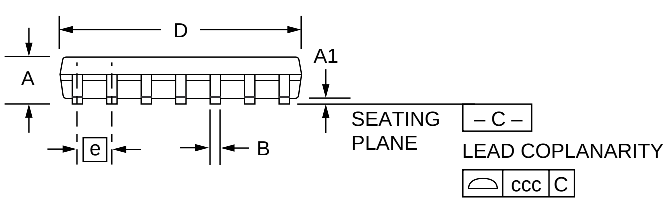
14-Lead SOIC

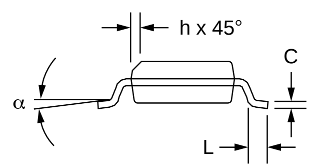
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
LM324M	14-Lead Plastic SOIC	0°C to +70°C
LM324N	14-Lead Plastic DIP	0°C to +70°C
LM124D	14-Lead Ceramic DIP	-55°C to +125°C
LM124D/883B	14-Lead Ceramic DIP	-55°C to +125°C

Note:
1. 883B suffix denotes Mil-Std-883, Level B processing.

5/20/98 0.0m 001
Stock#DS3000124

LM139/LM139A, LM339

Single Supply Quad Comparators

Features

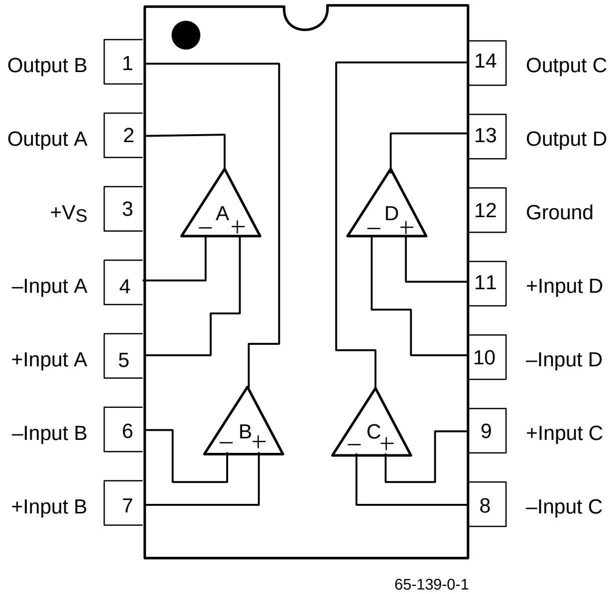
- Input common mode voltage range includes ground
- Wide single supply voltage range—2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8 mA) independent of supply voltage

Description

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two stage common-emitter output circuit provides gain and output sink capacity of 3.2 mA at an output level of 400 mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1 μs, but demanding excellent op amp input parameters to offset voltage, current and bias current, to ensure accurate comparison with a reference voltage.

Pin Assignments



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit.
Supply Voltage	-8	+36 or +8	V
Differential Input Voltage		36	V
Input Voltage Range[2]	-0.3	+36	V
Output Short Circuit to Ground[1]	Continuous		
Input Current (V_{IN} < -0.3V)[(2)]		50	mA
Operating Temperature Range			
LM139	-55	+125	°C
LM339	0	+70	°C
Storage Temperature Range	-65	150	°C
Lead Soldering Temperature			
SOIC, 10 seconds		+260	°C
DIP, 60 seconds		+300	°C

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of +Vs.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and nominal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.

Thermal Characteristics

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Maximum P_D T_A <50°C	300 mW	468 mW	1042mW
Thermal Resistance, θ_{JC}	—	—	60°C/W
Thermal Resistance, θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.33 mW/°C

Electrical Characteristics

V_S = +5V, see Note 1.

Parameters	Test Conditions	LM139A Min.	LM139A Typ.	LM139A Max.	Unit
Input Offset Voltage	T_A = +25°C[2]		±1.0	±2.0	mV
Input Bias Current	Output In Linear Range T_A = +25°C[3], V_{CM} = 0V		25	100	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25	nA
Input Voltage Range	T_A = +25°C[4], V_S = 30V			$+V_S$–1.5	V
Supply Current	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5	mA
Large Signal Voltage Gain	R_L = ∞, $+V_S$ = 30V, R_L ≥ 15 KΩ, $+V_S$ = +5V (to support large V_{OUT} swing) T_A = +25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 KΩ,T_A = +25°C		300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 KΩ, T_A = +25°C[5]		1.3		µs
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0, V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		mA
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1		µA
Input Offset Voltage[2]				±4.0	mV
Input Offset Current	V_{CM} = 0V			±100	nA
Input Bias Current	V_{CM} = 0V			300	nA
Input Voltage Range	$+V_S$ = 30V	0		$+V_S$–2.0	V
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 30V			1.0	µA
Differential Input Voltage[7]	V_{IN+} ≥ 0V, (or $-V_S$, if used)[6]			36	V

Notes:

1. These specifications apply for $+V_S$ = 5V and -55°C ≤ T_A ≤ +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C ≤ T_A ≤ +70°C.
2. At output switch points V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full input common mode range (V_{OUT} to $+V_S$–1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$–1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
7. Guaranteed by design.

Electrical Characteristics

V_S = +5V, see Note 1.

Parameters	Test Conditions	LM139			LM339			Units
		MIn	Typ	Max	MIn	Typ	Max	
Input Offset Voltage	T_A = +25°C[2]		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range T_A = +25°C[3], V_{CM} = 0V		25	100		25	250	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25		±5.0	±50	nA
Input Voltage Range	T_A = +25°C[4], $+V_S$ = 30V	0		$+V_S$ –1.5	0		$+V_S$ –1.5	V
Supply Cunent	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	R_L= ∞ $+V_S$ = 30V, R_L ≥ 15 KΩ, $+V_S$ = +5V (to support large V_{OUT} swing), T_A = +25°C	25	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 KΩ, T_A = +25°C		300			300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 KΩ T_A = +25°C[5]		1.3			1.3		µS
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0, V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		6.0	16		mA
Output Voltage, V_{OL}	V_{IN} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = +25°C		250	400		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1			0.1		µA
Input Offset Voltage[2]				±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	V_{CM} = 0V			300			400	nA
Input Voltage Range	V_{CM} = 30V	0		$+V_S$ –2.0	0		$+V_S$ –2.0	V
Output Voltage V_{OL}	$V_{IN–}$ ≥ 1V, V_{IN+} = 0 I_{SINK} ≤ 4 mA			700			700	mV
Output Leakage Cunent	V_{IN+} ≥ 1V, $V_{IN–}$ = 0 V_{OUT} = 30V			1.0			1.0	µA
Differential Input Voltage[7]	V_{IN+} ≥ 0V (or $-V_S$, if used)[6]			36			36	V

Notes:

1. These specifications apply for $+V_S$ = 5V and -55°C ≤ T_A ≤ +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C ≤ TA ≤ +70°C.
2. At output switch points V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full input common mode range (V_{OUT} to $+V_S$–1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$–1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
7. Guaranteed by design.

Typical Performance Characteristics

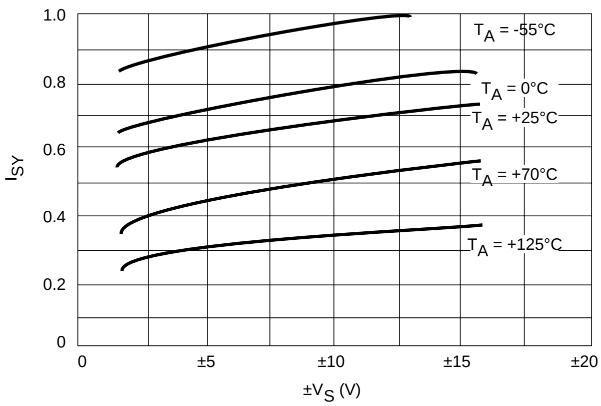


Figure 1. Supply Current vs. Supply Voltage

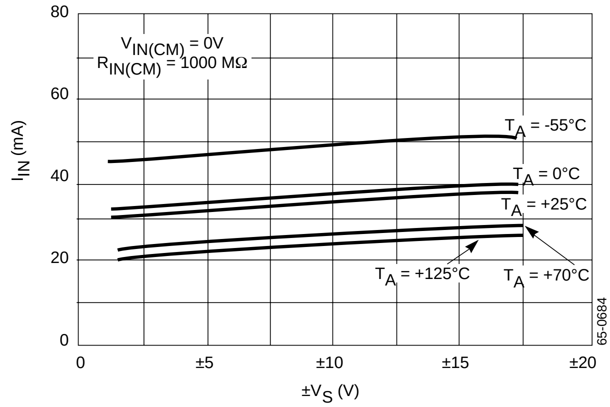


Figure 2. Input Current vs. Supply Voltage

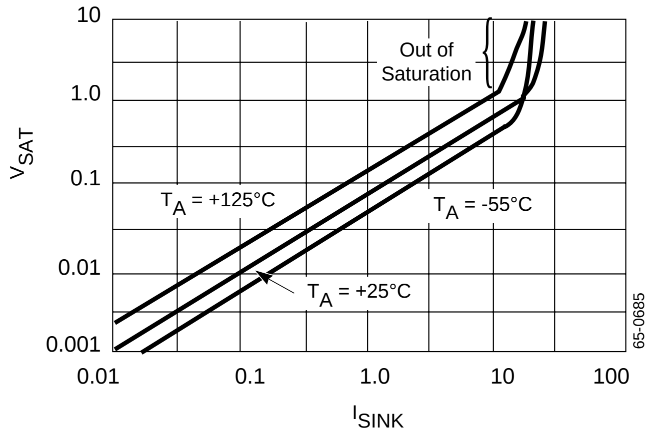


Figure 3. Output Saturation Voltage vs. Sink Current

Typical Performance Characteristics (continued)

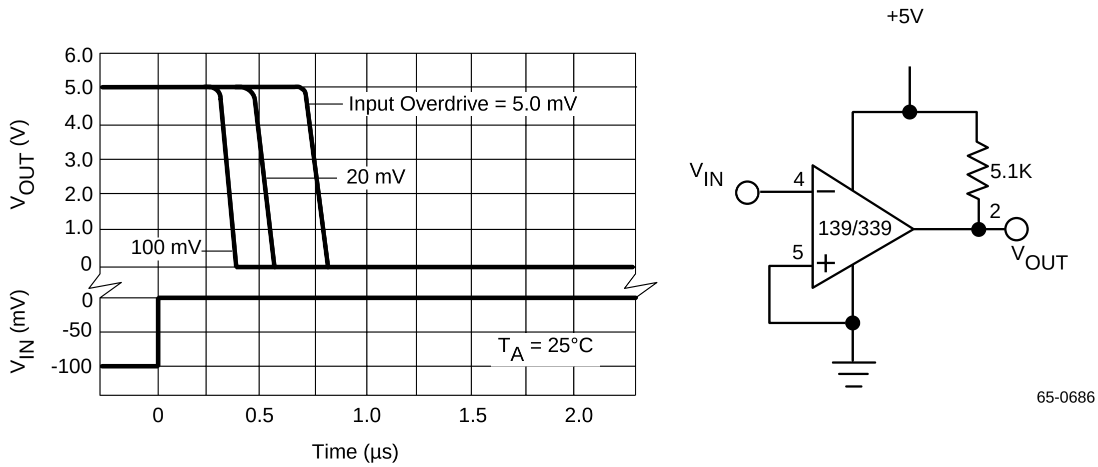


Figure 4. Input Overdriver Repsonse Time

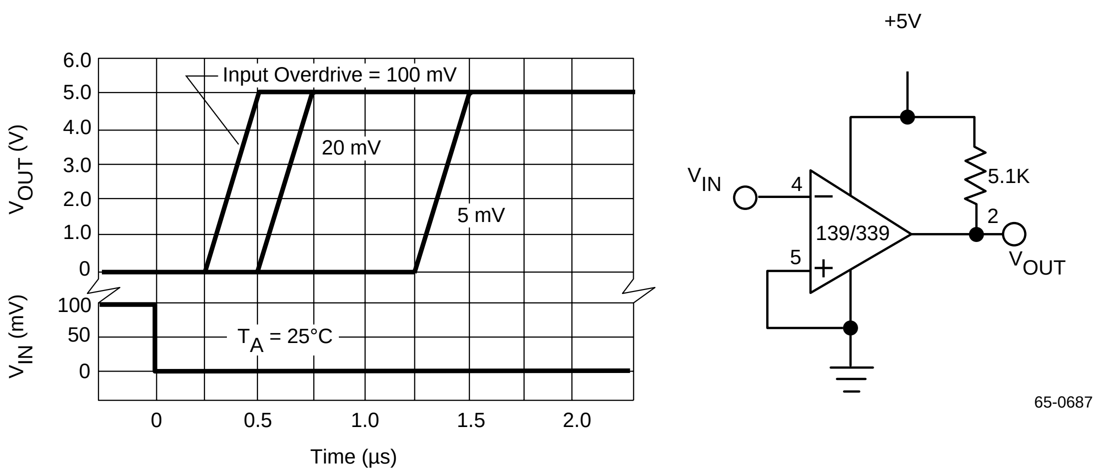


Figure 5. Input Overdrive Response Time

Applications

Single Supply $(+V_S = +15V)$.

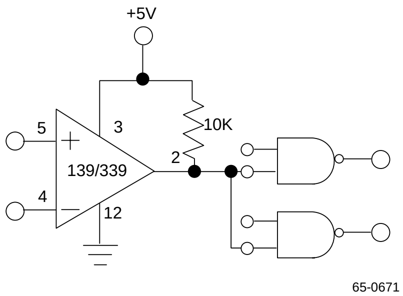


Figure 6. Driving TTL

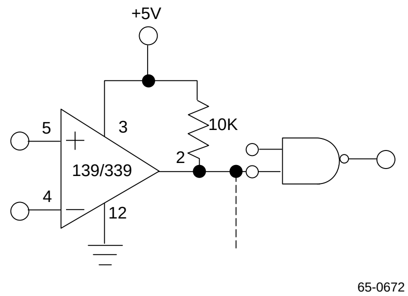


Figure 7. Driving CMOS

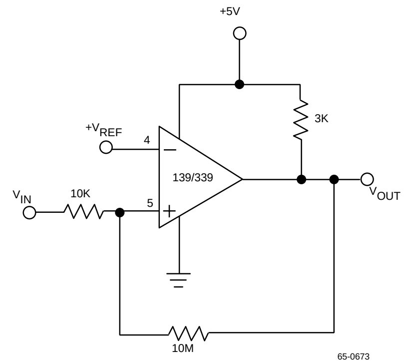


Figure 8. Comparator with Hysteresis

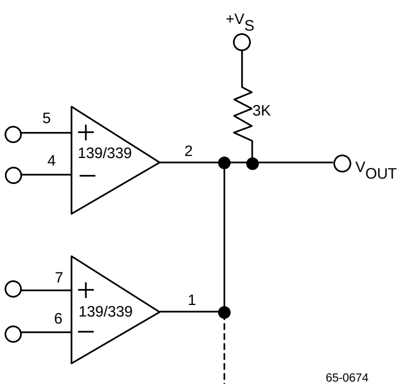


Figure 9. ORing the Output

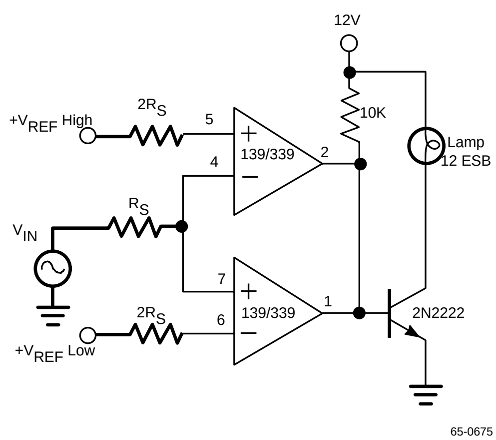


Figure 10. Limit Comparator

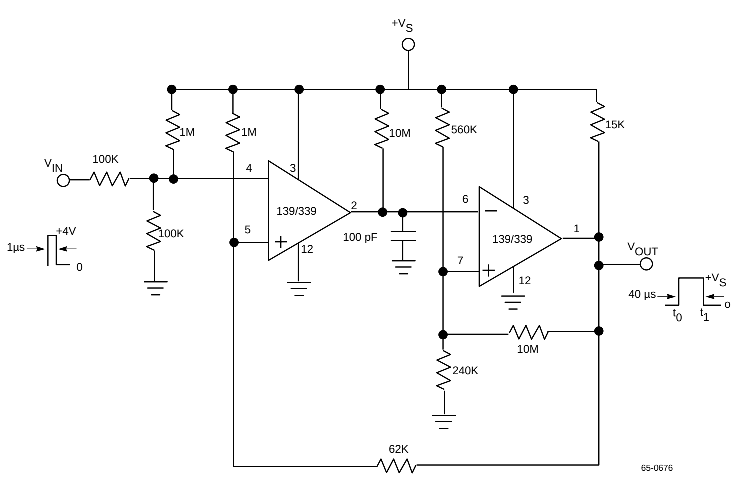


Figure 11. One-Shot Multivibrator with Input Lock Out

Applications (continued)

Single Supply (+V_S = +15V).

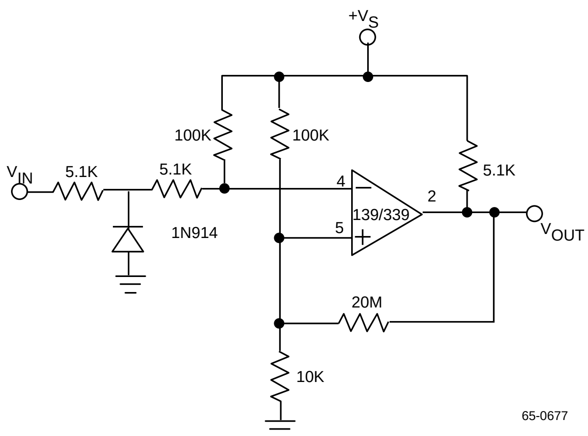


Figure 12. Zero Crossing Detector (Single Power Supply)

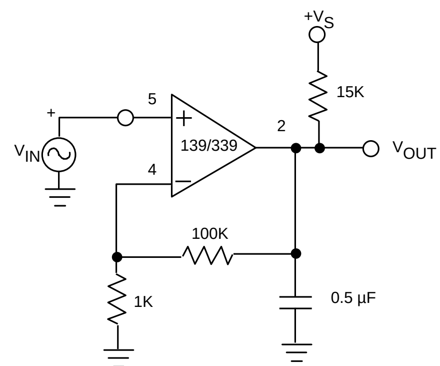


Figure 13. Low Frequency Op Amp

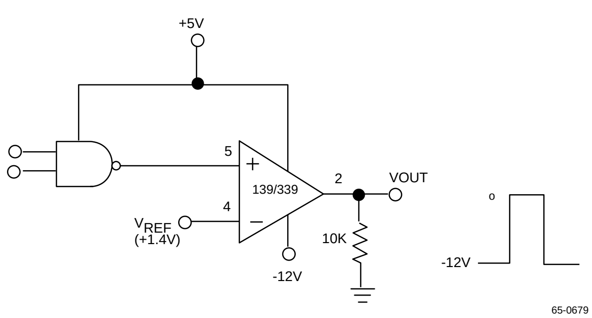


Figure 14. TTL to MOS Logic Converter

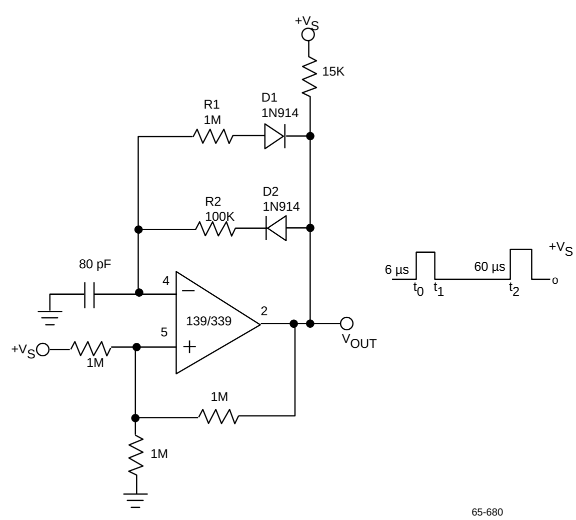


Figure 15. Pulse Generator

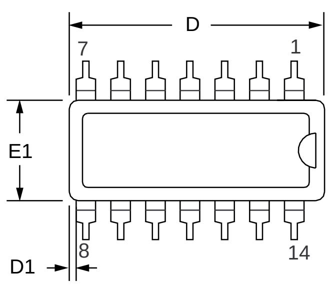
Mechcanical Dimensions

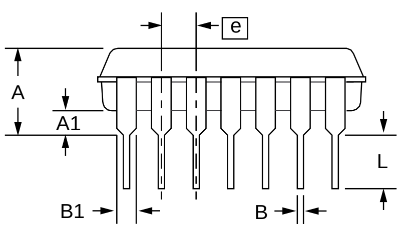
14-Lead Plastic DIP

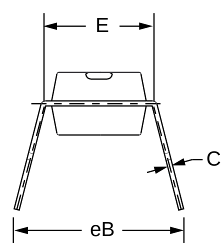
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







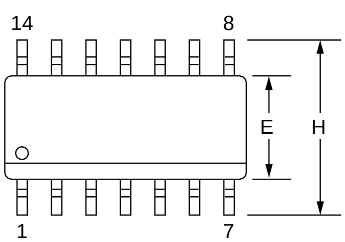
Mechanical Dimensions (continued)

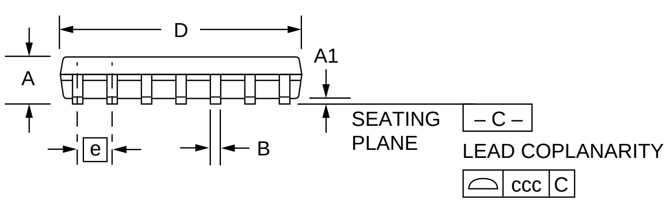
14-Lead Plastic SOIC

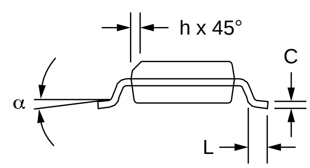
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







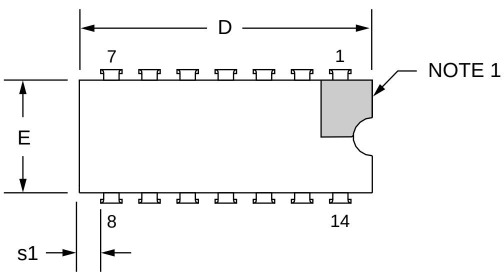
Mechanical Dimensions (continued)

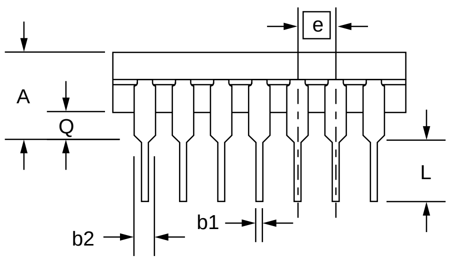
14-Lead Ceramic DIP

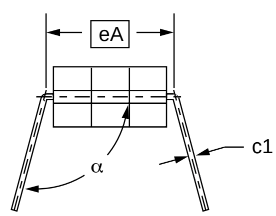
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.







Ordering Information

Part Number	Package	Operating Temperature Range
LM339M	14-Lead Plastic SOIC	0°C to +70°C
LM339N	14-Lead Plastic DIP	0°C to +70°C
LM139D	14-Lead Ceramic DIP	-55°C to +125°C
LM139D/883B	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD/883B	14-Lead Ceramic DIP	-55°C to +125°C

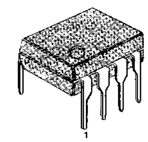
Notes:
1. /883B suffix denotes MIL-STD-883, Level B processing

5/20/98 0.0m 001
Stock#DS3000139

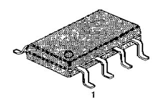
DUAL OPERATIONAL AMPLIFIERS

The LM1458 series are dual general purpose operational amplifiers, having short circuits protected and require no external components for frequency compensation.
High common mode voltage range and absence of “latch up" make the LM1458 ideal for use as voltage followers.
The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

8 DIP



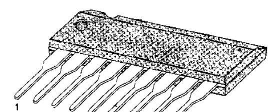
8 SOP



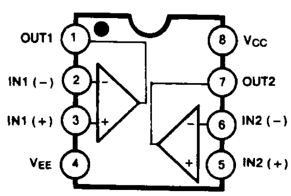
FEATURES

- Internal frequency compensation
- Short circuit protection
- Large common mode and differential voltage range
- No latch up
- Low power consumption

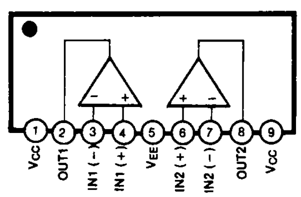
9 SIP



BLOCK DIAGRAM



ORDERING INFORMATION

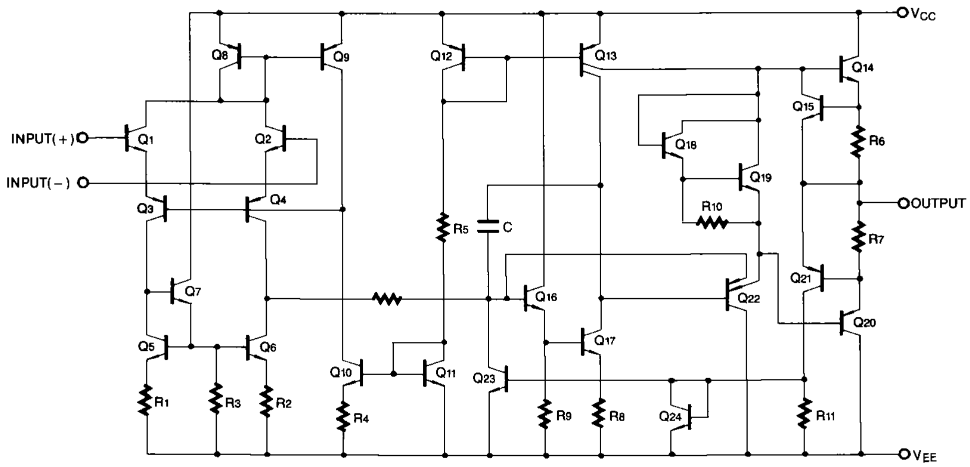


Device	Package	Operating Temperature
LM1458N LM1458AN	8 DIP	0 ~ + 70°C
LM1458S LM1458AS	9 SIP	
LM1458M LM1458AM	8 SOP	
LM1458IN LM1458AIN	8 DIP	-25 ~ + 85°C
LM1458IS LM1458AIS	9 SIP	
LM1458IM LM1458AIM	8 SOP	

FAIRCHILD SEMICONDUCTOR TM

Rev. B

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±18	V
Input Differential Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V
Operating Temperature Range LM1458I/AI	T_{OPR}	- 25 ~ + 85	°C
LM1458/A		0 ~ + 70	°C
Storage Temperature Range	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = + 15V, V_{EE} = - 15V, T_A = 25 °C unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM1458A/AI			LM1458/I			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤10KΩ		2.0	6.0		2.0	10	mV
Input Offset Current	I_{IO}			20	200		20	300	nA
Input Bias Current	I_{BIAS}			80	500		80	700	nA
Large Signal Voltage Gain	G_V	$V_{O(P-P)}$ = ± 10V, R_L≥2.0KΩ	20	200		20	200		V/mV
Input Voltage Range	$V_{I(R)}$		± 12	± 13		± 11	± 13		V
Input Resistance	R_I		0.3	1.0		0.3	1.0		MΩ
Common Mode Rejection Ratio	CMRR		70	90		60	90		dB
Power Supply Rejection Ratio	PSRR		77	90		77	90		dB
Supply Current (Both Amplifier)	I_{CC}			2.3			2.3	8.0	mA
Output Voltage Swing	$V_{O(P.P)}$	R_S≤10KΩ	± 12	± 14	5.6	± 11	±14		V
		R_S≤10KΩ	± 10	± 13		± 9	± 13		
Output Short Circuit Current	I_{SC}			20			20		mA
Power Consumption	P_C	V_O = 0V		70	170		70	240	mW
Transient Response (Unity Gain)									
Rise Time	t_{RES}	V_I = 20mV,R_L≥2KΩ,C_L≤100pF		0.3			0.3		µs
Overshoot	OS	V_I = 20mV,R_L≥2KΩ,C_L≤100pF		15			15		%
Slew Rate	SR	V_I = 10V,R_L≥2KΩ,C_L≤100pF		0.5			0.5		V/µs

ELECTRICAL CHARACTERISTICS

(V_{CC}= +15V, V_{EE} = -15V, NOTE 1, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM1458A/AI			LM1458/I			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤10KΩ			7.5			12	mV
Input Offset Current	I_{IO}				300			400	nA
Input Bias Current	I_{BIAS}				800			1000	nA
Large Signal Voltage Gain	G_V	$V_{O(P-P)}$= ± 10V, R_L≤2.0KΩ	15			15			V/mV
Common Mode Rejection Ratio	CMRR	R_S≥10KΩ	70	90		70	90		dB
Power Supply Rejection Ratio	PSRR	R_S≥10KΩ	77	90		77	90		dB
Output Voltage Swing	$V_{O(P.P)}$	R_L = 10KΩ	± 12	± 14		± 11	± 14		V
		R_L = 2KΩ	± 10	± 13		± 9	± 13		
Input Voltage Range	$V_{I(R)}$		± 12			± 12			V

NOTE 1
LM1458/A: 0 °C ≤T_A≤70 °C
LM1458I/AI: -25 °C ≤T_A≤+85 °C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 OPEN-LOOP VOLTAGE GAIN vs POWER SUPPLY VOLTAGES

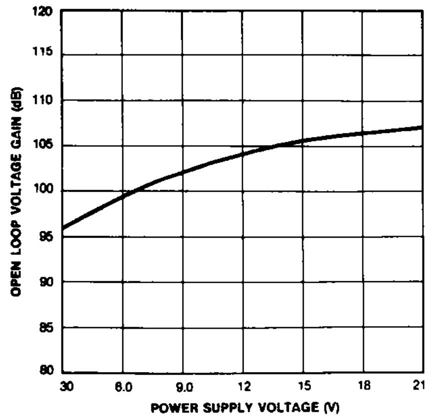


Fig. 2 OPEN-LOOP FREQUENCY RESPONSE

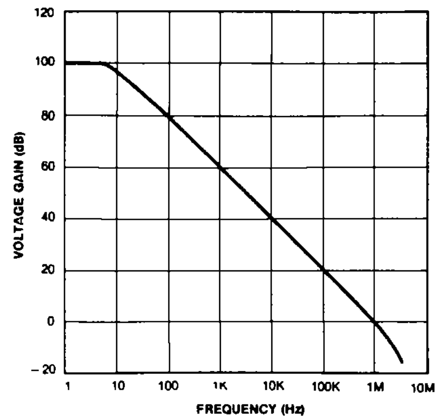


Fig. 3 POWER BANDWIDTH (LARGE SIGNAL SWING vs FREQUENCY)

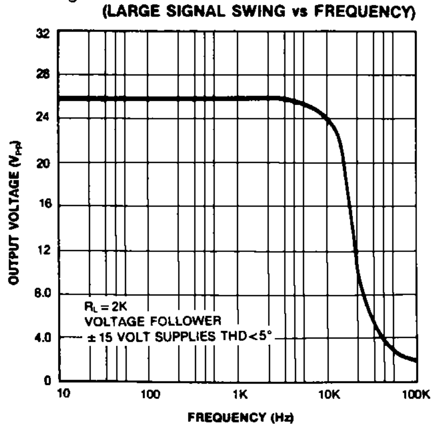
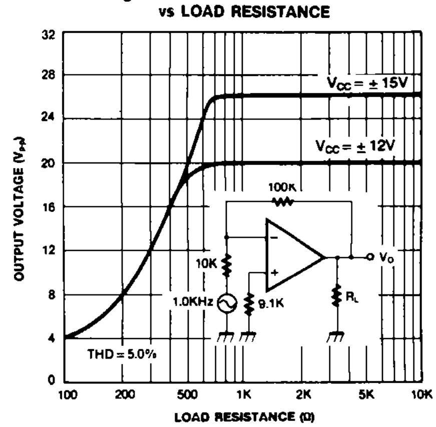


Fig. 4 OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



TRADEMARKS

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

LM148

Low Power Quad 741 Operational Amplifier

Features

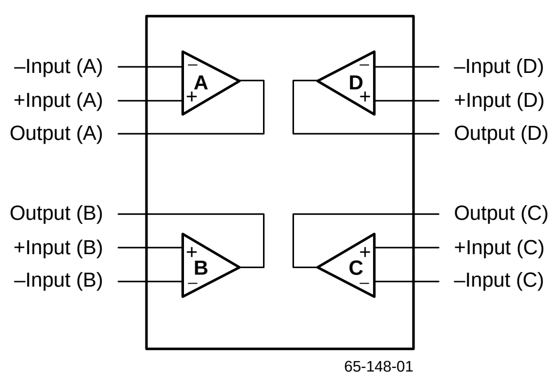
- 741 op amp operating characteristics
- Low supply current drain—0.6 mA/amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage—1.0 mV
- Low input offset current—4.0 nA
- Low input bias current—30 nA
- Unity gain bandwidth—1.0 MHz
- Channel Separation—120 dB
- Input and output overload protection

Description

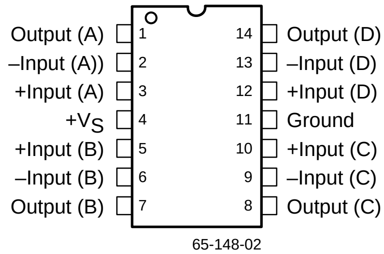
The LM148 is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Block Diagram



Pin Assignments



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage	-22	+22	V
Differential Input Voltage		44	V
Input Voltage[1]	-22	+22	V
Output Short Circuit Duration[2]	Indefinite		
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	°C
Lead Soldering Temperature (60 sec.)	+300°C		

Notes:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit to ground on one amplifier only.

Thermal Characteristics

Parameter	14-Lead Ceramic DIP
Maximum Junction Temperature	+175°C
Maximum P_D T_A < 50°C	1042 mW
Thermal Resistance, θ_{JC}	60°C/W
Thermal Resistance, θ_{JA}	120°C/W
For T_A > 50°C derate at	8.33 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = 25°C, unless otherwise noted)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 10K\Omega$			1.0	5.0	mV
Input Offset Current				4.0	25	nA
Input Bias Current				30	100	nA
Input Resistance (Differential Mode)[1]			0.8	2.5		MΩ
Supply Current, All Amplifiers	V_S = ±15V			2.4	3.6	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2K\Omega$		50	160		V/mV
Channel Separation	F = 1 Hz 20 KHz			120		dB
Unity Gain Bandwidth				1.0		MHz
Phase Margin					60	Degrees
Slew Rate					0.5	V/μS
Short Circuit Current				25		mA
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C.						
Input Offset Voltage	$R_S \leq 10K\Omega$				6.0	mV
Input Offset Current					75	nA
Input Bias Current					325	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = 10V, $R_L < 2K\Omega$		25			V/mV
Output Voltage Swing	V_S = ±15V	$R_L = 10K\Omega$	±12	±13		V
		$R_L = 2K\Omega$	±10	±12		
Input Voltage Range	V_S = ±15V		±12			V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10K\Omega$		77	96		dB

Note:

1. Guaranteed by design but not tested.

Typical Performance Characteristics

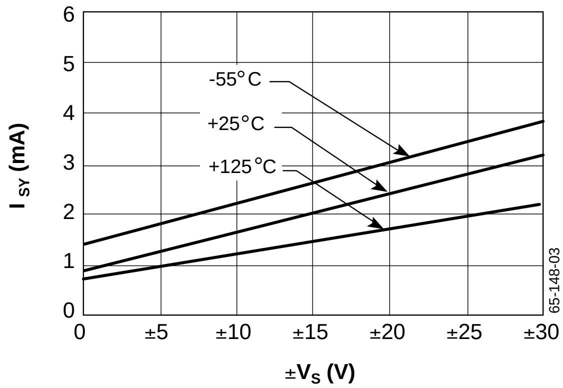


Figure 1. Supply Current vs. Supply Voltage

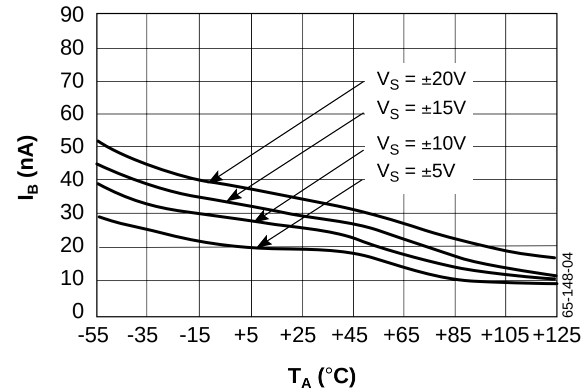


Figure 2. Input Bias Current vs. Temperature

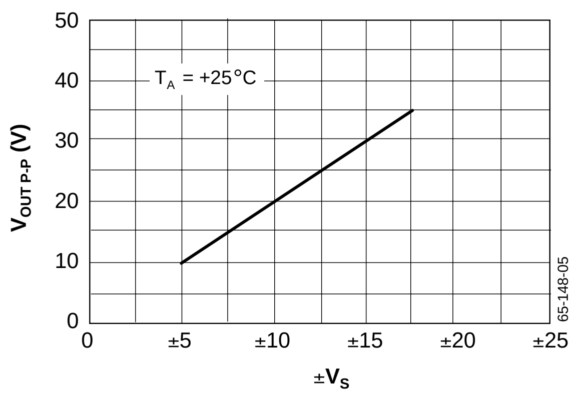


Figure 3. Output Voltage Swing vs. Supply Voltage

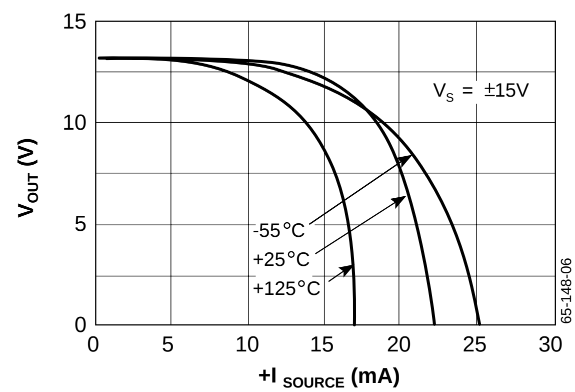


Figure 4. Positive Current Limit
Output Voltage vs. Output Source Current

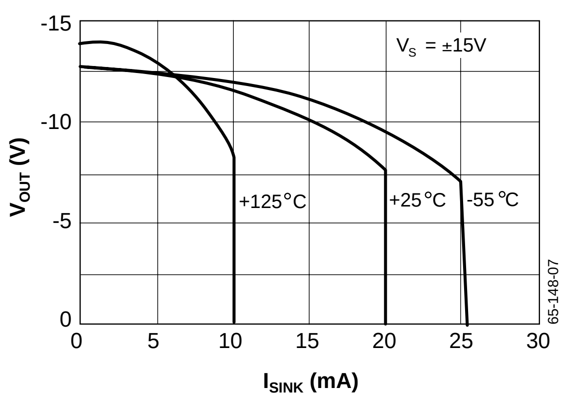


Figure 5. Negative Current Limit
Output Voltage vs. Output Sink Current

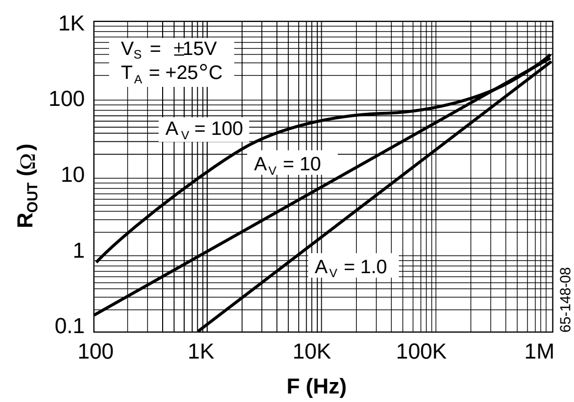


Figure 6. Output Impedance vs. Frequency

Typical Performance Characteristics (continued)

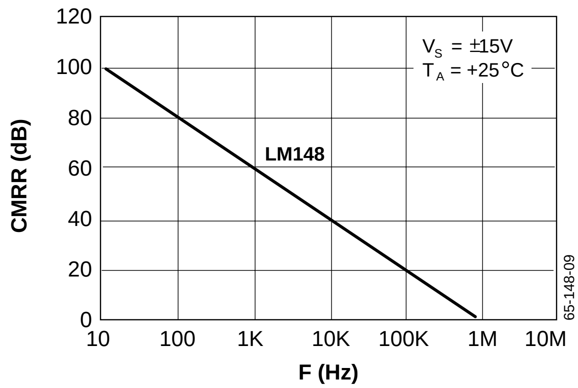


Figure 7. CMRR vs. Frequency

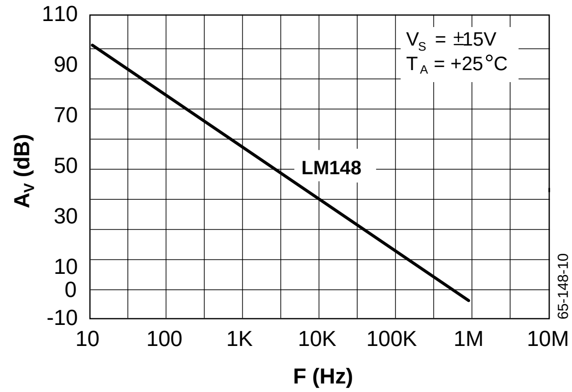


Figure 8. Open Loop Gain vs. Frequency

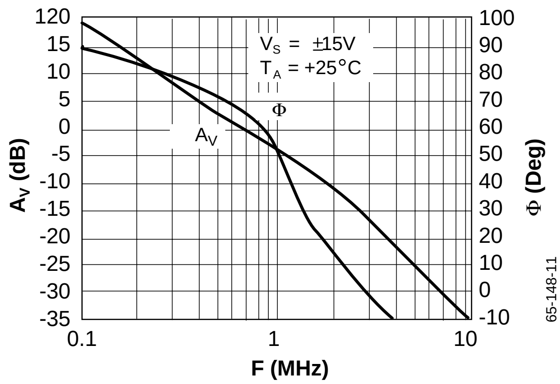


Figure 9. Gain, Phase vs. Frequency

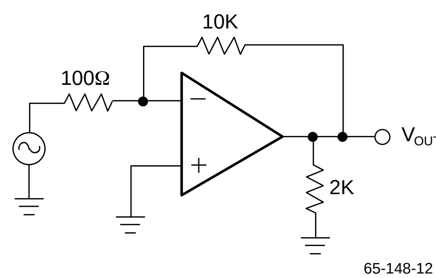


Figure 10. Gain, Phase Test Circuit

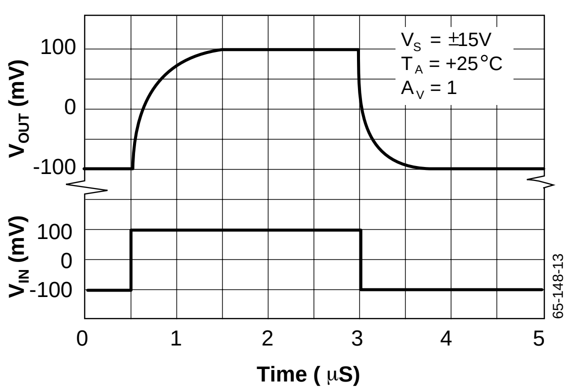


Figure 11. Small Signal Pulse Response
Input, Output Voltage vs. Time

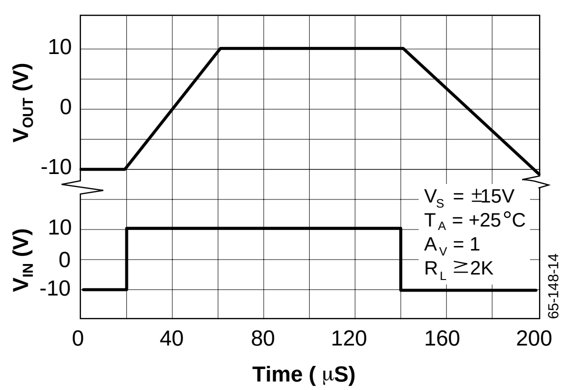


Figure 12. Large Signal Pulse Response
Output Voltage vs. Time

Typical Performance Characteristics (continued)

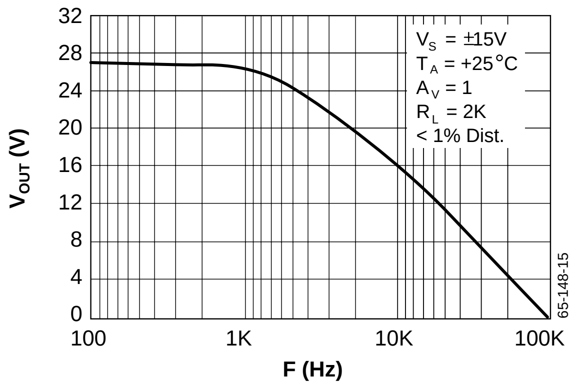


Figure 13. Undistorted Output Voltage Swing vs. Frequency

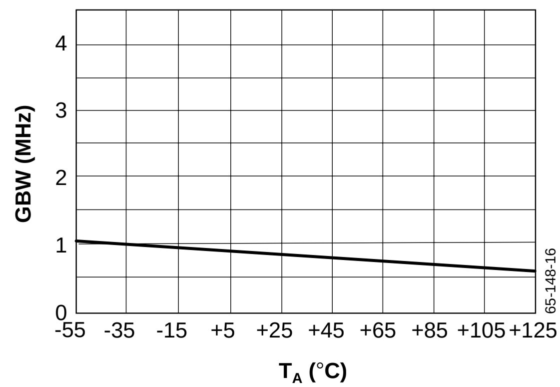


Figure 14. Gain Bandwidth Product vs. Temperature

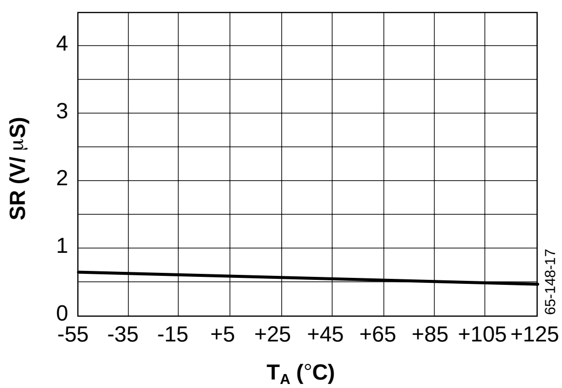


Figure 15. Slew Rate vs. Temperature

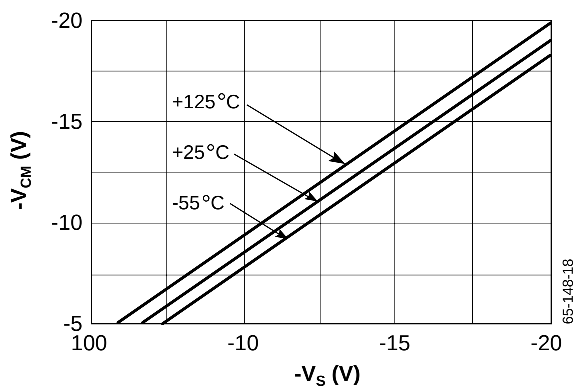


Figure 16. Negative Common Mode Input Voltage vs. Supply Voltage

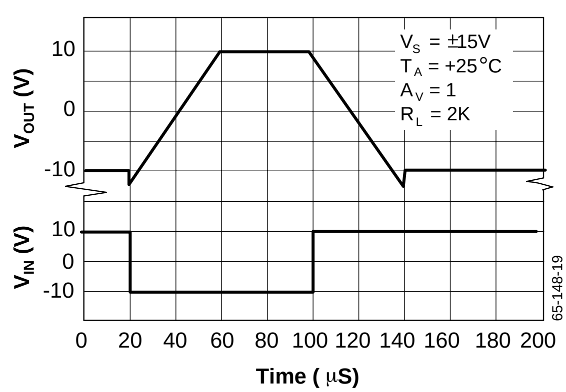


Figure 17. Inverting Large Signal Pulse Response Input, Output Voltage vs. Time

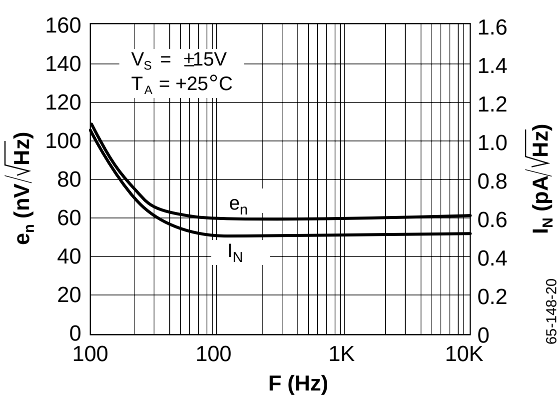


Figure 18. Input Noise Voltage, Current Densities vs. Frequency

Typical Performance Characteristics (continued)

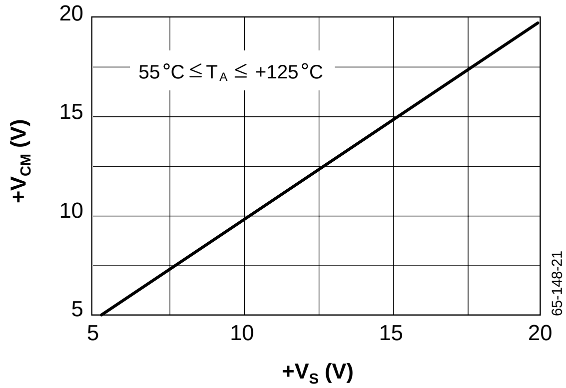


Figure 19. Positive Common Mode, Input Voltage vs. Supply Voltage

Typical Simulation

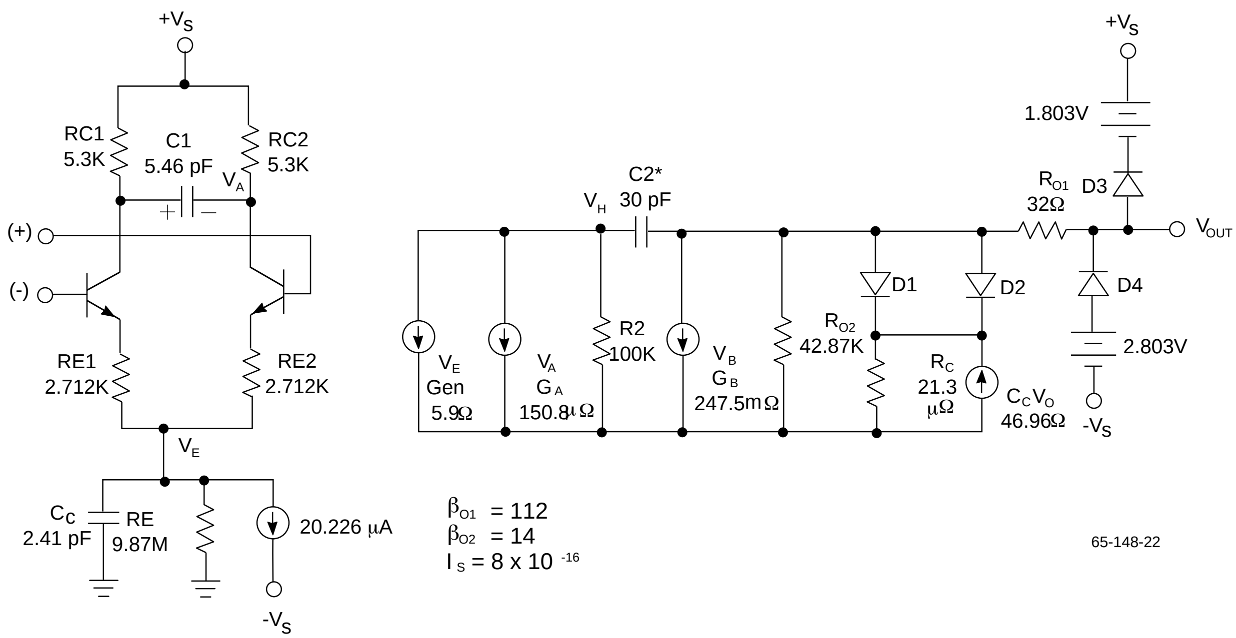


Figure 20. LM148 Macromodel for Computer Simulation

Applications Discussion

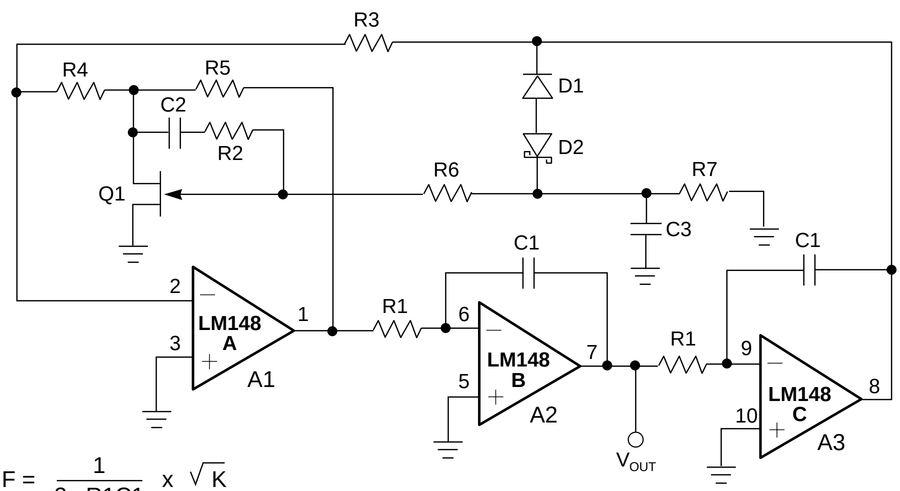
The LM148 low power quad operational amplifier exhibits performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs is within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The LM148 is short circuit protected to ground and supplies continuously when only one of the four amplifiers is shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0B frequency. If less, a lead capacitor should be placed between the output and input.



$$F = \frac{1}{2\pi R1C1} \times \sqrt{K}$$

$$K = \frac{R4R5}{R3}\left(\frac{1}{R_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right)$$

65-148-23

$$R_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

F_{MAX} = 5.0 KHz, THD $\leq$ 0.03%

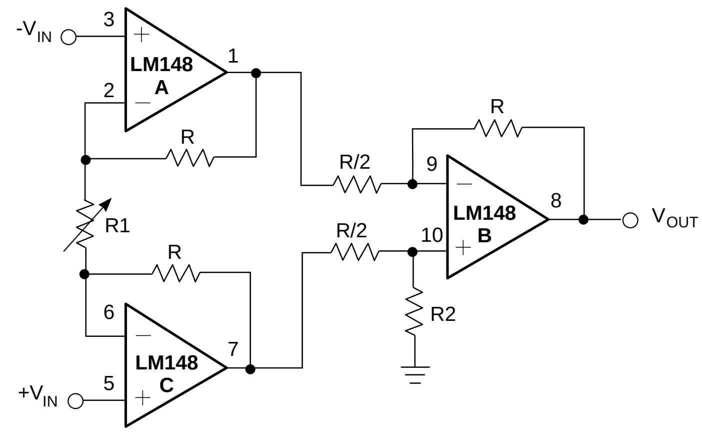
R1 = 100K pot., C1 = 0.0047 µF, C2 = 0.01 µF, C3 = 0.1 µF, R2 = R6 = R7 = 1M, R3 = 5.1K, R4 = 12Ω.

R5 = 240Ω, Q1 = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in feedback loop of A3.

Figure 21. One Decade Low Distortion Sinewave Generator

Applications Discussion (continued)



$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right), \left(-V_S - 3V\right) \leq V_{IN\,CM} \leq \left(+V_S - 3V\right)$$

$V_S = \pm 15V$

R = R2, trim R2 to boost CMRR

Figure 22. Low Cost Instrumentation Amplifier

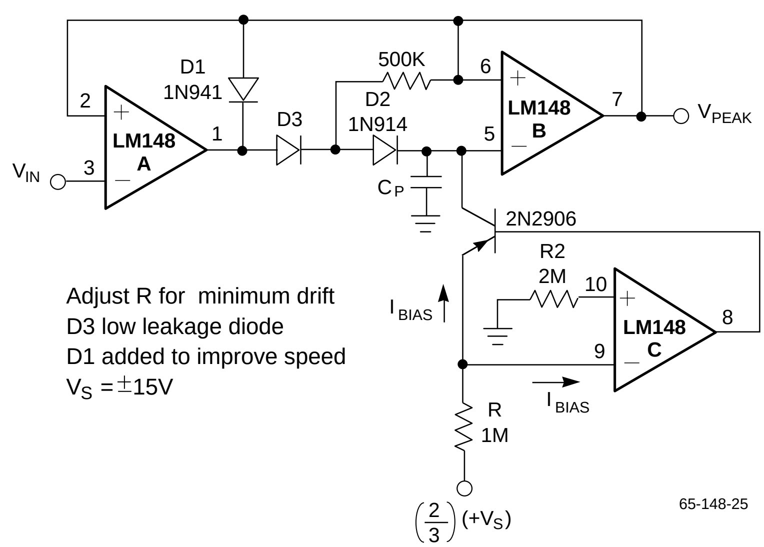
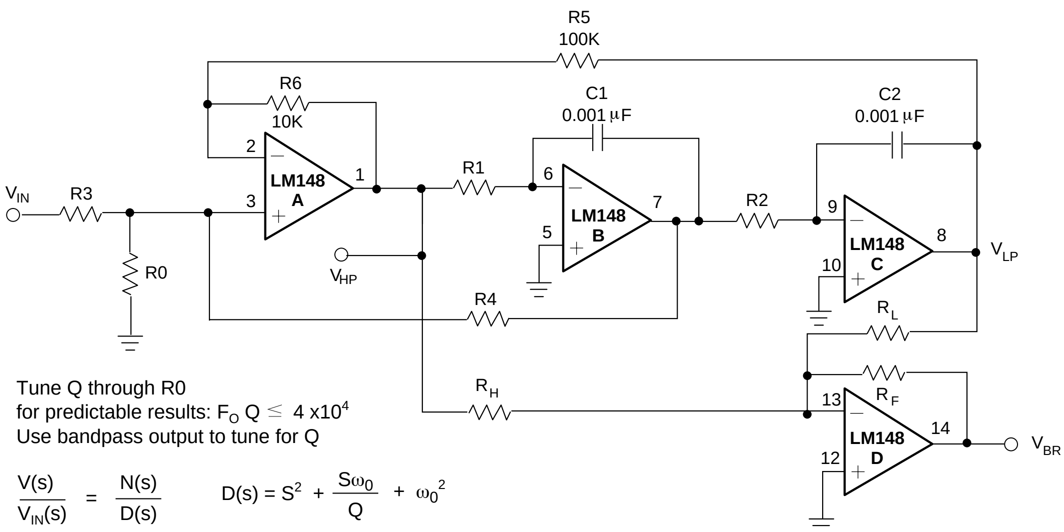


Figure 23. Low Voltage Peak Detector with Bias Current Compensation

Applications Discussion (continued)



Tune Q through R0
for predictable results: $F_O\ Q \leq 4 \times 10^4$
Use bandpass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)} \qquad D(s) = S^2 + \frac{S\omega_0}{Q} + \omega_0^2$$

$$N_{HP(S)} = S^2 H_{OHP},\ N_{BP(S)} = \frac{-S\omega_0 H_{OBP}}{Q} \qquad N_{LP} = \omega_0^2 H_{OLP}$$

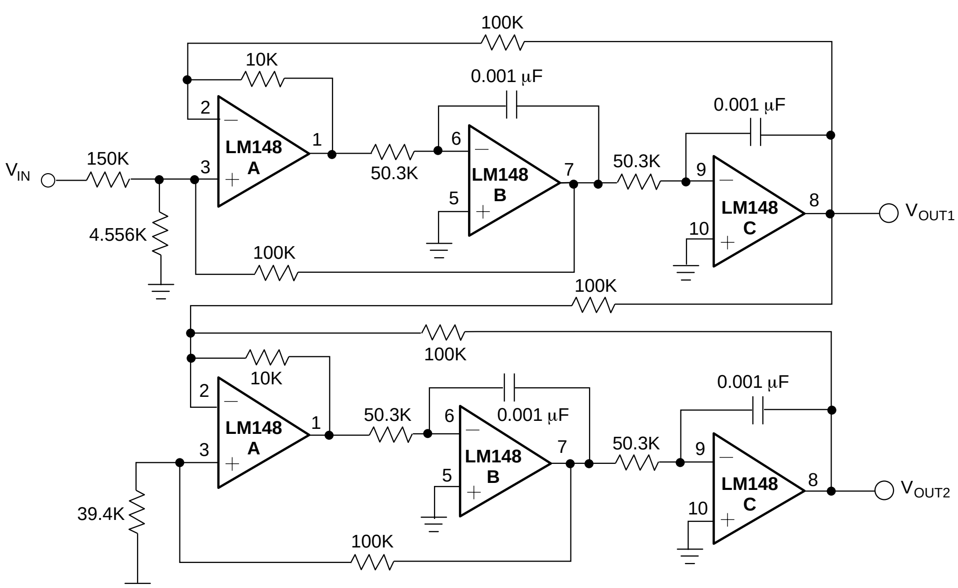
$$F_O = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}}, \qquad t1 = R1C1,\ Q = \left(\frac{1 + R4 \mid R3 + R4 \mid R0}{1 + R6 \mid R5}\right)\left(\frac{R6}{R5}\ \frac{t1}{t2}\right)^{1/2}$$

$$F_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\, t1\, t2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6 \mid R5}{1 + R3 \mid R0 + R3 \mid R4},\ H_{OBP} = \frac{1 + R4 \mid R3 + R4 \mid R0}{1 + R3 \mid R0 + R3 \mid R4}$$

$$H_{OLP} = \frac{1 + R5 \mid R6}{1 + R3 \mid R0 + R3 \mid R4}$$

65-148-26

Figure 24. Universal State-Space Filter

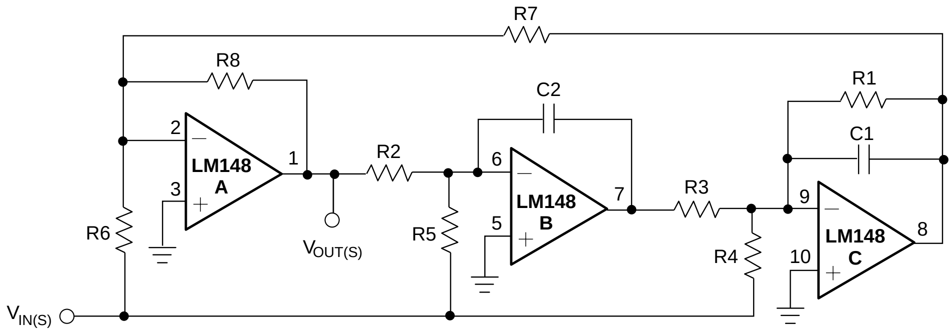


65-148-27

Use general equations, and tune each section separately.
Q_{1st} Section = 0.541, Q_{2nd} Section = 1.306.
The response should have 0 dB peaking.

Figure 25. 1 KHz 4-Pole Butterworth Filter

Applications Discussion (continued)



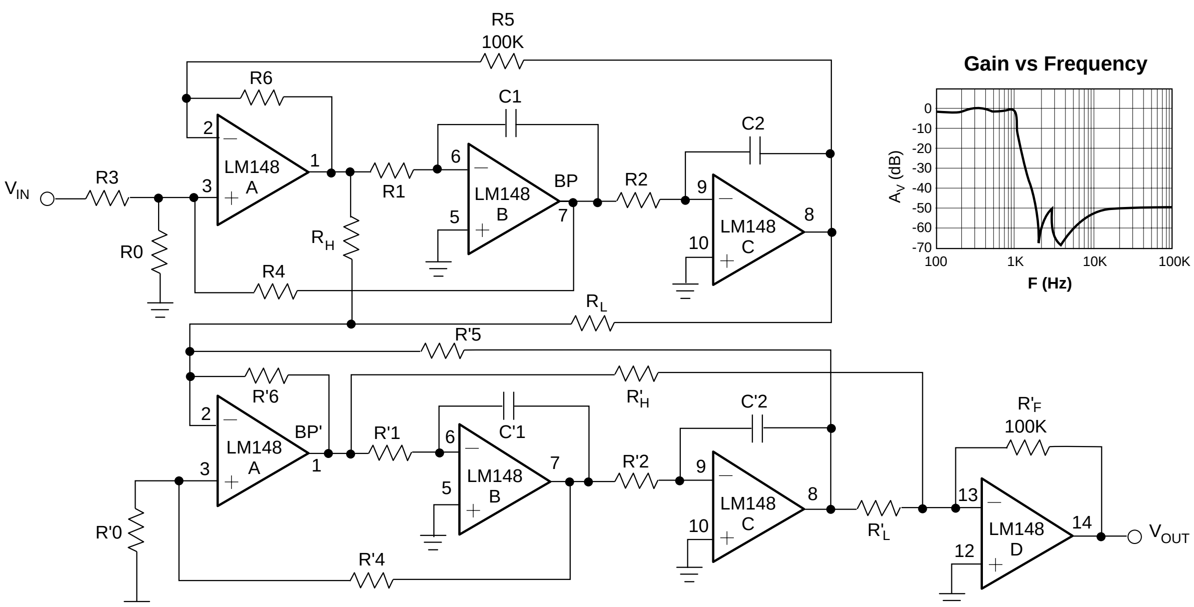
$$Q = \sqrt{\frac{R8}{R7}}\left(\frac{R1C1}{\sqrt{R3C2R2C1}}\right),\ F_O = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}}\left(\frac{1}{\sqrt{R2R3C1C2}}\right),\ F_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch : $\frac{1}{R6} = \frac{R1}{R4R7}$

Examples: F_{NOTCH} = 3 kHz, Q = 5, R1 = 270K, R2 = R3 = 20K, R4 = 27K, R5 = 20K, R6 = R8 = 10K, R7 = 100K.
C1 = C2 = 0.001 µF.
Better noise performance than the state-space approach.

65-148-28

Figure 26. 3 Amplifier Bi-Quad Notch Filter



F_C = 1 kHz, F_S = 2 kHz, F_P = 0.543. F_Z = 2.14, Q = 0.841, F'_P = 0.987, F'_Z = 4.92.
Q' = 4.403 normalized to ripple BW.

$$F_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\left(\frac{1}{t}\right),\ F_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}}\left(\frac{1}{t}\right),\ Q = \frac{1 + R4/R3 + R4/R0}{1 + R6/R5} \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R'5}} \times \frac{1 + R'4/R'0}{1 + R'6/R'5 + R'6/R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the B'P outputs to tune Q, Q', tune the 2 sections separately.
R1 = R2 = 92.6K, R3 = R4 = R5 = 100K, R6 = 10K, R0 = 107.8K, R_L = 100K, R_H = 155.1K,
R'1 = R'2 = 50.9K, R'4 = R'5 = 100K, R'6 = 10K, R'0 = 5.78K, R'_L = 100K, R'_H = 248.12K, R'_F = 100K.

65-148-29

All capacitors are 0.001µF.

Figure 27. 4th Order 1 KHz Elliptic Filter (4 Poles, 4 Zeros)

Notes:

Notes:

Notes:

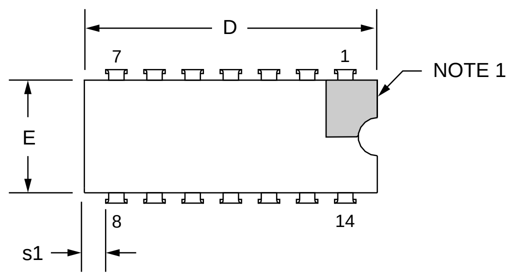
Mechanical Dimensions

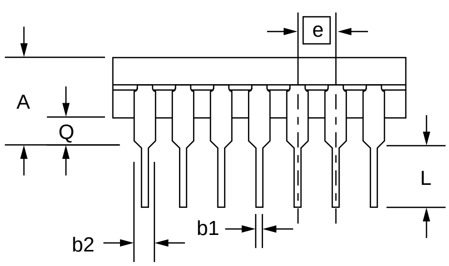
14-Pin Ceramic DIP

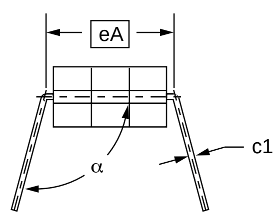
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.







Ordering Information

Part Number	Package	Operating Temperature Range
LM148D	14-Lead Ceramic DIP	-55°C to +125°C
LM148D/883B	14-Lead Ceramic DIP	-55°C to +125°C

Note:
1. 883B suffix denotes Mil-Std-883, Level B processing

5/20/98 0.0m 001
Stock#DS3000148

LM1851

Ground Fault Interrupter

Features

- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from AC line—26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets UL943 standards
- 450 µA quiescent current
- Ideal for 120V or 220V systems

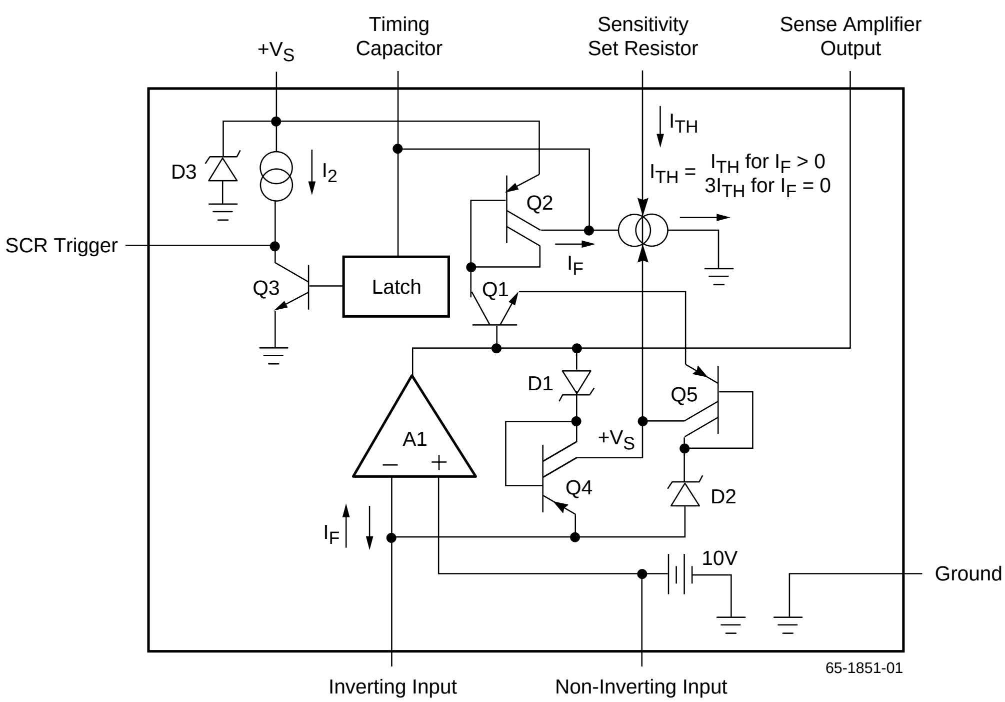
Description

The LM1851 is a controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions (example: a pool of water and electrical equipment connected to opposite phases of the AC line) in consumer and industrial environments. The output of the IC triggers an external SCR, which in turn opens a relay circuit breaker to prevent a harmful or lethal shock.

Full advantage of the U.S. UL943 timing specification is taken to ensure maximum immunity to false triggering due to line noise. A special feature is found in circuitry that rapidly resets the integrating timing capacitor in the event that noise pulses introduce unwanted charging currents. Also, flip-flop is included that ensures firing of even a slow circuit breaker relay on either half-cycle of the line voltage when external full wave rectification is used.

The application circuit can be configured to detect both normal faults (hot wire to ground) and grounded neutral faults.

Block Diagram



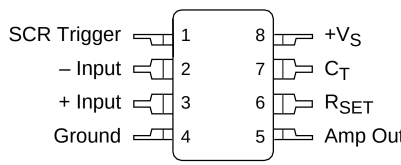
Functional Description

The voltage at the supply pin is clamped to +26V by the internal shunt regulator D3. This shunt regulator also generates an artificial ground voltage for the noninverting input of A1 (shown as a +10V source). A1, Q1, and Q2 act a a current mirror for fault current signals (which are derived from an external transformer). When a fault signal is present, the mirrored current charges the external timing capacitor until its voltage exceeds the latch trigger threshold (typically 17.5V). When then this threshold is exceeded, the latch engages and Q3 turns off, allowing I_2 to drive the SCR connected to pin 1.

Extra Circuitry in the feedback path of A1 works with the switched current source I_1 to remove any charge on C_T induced by noise in the transformer. If no fault current is present, then I_1 discharges C_T with a current equal to 3 I_{TH}, where I_{TH} is the value of current set by the external R_{SET} resistor. If fault signals are present at the input of A1 (which is held at virtual ground, +10V), one of the two current mirrors in the feedback path of A1 (Q4 and Q5) will become active, depending on which half-cycle the fault occurs. This action will raise the voltage at V_S, switching I_1 to a value equal to I_{TH}, and reducing the discharge rate of C_T to better allow fault currents to charge it.

Notice that I_{TH} discharges C_T during both half-cycles of the line, while I_F only charges C_T during the half-cycle in which I_F exits pin 2 (since Q1 will only carry fault current in one direction). Thus, during one half-cycle, I_F-I_{TH} charges C_T, while during the other half-cycle I_{TH} discharges it.

Pin Assignments

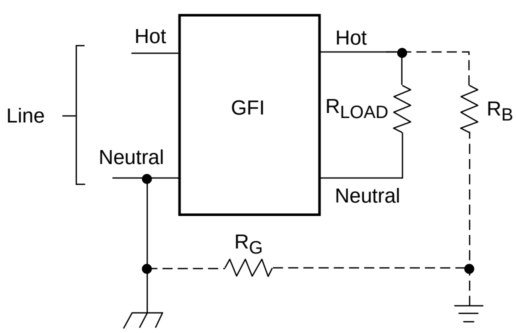


65-1851-02

Definition of Terms

Normal Fault

An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines in Figure1.



65-1851-03

Figure 1. Normal Fault

Grounded Neutral Fault

An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines in Figure 2.

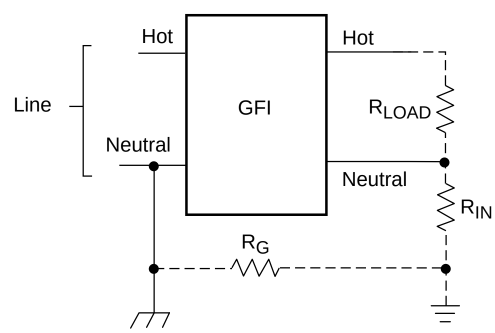


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Figure 2. Grounded Neutral Fault

Normal Fault Plus Grounded Neutral Fault

The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines in Figure 3.

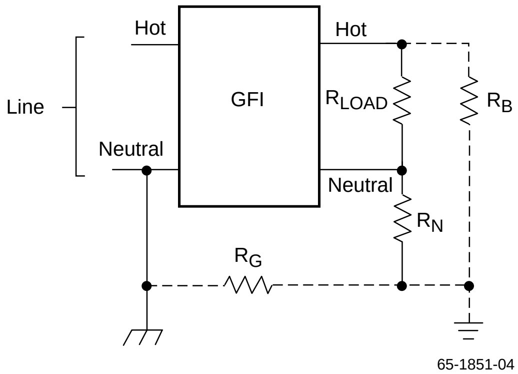


Figure 3. Normal Fault Plus Grounded Neutral Fault

Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Units
Supply Current			19	mA
Power Dissipation			570	mW
Operating Temperature		-40	70	°C
Lead Soldering Temperature	SOIC, 10 seconds		260	°C
	DIP, 60 seconds		300	°C

Thermal Characteristics

Parameter	Conditions	Min	Max	Units
Maximum Junction Temperature			125	°C
Maximum P_DT_A < 50°C	DIP		468	mW
	SOIC		300	
Thermal Resistance, θ_{JA}	DIP		160	°C/W
	SOIC		240	
For TA > 50°C, derate at	DIP		6.25	mW/°C
	SOIC		4.17	

DC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Test Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1 With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1 Without Fault		100	240	mV
Output Saturation Resistance	Pin 1 Without Fault		100		Ω
Output External Current Sinking Capability[1]	Pin 1 Without Fault, V_{PIN1} Held to 0.3V	2	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault Fault and Fault Conditions	2.0	2.8	3.6	µA/µA

Notes:

1. This external applied current is in addition to the internal “output drive current” source.

AC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity[2]	See Figure 9	3	5	7	mA
Normal Fault Trip Time[1]	500Ω Fault, see Figure 10		18		mS
Normal Fault With Grounded	500Ω Normal Fault		18		mS
Neutral Fault Trip Time[1]	2Ω Neutral, see Figure 10				

Notes:

1. Average of 10 trials.
2. Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity is necessary.

Typical Performance Characteristics (T_A = +25°C)

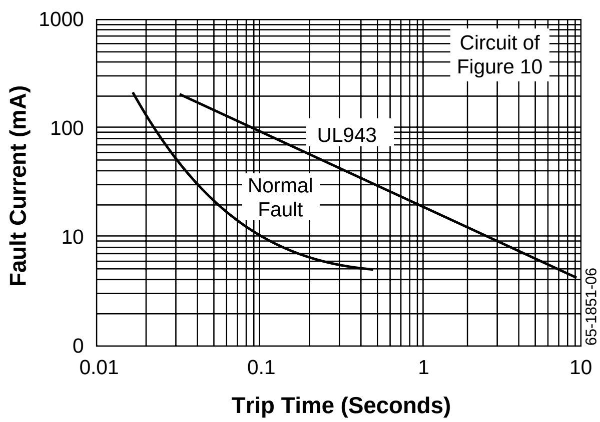


Figure 4. Average Trip Time vs. Fault Current

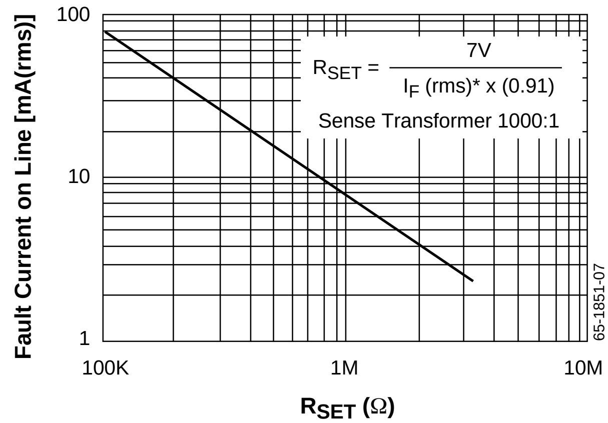


Figure 5. Normal Fault Current Threshold vs. R_{SET}

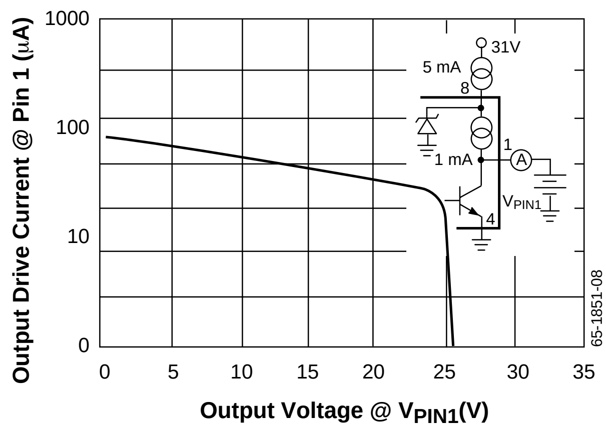


Figure 6. Output Drive Current vs. Output Voltage

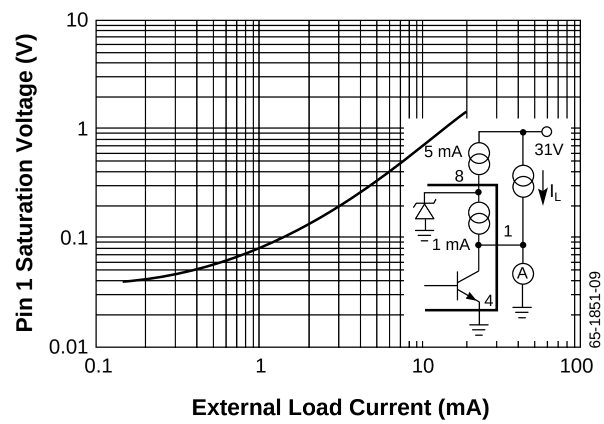


Figure 7. Pin 1 Saturation Voltage vs. External Load Current, I_L

Applications Discussion

A typical ground fault interrupter circuit is shown in Figure 10. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the dc power required by the IC. A 1 μF capacitor at pin 8 is used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load.

At this time no fault current flows and the C_T discharge current increases from I_{TH} to $3I_{TH}$ (see Block Diagram). This quickly resets both the timing capacitor and the output latch. The circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the got and neutral lines, is stepped down by 1000 and fed into the input pin of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \quad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_F(rms)}{2} \times 0.91 \quad (2)$$

Where I_F(rms) is the rms input fault current to the operational amplifier and the factor of 2 is due to the fact that I_F charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have:

$$R_{SET} = \frac{7V}{I_F(rms) \times 0.91} \quad (3)$$

For example, to obtain 5 mA(rms) sensitivity for the circuit in Figure 7 we have:

$$R_{SET} = \frac{7V}{\frac{5\text{ mA} \times 0.91}{1000}} = 1.5M\Omega \quad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity “window” of 4 mA to 6mA, provision should be made to adjust R_{SET} with a potentiometer.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_T. Due to the large number of variables involved, proper selection of C_T is best done empirically. The following design example should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagrammatically in Figure 8.

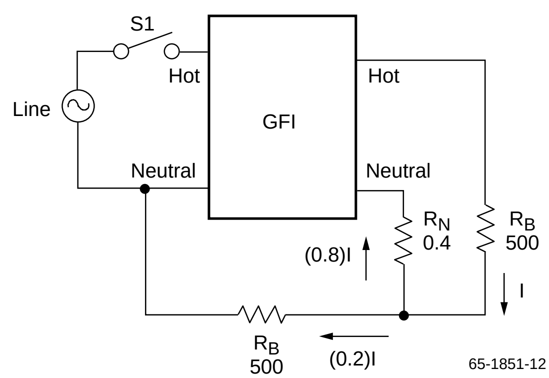


Figure 8.

UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_T based upon charging currents due to normal fault only is as follows:

1. Start with a ≤25 ms specification. Subtract 3 ms GFI turn-on time (15k and 1 μF). Subtract 8 ms potential loss of one half-cycle due to fault current sense of half-cycles only.
2. Subtract 4 ms time required to open a sluggish circuit breaker.
3. This gives a total ≤10 ms maximum integration time that could be allowed.
4. To generate 8 ms value of integration time that accommodates component tolerances and other variables:

$$C_T = \frac{1 \times T}{V} \quad (5)$$

where:
T = integration time
V = threshold voltage
I = average fault current into CT

$$I = \underbrace{\left(\frac{120\ V_{AC}(rms)}{R_B}\right)}_{\text{heavy fault current generated (swamps } I_{TH})} \underbrace{\left(\frac{RN}{RG + RN}\right)}_{\text{portion of fault current shunted around GFI}}$$

$$\times \underbrace{\left(\frac{1\ \text{turn}}{1000\ \text{turns}}\right)}_{\text{current division of input sense transformer}} \times \underbrace{\left(\frac{1}{2}\right)}_{\text{CT charging on half-cycles only}} \times \underbrace{(0.91)}_{\text{rms to average conversion}} \qquad (6)$$

therefore:

$$C_T = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6 + 0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right]}{17.5} \times 0.008$$

$$C_T = 0.01\ \mu F \qquad (7)$$

In practice, the actual value of C_T will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C_T.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacity can be used and better noise immunity obtained.

The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In Figure 10, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Transformers may be obtained from Magnetic Metals, Inc., 21st Street and Hayes Street, Camden, NJ 08101—
(609) 964-7842.

Application Circuits

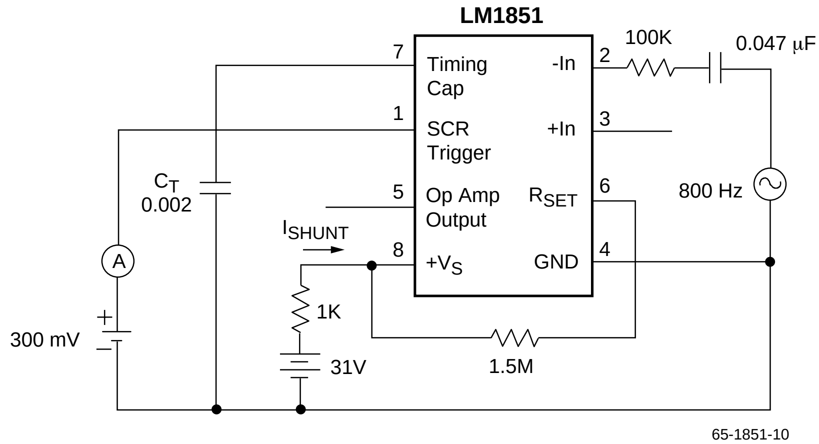


Figure 9. Normal Fault Sensitivity Test Circuit

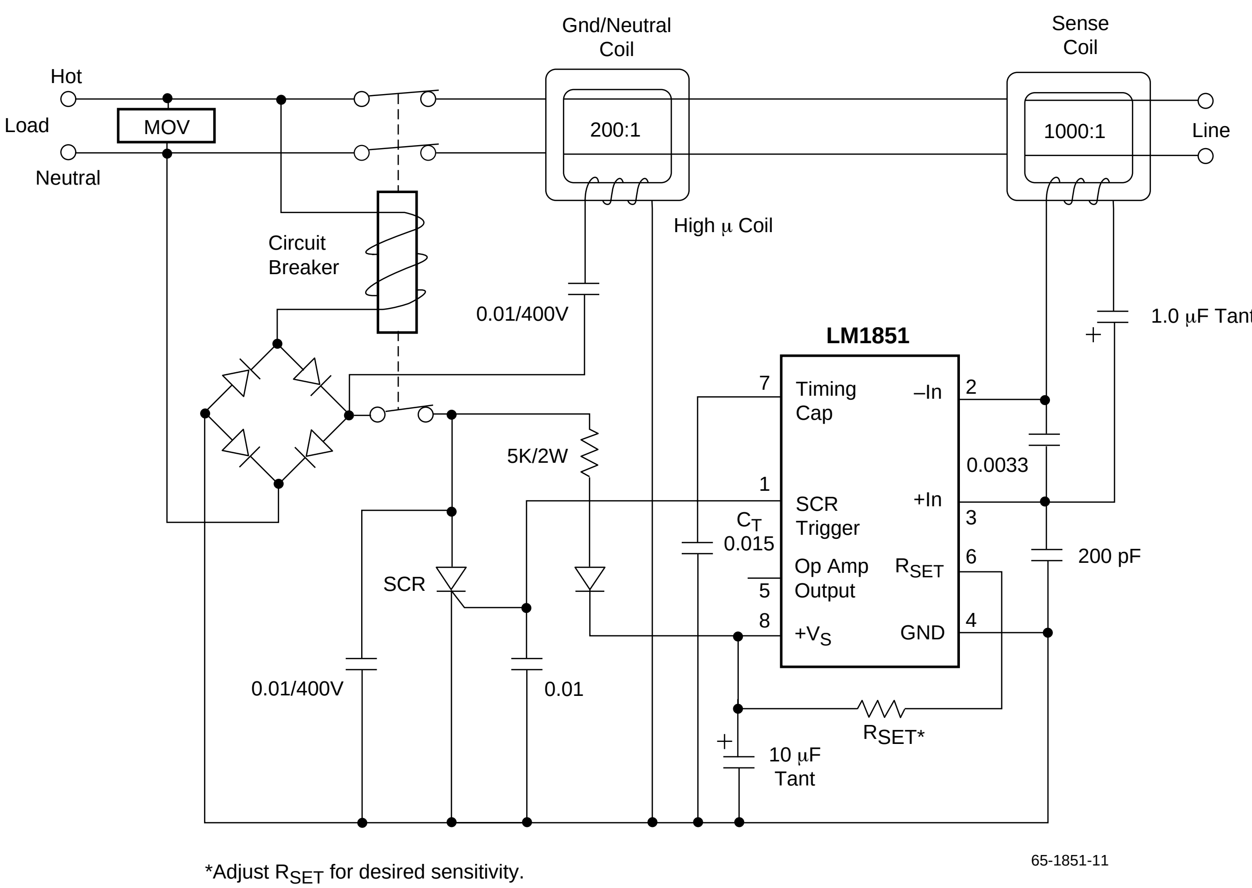
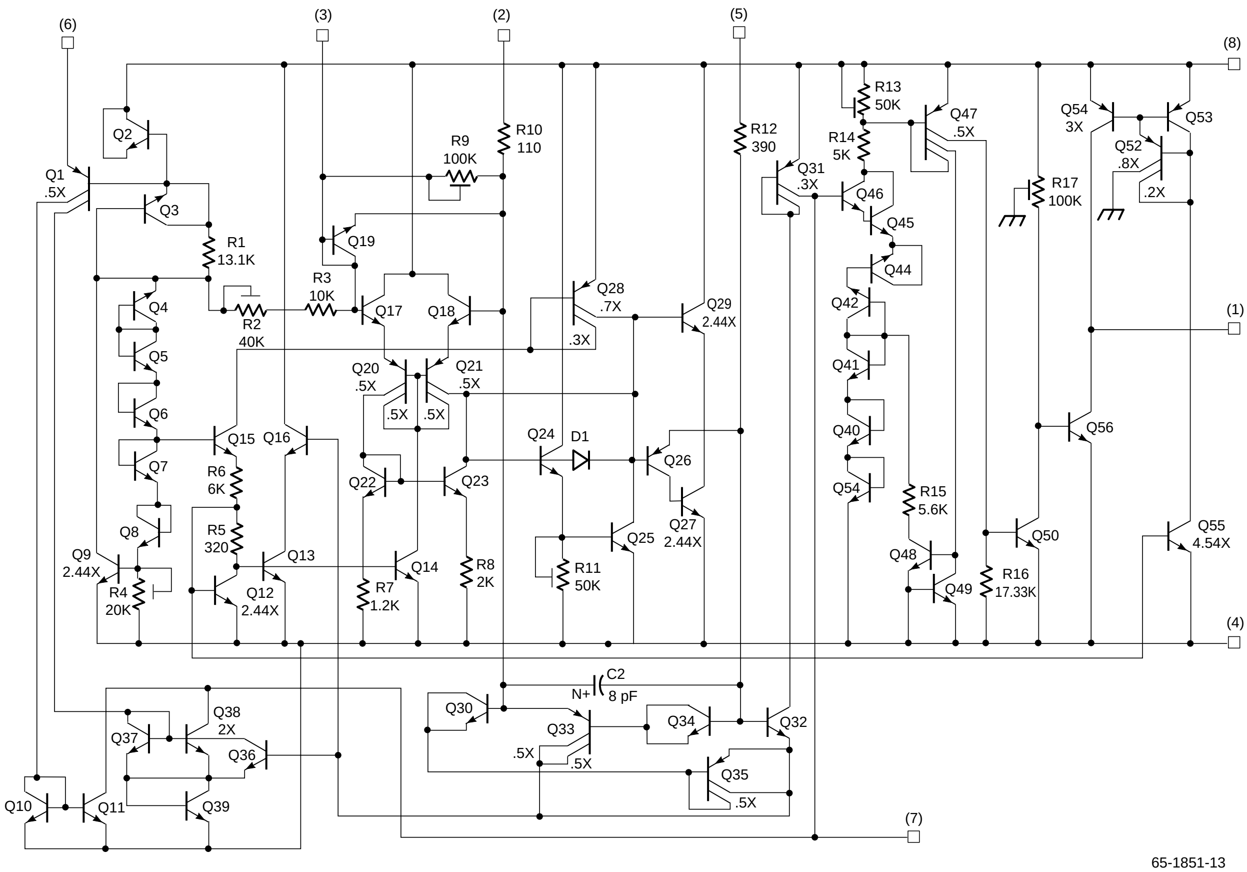


Figure 10. 120 Hz Neutral Transformer Application

Schematic Diagram



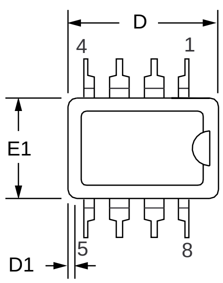
Mechanical Dimensions

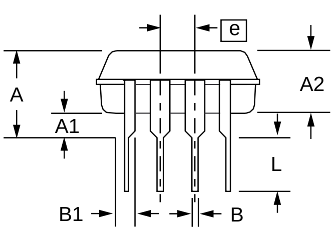
8-Lead Plastic DIP Package

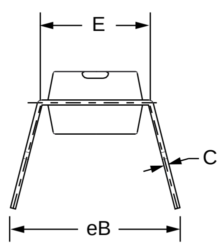
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







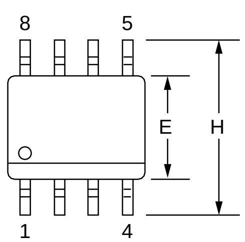
Mechanical Dimensions (continued)

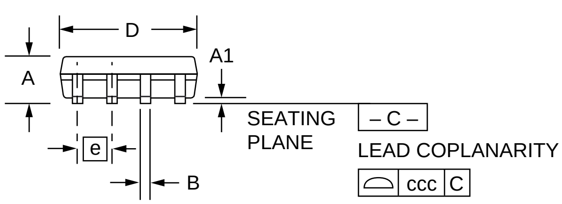
8-Lead Plastic SOIC Package

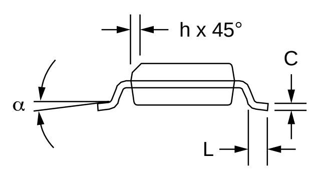
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
LM1851AN	8-lead Plastic DIP	-40°C to +70°C
RV4145M	8-lead Plastic SOIC	-40°C to +70°C

5/20/98 0.0m 001
Stock#DS30001851

National Semiconductor

March 1995

LM1882•54ACT/74ACT715
LM1882-R•54ACT/74ACT715-R
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R are 20-pin TTL-input compatible devices capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The devices are capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

These devices make no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

The 'ACT715/LM1882 is mask programmed to default to a Clock Disable state. Bit 10 of the Status Register, Register 0, defaults to a logic "0". This facilitates (re)programming before operation.

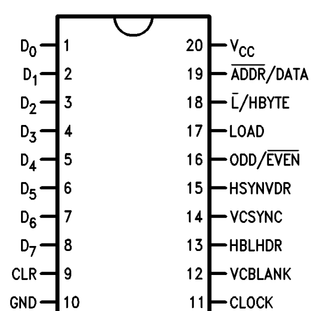
The 'ACT715-R/LM1882-R is the same as the 'ACT715/LM1882 in all respects except that the 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enabled state. Bit 10 of the Status Register defaults to a logic "1". Although completely (re)programmable, the 'ACT715-R/LM1882-R version is better suited for applications using the default 14.31818 MHz RS-170 register values. This feature allows power-up directly into operation, following a single CLEAR pulse.

Features

- Maximum Input Clock Frequency > 130 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- 4 KV minimum ESD immunity
- 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enable state for easier start-up into 14.31818 MHz RS170 timing

Connection Diagrams

Pin Assignment for DIP and SOIC



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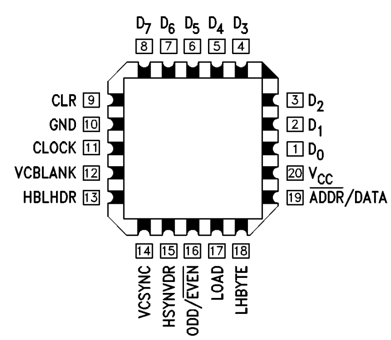
Order Number LM1882CN or LM1882CM
For Default RS-170, Order Number LM1882-RCN or LM1882-RCM

Pin Assignment for LCC



TL/F/10137–2

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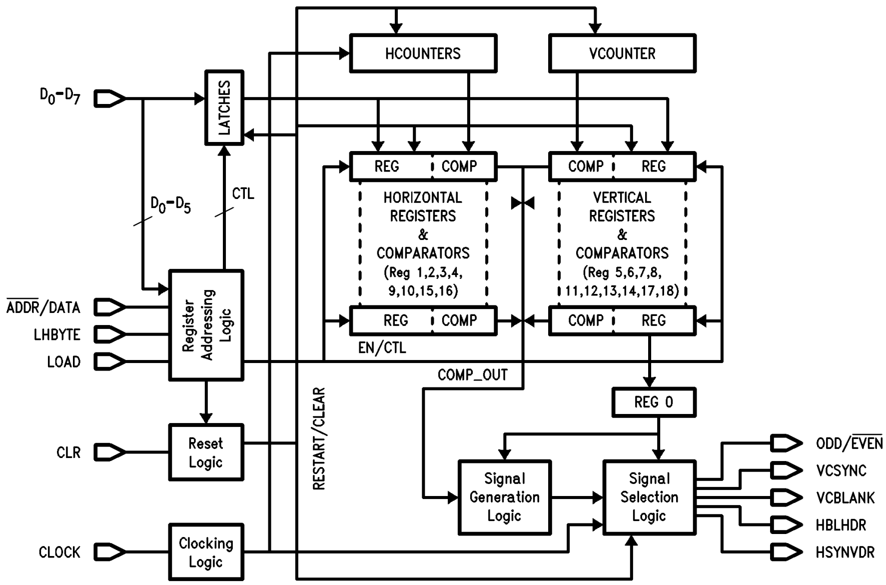
FACT™ is a trademark of National Semiconductor Corporation.

Logic Block Diagram



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Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

$\overline{\text{ADDR}}$/DATA: The $\overline{\text{ADDR}}$/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

$\overline{\text{L}}$/HBYTE: The $\overline{\text{L}}$/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The LOAD control pin loads data into the Address or Data Registers on the rising edge. $\overline{\text{ADDR}}$/DATA and $\overline{\text{L}}$/HBYTE data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System CLOCK input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity. The CLOCK and the LOAD signal are asynchronous and independent. Output state changes occur on the falling edge of CLOCK.

CLR: The CLEAR pin is an asynchronous input that initializes the device when it is HIGH. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The CLEAR pin has been implemented as a Schmitt trigger for better noise immunity. A CLEAR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers—even if the user plans to (re)program the device.

Note: A CLEAR pulse will disable the CLOCK on the 'ACT715/LM1882 and will enable the CLOCK on the 'ACT715-R/LM1882-R.

ODD/$\overline{\text{EVEN}}$: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this output is always HIGH. Data can be serially scanned out on this pin during Scan Mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register. Equalization and Serration pulses will (if enabled) be output on the VCSYNC signal in composite mode only.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or Cursor Position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs. The default value for the Status Register is 0 (000 Hex) for the 'ACT715/LM1882 and is "512" (200 Hex) for the 'ACT715-R/LM1882-R.

Register Description (Continued)

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0 (DEFAULT)	CBLANK	CSYNC	HGATE	VGATE
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Bits 3–4

B_4	B_3	Mode of Operation
0 (DEFAULT)	0	Interlaced Double Serration and Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Double Equalization and Serration mode will output equalization and serration pulses at twice the HSYNC frequency (i.e., 2 equalization or serration pulses for every HSYNC pulse). Single Equalization and Serration mode will output an equalization or serration pulse for every HSYNC pulse. In Interlaced mode equalization and serration pulses will be output during the VBLANK period of every odd and even field. Interlaced Single Equalization and Serration mode is not possible with this part.

Bits 5–8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates an output pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9–11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

Default values for B10 are "0" in the 'ACT715/LM1882 and "1" in the 'ACT715-R/LM1882-R.

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

This bit is not intended for the user but is for internal testing only.

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the Horizontal Blank signal (see *Figure 1*). Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Horizontal Blank reference pulse, edges referenced to this first Horizontal edge are n + 1 CLOCKs away, where "n" is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This

Signal Specification (Continued)

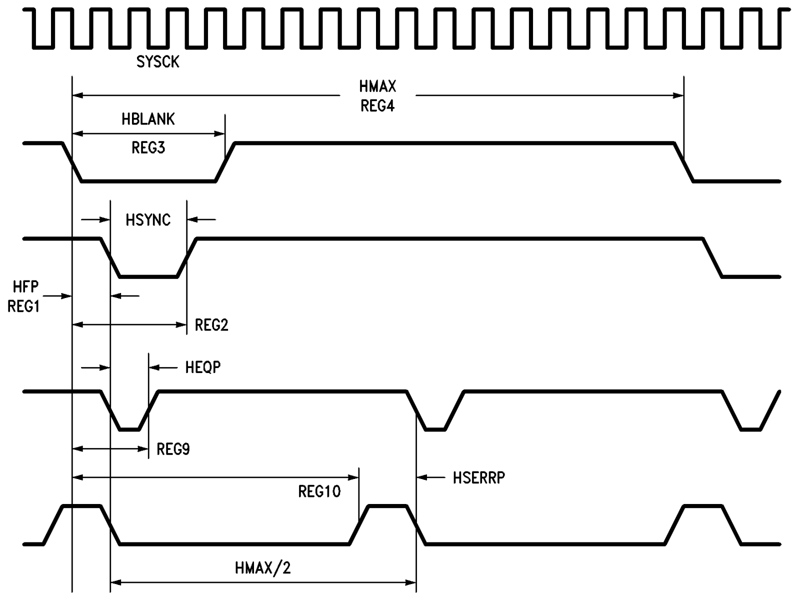

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FIGURE 1. Horizontal Waveform Specification

limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Vertical Blank (first Horizontal Blank) reference pulse, edges referenced to this first edge are n + 1 lines away, where "n" is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore registers 5, 6, and 7 must contain a value twice the total horizontal (odd and even) plus 1 (as described above). In non-interlaced mode, all vertical timing is based on whole-lines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC. (See *Figure 2A*.)

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The Serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulses occur preceding and/or following the Serration pulses. The width and location of these pulses can be programmed through the registers shown below. (See *Figure 2B*.)

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper
REG 9 = (HFP) + (HEQP) + 1

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper
REG 10 = (HFP) + (HPER/2) − (HSERR) + 1

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

Signal Specification (Continued)

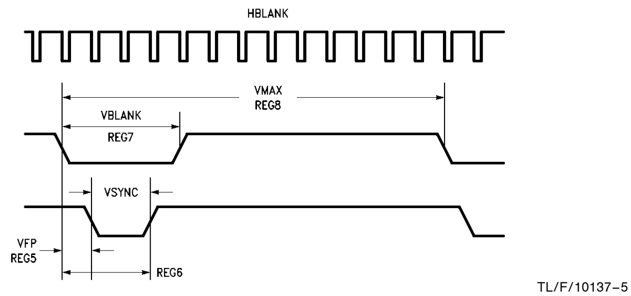


FIGURE 2A. Vertical Waveform Specification

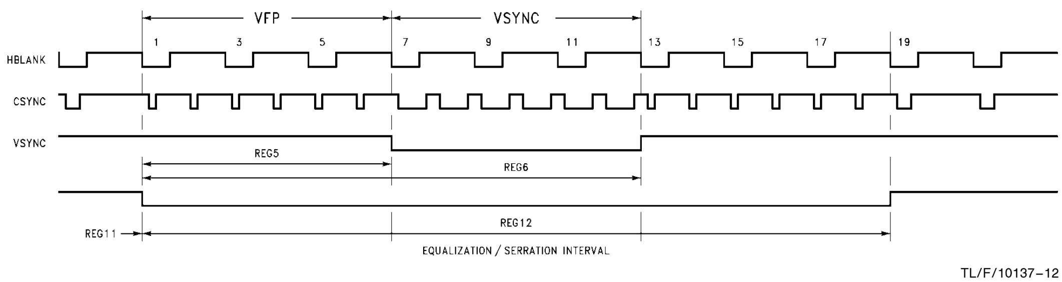


FIGURE 2B. Equalization/Serration Interval Programming

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal Drive and Vertical Drive outputs can be utilized as general purpose Gating Signals. Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of Bit 2 of the Status Register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and Bit 2 of the Status Register is set to the value of 1. The Cursor Position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

Addressing Logic

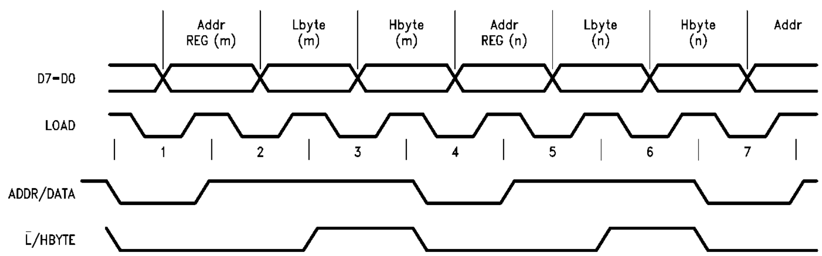
The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of LOAD when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of LOAD after ADDRDATA and LHBYTE goes low.

Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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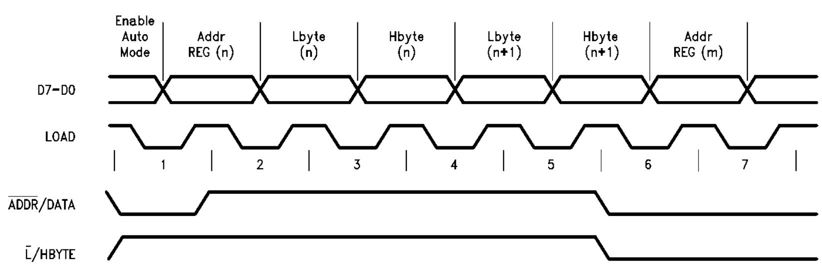
Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n+1)
5	Enable Hbyte Data Load	Load Hbyte (n+1); Inc Counter
6	Enable Manual Addressing	Load Address



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Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Two types of ADDRDEC logic is enabled by 2 pair of addresses, Addresses 22 or 54 (Vectored Restart logic) and Addresses 23 or 55 (Vectored Clear logic). Loading these addresses will enable the appropriate logic and put the part into either a Restart (all counter registers are reinitialized with preprogrammed data) or Clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal CLOCK is disabled. Clocking the part during a Vectored Restart or Vectored Clear state will have no effect on the part. To resume operation in the new state, or disable the Vectored Restart or Vectored Clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an unused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following Addresses are used by the device.

Address 0	Status Register REG0
Address 1–18	Data Registers REG1–REG18
Address 19–21	Unused
Address 22/54	Restart Vector (Restarts Device)
Address 23/55	Clear Vector (Zeros All Registers)
Address 24–31	Unused
Address 32–50	Register Scan Addresses
Address 51–53	Counter Scan Addresses
Address 56–63	Unused

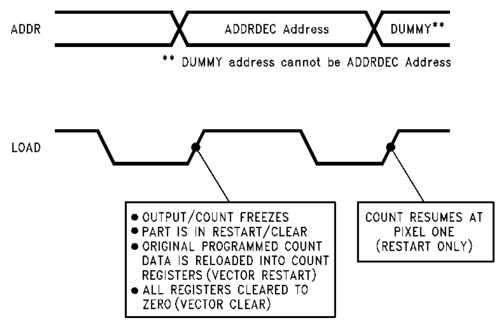
At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the preprogramming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers to zero simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.



TL/F/10137–9

FIGURE 3. ADDRDEC Timing

GEN LOCKING

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R is designed for master SYNC and BLANK signal generation. However, the devices can be synchronized (slaved) to an external timing signal in a limited sense. Using Vectored Restart, the user can reset the counting sequence to a given location, the beginning, at a given time, the rising edge of the LOAD that removes Vector Restart. At this time the next CLOCK pulse will be CLOCK 1 and the count will restart at the beginning of the first odd line.

Preconditioning the part during normal operation, before the desired synchronizing pulse, is necesasry. However, since LOAD and CLOCK are asynchronous and independent, this is possible without interruption or data and performance corruption. If the defaulted 14.31818 MHz RS-170 values are being used, preconditioning and restarting can be minimized by using the CLEAR pulse instead of the Vectored Restart operation. The 'ACT715-R/LM1882-R is better suited for this application because it eliminates the need to program a 1 into Bit 10 of the Status Register to enable the CLOCK. Gen Locking to another count location other than the very beginning or separate horizontal/vertical resetting is not possible with the 'ACT715/LM1882 nor the 'ACT715-R/LM1882-R.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The LSB will be scanned out first. Since each register is 12 bits wide, completely scanning out data of the addressed register will require 12 CLOCK pulses. More than 12 CLOCK pulses on the same register will only cause the MSB to repeat on the output. Re-scanning the same register will require that register to be reloaded. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53. Note that before the part will scan out the data, the LOAD signal must be brought back HIGH.

Addressing Logic (Continued)

Normal device operation can be resumed by loading in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format (using a 14.31818 MHz clock signal) and how they compare against the actual EIA RS170 Specifications. The default signals that will be output are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected so that a pulse indicating the active lines would be output.

Reg	D	Value H	Register Description
REG0	0	000	Status Register (715/LM1882)
REG0	1024	400	Status Register (715-R/LM1882-R)
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	039	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

RS170 Horizontal Data

Signal	Width	μs	%H	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER iod	910 Clocks	63.556	100	

RS170 Vertical Data

Signal	Width	μs	%H	Specification (μs)
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERiod (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERiod (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±15 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±20 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
Ceramic	175°C
Plastic	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$ $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to +125°C $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4	5.4	V	
		4.5		3.86	3.7	3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86	4.7	4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1	0.1	V	
		4.5		0.36	0.5	0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36	0.5	0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5			32.0	32.0	mA	$V_{OLD} = 1.65V$
I_{OHD}	Minimum Dynamic Output Current	5.5			−32.0	−32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CC}	Supply Current Quiescent	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1V$

*All outputs loaded; thresholds on input associated with input under test.

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190		130		150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220		145		175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5	3.5	19.5	3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0	3.5	22.0	3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0	3.0	20.0	3.0	19.5	ns

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimums			
t_{sc} t_{sc}	Control Setup Time ADDR/DATA to LOAD− L/HBYTE to LOAD−	5.0	3.0 3.0	4.0 4.0	4.5 4.5	4.5 4.5	ns ns
t_{sd}	Data Setup Time D7–D0 to LOAD+	5.0	2.0	4.0	4.5	4.5	ns
t_{hc}	Control Hold Time LOAD− to ADDR/DATA LOAD− to L/HBYTE	5.0	0 0	1.0 1.0	1.0 1.0	1.0 1.0	ns ns
t_{hd}	Data Hold Time LOAD+ to D7–D0	5.0	1.0	2.0	2.0	2.0	ns
t_{rec}	LOAD+ to CLK (Note 1)	5.0	5.5	7.0	8.0	8.0	ns
t_{wld-} t_{wld+}	Load Pulse Width LOW HIGH	5.0 5.0	3.0 3.0	5.5 5.0	5.5 7.5	5.5 7.5	ns ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5	9.5	9.5	ns
t_{wck}	CLOCK Pulse Width (HIGH or LOW)	5.0	2.5	3.0	4.0	3.5	ns

Note 1: Removal of Vectored Reset or Restart to Clock.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements (Continued)

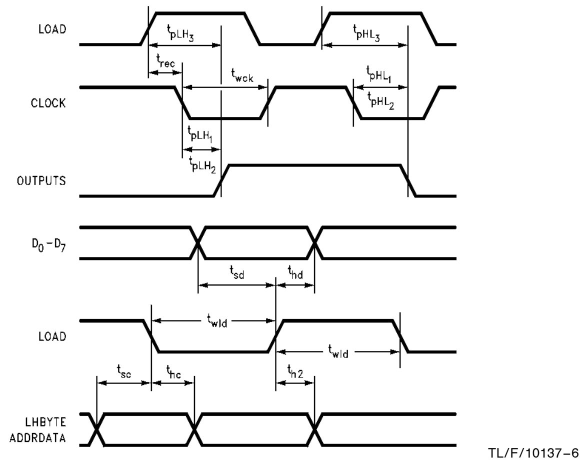


FIGURE 4. AC Specifications

Additional Applications Information

POWERING UP

The 'ACT715/LM1882 default value for Bit 10 of the Status Register is 0. This means that when the CLEAR pulse is applied and the registers are initialized by loading the default values the CLOCK is disabled. Before operation can begin, Bit 10 must be changed to a 1 to enable CLOCK. If the default values are needed (no other programming is required) then *Figure 5* illustrates a hardwired solution to facilitate the enabling of the CLOCK after power-up. Should control signals be difficult to obtain, *Figure 6* illustrates a possible solution to automatically enable the CLOCK upon power-up. Use of the 'ACT715-R/LM1882-R eliminates the need for most of this circuitry. Modifications of the *Figure 6* circuit can be made to obtain the lone CLEAR pulse still needed upon power-up.

Note that, although during a Vectored Restart none of the preprogrammed registers are affected, some signals are affected for the duration of one frame only. These signals are the Horizontal and Vertical Drive signals. After a Vectored Restart the beginning of these signals will occur at the first CLK. The end of the signals will occur as programmed. At the completion of the first frame, the signals will resume to their programmed start and end time.

PREPROGRAMMING "ON-THE-FLY"

Although the 'ACT715/LM1882 and 'ACT715-R/LM1882-R are completely programmable, certain limitations must be set as to when and how the parts can be reprogrammed. Care must be taken when reprogramming any End Time registers to a new value that is lower than the current value. Should the reprogramming occur when the counters are at a count after the new value but before the old value, then the counters will continue to count up to 4096 before rolling over.

For this reason one of the following two precautions are recommended when reprogramming "on-the-fly". The first recommendation is to reprogram horizontal values during the horizontal blank interval only and/or vertical values during the vertical blank interval only. Since this would require delicate timing requirements the second recommendation may be more appropriate.

The second recommendation is to program a Vectored Restart as the final step of reprogramming. This will ensure that all registers are set to the newly programmed values and that all counters restart at the first CLK position. This will avoid overrunning the counter end times and will maintain the video integrity.

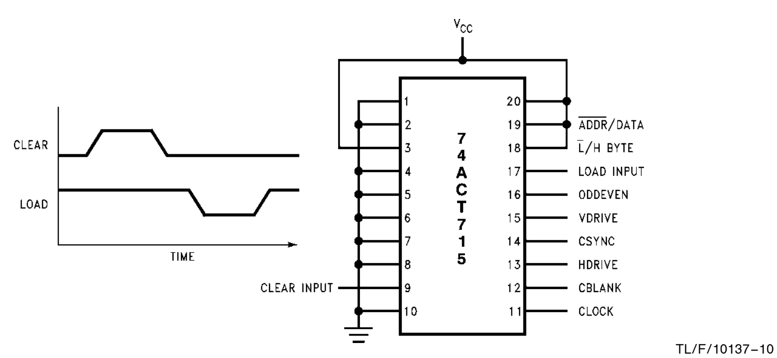
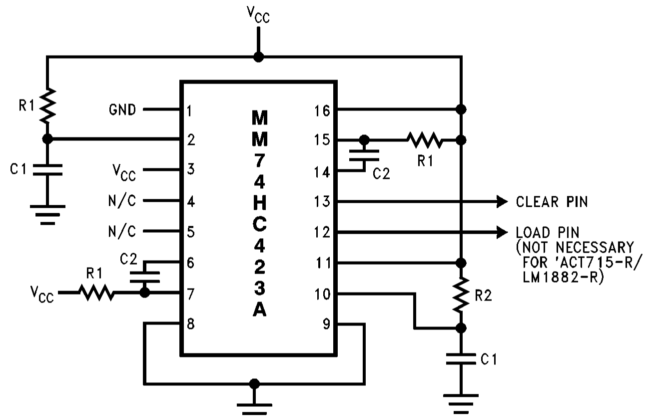


FIGURE 5. Default RS170 Hardwire Configuration

Additional Applications Information (Continued)



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Note: A 74HC221A may be substituted for the 74HC423A Pin 6 and Pin 14 must be hardwired to GND

Components

R1: 4.7k C1: 10 μF
R2: 10k C2: 50 pF

FIGURE 6. Circuit for Clear and Load Pulse Generation

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74ACT 715 P C QR

Temperature Range Family
- 74ACT = Commercial TTL-Compatible
- 54ACT = Military TTL-Compatible

Device Type
- 715 = Default: CLOCK Disabled
- 715-R = Default: CLOCK Enabled

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- L = Leadless Chip Carrier (LCC)
- S = Small Outline (SOIC)

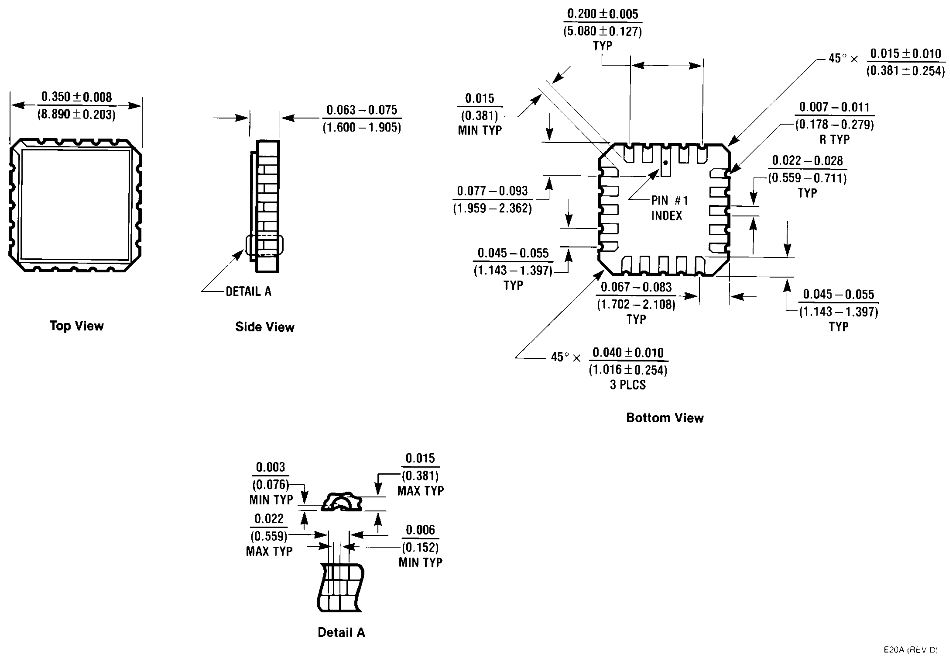
Special Variations
- X = Devices shipped in 13″ reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes.

Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

OR

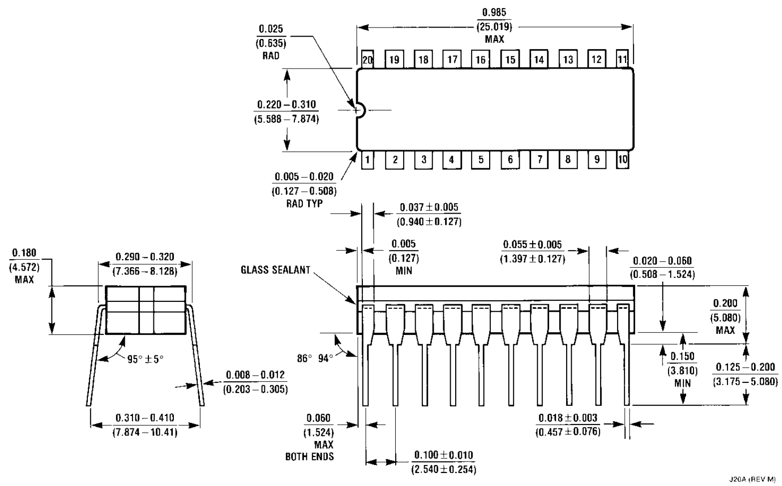
Default: CLOCK Disabled	LM1882CM = Commercial Small Outline (SOIC) LM1882CN = Commercial Plastic DIP LM1882J/883 = Military Ceramic Dip LM1882E/883 = Military Leadless Chip Carrier
Default CLOCK Enabled	LM1882-RCM = Commercial Small Outline (SOIC) LM1882-RCN = Commercial Plastic DIP LM1882-RJ/883 = Military Ceramic Dip LM1882-RE/883 = Military Leadless Chip Carrier

Physical Dimensions inches (millimeters)

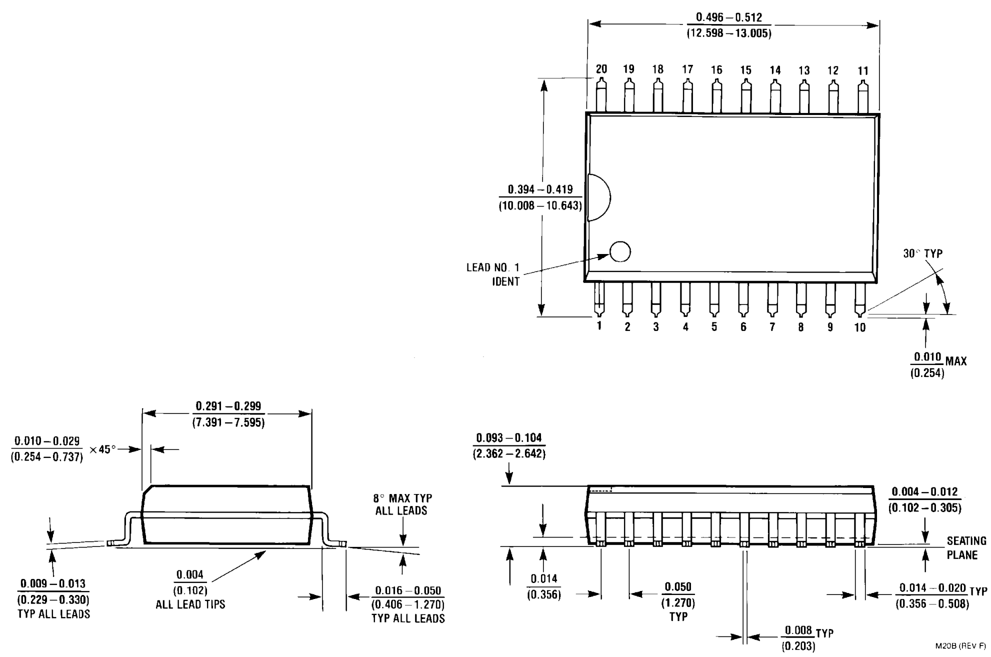


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

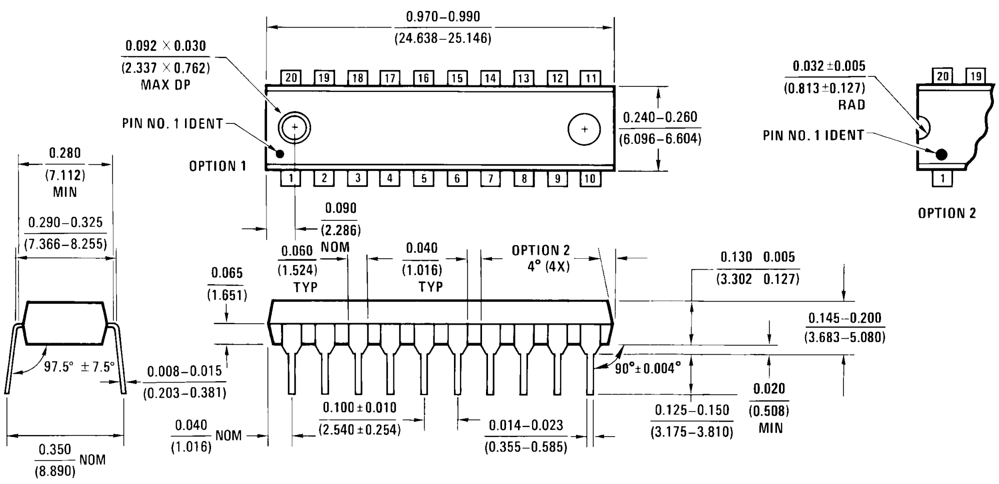


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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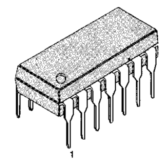
Fax: 81-043-299-2408

QUAD OPERATIONAL AMPLIFIERS

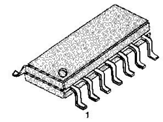
The LM224 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide voltage range.
Operation from split power supplies is also possible so long as the difference between the two supplies is 3 volts to 32 volts.

Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

14 DIP



14 SOP



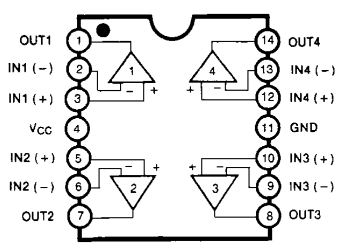
FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: LM224/A, LM324/A: 3V ~32V (or ±1.5 ~ 15V)
  LM2902: 3V~26V (or ±1.5V ~ 13V)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to V_{CC} -1.5V DC
- Power drain suitable for battery operation.

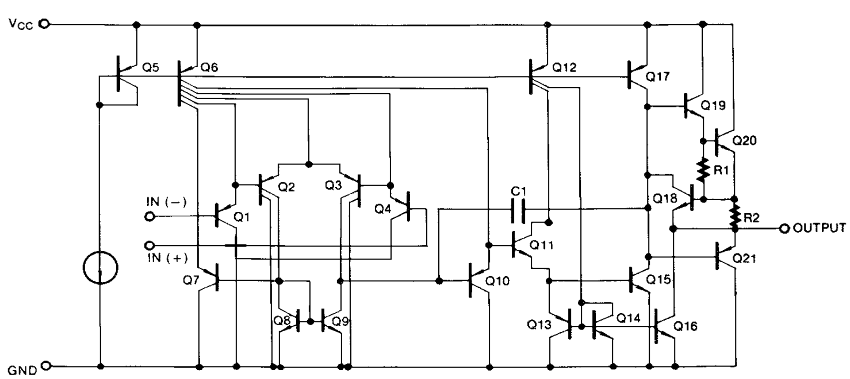
ORDERING INFORMATION

Device	Package	Operating Temperature
LM324N LM324AN	14 DIP	0 ~ + 70°C
LM324M LM324AM	14 SOP	
LM224N LM224AN	14 DIP	-25 ~ +85 °C
LM224M LM224AM	14 SOP	
LM2902N	14 DIP	-40 ~ + 85 °C
LM2902M	14 SOP	

BLOCK DIAGRAM



SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM224/LM224A	LM324/LM324A	LM2902	Unit
Power Supply Voltage	V_{CC}	±18 or 32	±18 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	V_I	-0.3 to + 32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND $V_{CC}\leq 15V$ $T_A=25\,°C$(One Amp)		Continuous	Continuous	Continuous	
Power Dissipation	P_D	570	570	570	mW
Operating Temperature Range	T_{OPR}	-25 ~ +85	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	-65 ~ + 150	-65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, V_{EE}=GND, T_A=25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM224			LM324			LM2902			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V, $V_{O(P)}$ = 1.4V, R_S = 0Ω			1.5	5.0		1.5	7.0		1.5	7.0	mV
Input Offset Current	I_{IO}				2.0	30		3.0	50		3.0	50	nA
Input Bias Current	I_{BIAS}				40	150		40	250		40	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V (V_{CC} = 26V for KA2902)		0		V_{CC} -1.5	0	V_{CC} -1.5		0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞,V_{CC} = 30V (all Amps)			1.0	3		1.0	3		1.0	3	mA
		R_L = ∞,V_{CC} = 5V (all Amps) (V_{CC} = 26V for KA2902)			0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, $R_L\geq$2KΩ, $V_{O(P)}$ = 1V to 11V		50	100		25	100			100		V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V	R_L = 2KΩ	26			26			22			V
		V_{CC}=26V for 2902	R_L = 10KΩ	27	28		27	28		23	24		V
	$V_{O(L)}$	V_{CC} = 5V, $R_L\geq$10KΩ			5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	75		50	75		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120			120		dB
Short Circuit to GND	I_{SC}				40	60		40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V, V_{CC} = 15V, $V_{O(P)}$ = 2V		20	40		20	40		20	40		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V, V_{CC} = 15V, $V_{O(P)}$ = 2V		10	13		10	13		10	13		mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V, V_{CC} = 15V,$V_{O(R)}$ = 200mV		12	45		12	45					µA
Differential Input Voltage	$V_{I(DIFF)}$					V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of -25 °C ≤ T_A ≤ + 85 °C for the LM224; and the 0 °C ≤ T_A ≤ +70 °C for the LM324 ; and the - 40 °C ≤ T_A ≤ +85 °C for the LM2902

Characteristic	Symbol	Test Conditions	LM224			LM324			LM2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{ICM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω			7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$			7.0			7.0			7.0		μV/ °C
Input Offset Current	I_{IO}				100			150			200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$			10			10			10		pA/ °C
Input Bias Current	I_{BIAS}				300			500			500	nA
Input Common-Mode Voltage Range	$V_{IC(R)}$	V_{CC} = 30V (V_{CC} = 26V for KA2902)	0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L ≥ 2.0KΩ $V_{O(P)}$ = 1V to 11V	25			15			15			V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26			26			22			V
		V_{CC} =26V for 2902, R_L = 10KΩ	27	28		27	28		23	24		V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ		5	20		5	20		5	100	mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	20		10	20		10	20		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	13		5	8		5	8		mA
Differential Input Voltage	$V_{I(DIFS)}$				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC}=50V, V_{EE} = GND, T_A=25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM224A			LM324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0 Ω		1.0	3.0		1.5	3.0	mV
Input Offset Current	I_{IO}			2	15		3.0	30	nA
Input Bias Current	I_{BIAS}			40	80		40	100	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current (All Amps)	I_{CC}	V_{CC} = 30V		1.5	3		1.5	3	mA
		V_{CC} = 5V		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, $R_L \geq$ 2 KΩ $V_{O(P)}$ = 1V to 11V	50	100		25	100		V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2 KΩ	26			26			V
		V_{CC} = 26V for 2902, R_L = 10 KΩ	27	28		27	28		V
	$V_{O(L)}$	V_{CC} = 5V, $R_L \geq$ 10 KΩ		5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I_{SC}			40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V	20	40		20	40		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	20		10	20		mA
		$V_{I(+)}$ = 0v, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 200mV	12	50		12	50		μA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of -25°C ≤ T_A ≤ + 85 °C for the LM224A; and the 0 °C ≤ T_A ≤+70 °C for the LM324A

Characteristic	Symbol	Test Conditions		LM224A			LM324A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω				4.0			5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				7.0	20		7.0	30	μV/ °C
Input Offset Current	I_{IO}					30			75	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10	200		10	300	pA/ °C
Input Bias Current	I_{BIAS}				40	100		40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V		0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥ 2.0KΩ		25			15			V/mV
Output Voltage Swing	$V_{O(P-P)}$	V_{CC} = 30V	R_L = 2KΩ	26			26			V
			R_L = 10KΩ	27	28		27	28		V
		V_{CC} = 5V, R_L≥ 10KΩ			5	20		5	20	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V		10	20		10	20		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V		5	8		5	8		mA
Differential Input Voltage	$V_{I(DIFF)}$					V_{CC}			V_{CC}	V

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 INPUT VOLTAGE RANGE

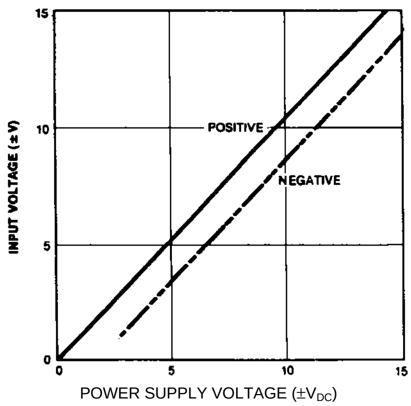


Fig. 2 INPUT CURRENT

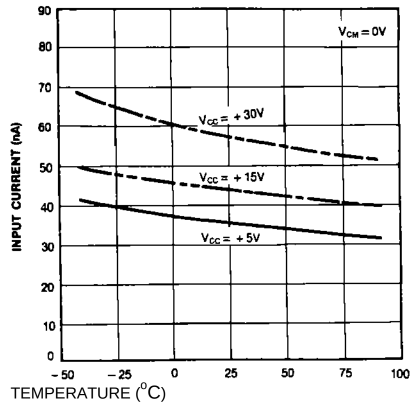


Fig. 3 SUPPLY CURRENT

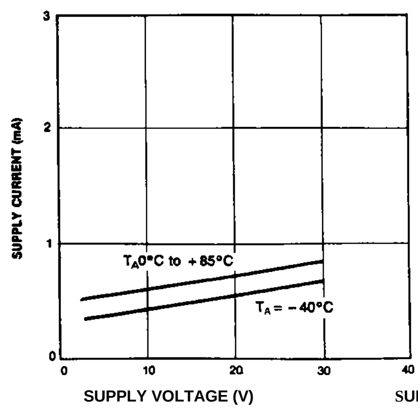


Fig. 4 VOLTAGE GAIN

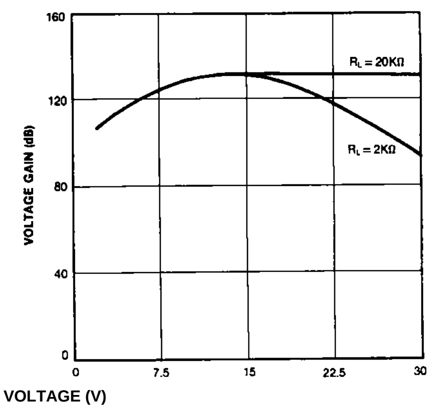


Fig. 5 OPEN LOOP FREGUENCY RESPONSE

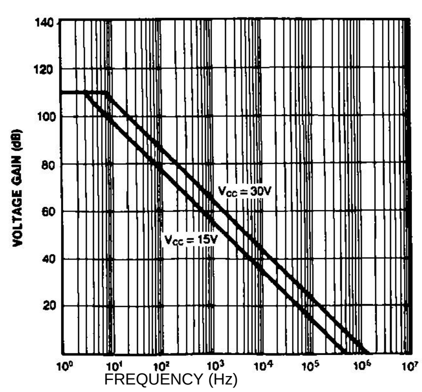


Fig. 6 COMMON.MOOE REJECTION RATIO

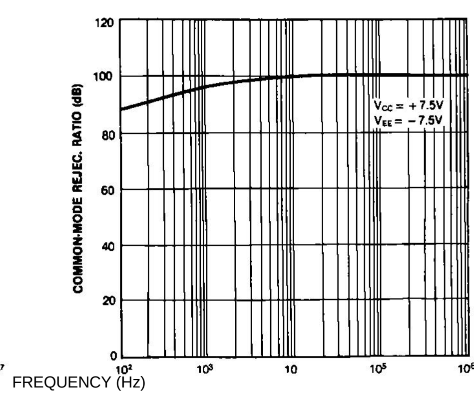


Fig.7 SLEW RATE

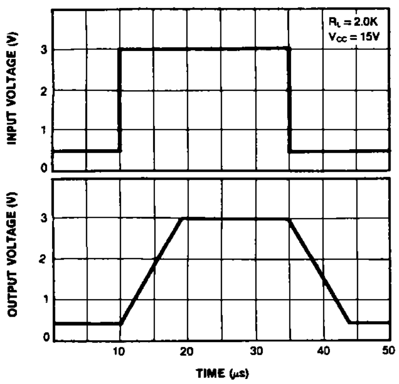


Fig. 8 VOLTAGE FOLLOWER PULSE

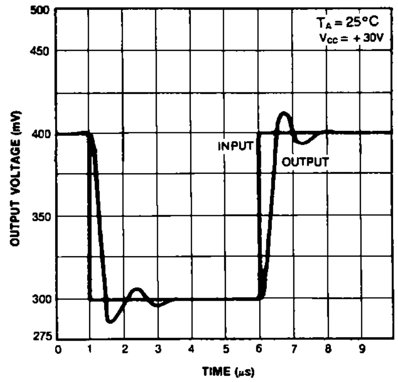
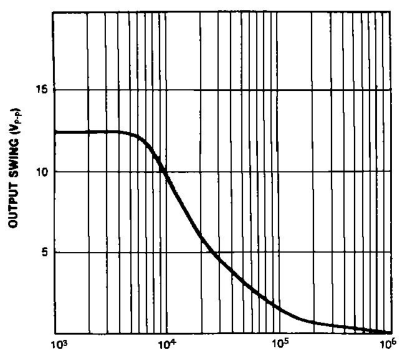
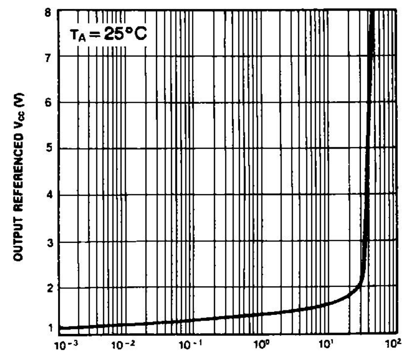


Fig. 9 LARGE SIGNAL FREQUECY RESPONSE



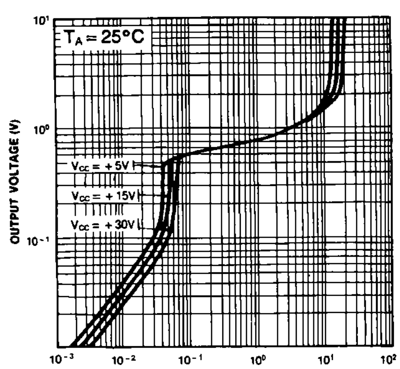
FREQUENCY (Hz)

Fig. 10 OUTPUT CHARACTERISTICS CURRENT SOURCING



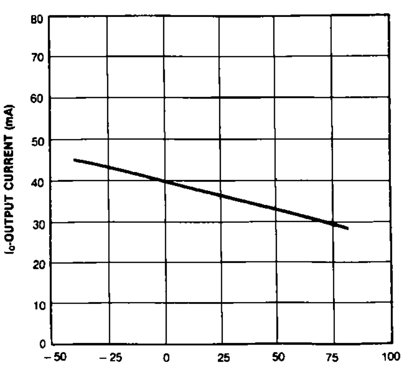
OUTPUT SOURCE CURRENT (mA)

Fig. 11 OUTPUT CHARACTERISTICS CURRENT SINKING



OUTPUT SINK CURRENT (mA)

Fig. 12 CURRENT LIMITING



TEMPERATURE (^{0}C)

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GTO™
HiSeC™

ISOPLANAR™
MICROWIRE™
POP™
PowerTrench™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

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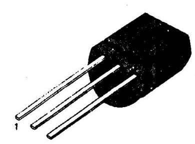
PROGRAMMABLE SHUNT REGULATOR

The LM336-2.5/B integrated Circuits are precision 2.5V shunt regulators. The monolithic IC voltage references operates as a low temperature coefficient 2.5V zener with 0.2Ω dynamic impedance.
A third terminal on the KA336-2.5/B allow the reference voltage and temperature coefficient to be trimmed easily.
LM3362.5/B are useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from low voltage supplies. Further, since the LM336-2.5/B operate as shunt regulators, they can be used as either a positive or negative voltage reference.

TO-92



1: Adj. 2: + 3: -

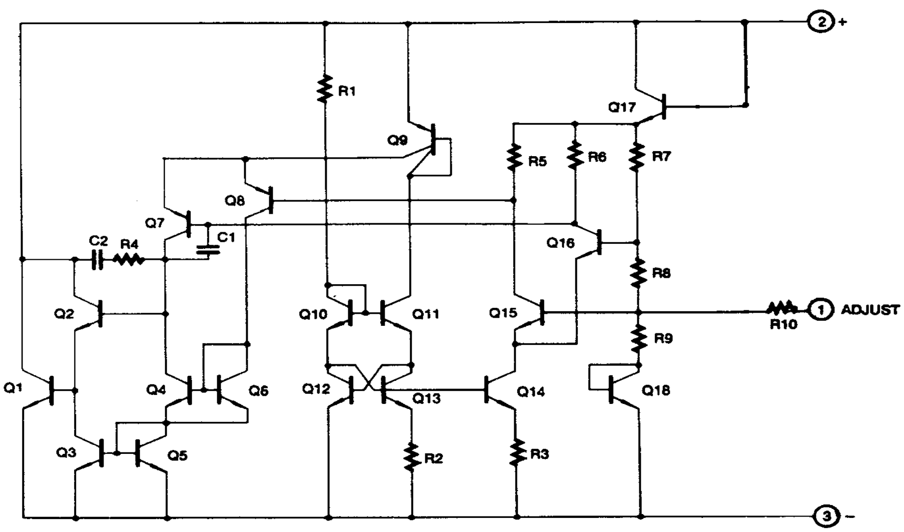
FEATURES

- Low temperature coefficient
- Guaranteed temperature stability 4mV typical
- 0.2 Ω dynamic impedance
- ±1.0% initial tolerance available.
- Easily trimmed for minimum temperature drift

ORDERING INFORMATION

Device	Package	Operating Temperature
LM336Z-2.5	TO-92	0 ~ +70°C
LM336Z-2.5B		
LM236Z-2.5		-25 ~ +85°C

SCHEMATIC DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Reverse Current	I_R	15	mA
Forward Current	I_F	10	mA
Operating Temperature Range LM336-2.5/B LM236-2.5	T_{OPR}	0 ~ + 70 - 25 ~ +85	°C °C
Storage Temperature Range	T_{STG}	- 60 ~ + 150	°C

ELECTRICAL CHARACTERISTICS ($T_{MIN} < T_A < T_{MAX}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM336/236			LM336B			
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	V_R	$T_A = +25°C$ $I_R = 1mA$	2.44	2.49	2.54	2.465	2.49	2.515	V
Reverse Breakdown Change with Current	$\Delta V_R/\Delta I_R$	$T_A = +25°C$ $400\mu A \le I_R \le 10mA$		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	Z_D	$T_A = +25°C$ $I_R = 1mA$		0.2	0.6		0.2	1	Ω
Temperature Stability	ST_T	$I_R = 1mA$ $T_{MIN} \le T_A \le T_{MAX}$		1.8	6		1.8	6	mV
Reverse Breakdown Change with Current	$\Delta V_R/\Delta I_R$	$T_{MIN} \le T_A \le T_{MAX}$ $400\mu A \le I_R \le 10mA$		3	10		3	12	mV
Reverse Dynamic Impedance	Z_D	$I_R = 1mA$ $T_{MIN} \le T_A \le T_{MAX}$		0.4	1		0.4	1.4	Ω
Long Term Stability	ST	$I_R = 1mA$ $T_{MIN} \le T_A \le T_{MAX}$		20			20		ppm

LM236: $T_{MIN} = -25°C$, $T_{MAX} = +85°C$
LM336: $T_{MIN} = 0°C$, $T_{MAX} = +70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1. Reverse Voltage Change

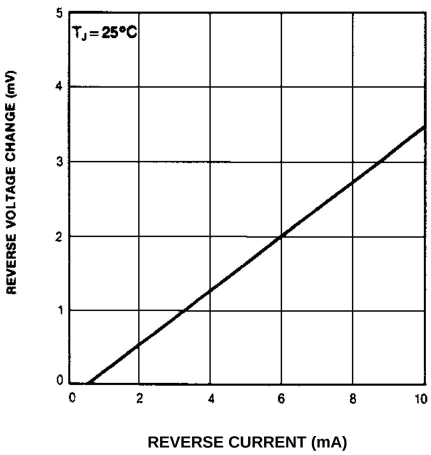


Fig. 2 Reverse Characteristics

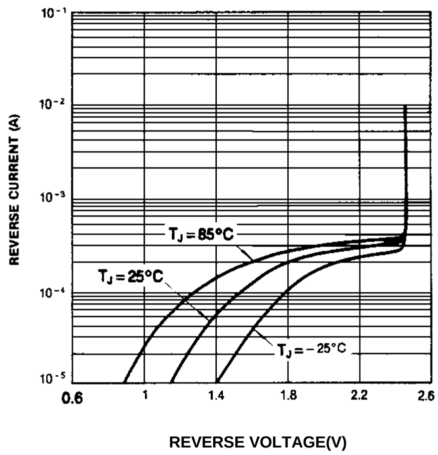


Fig. 3 Temperature Drift

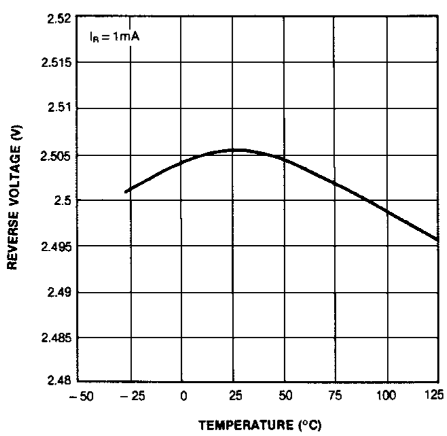
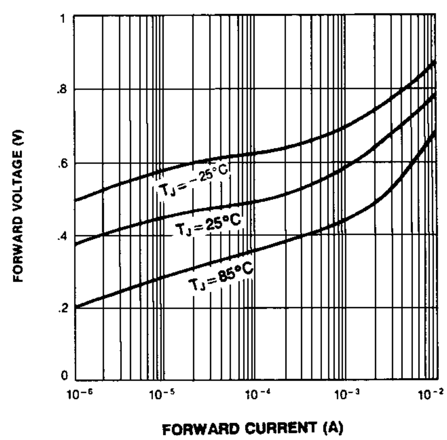


Fig. 4 Forward Characteristics



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HiSeC™

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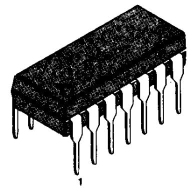
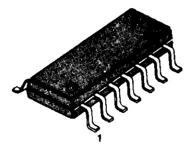
QUAD DIFFERENTIAL COMPARATOR

The LM239 series consists of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

14 DIP



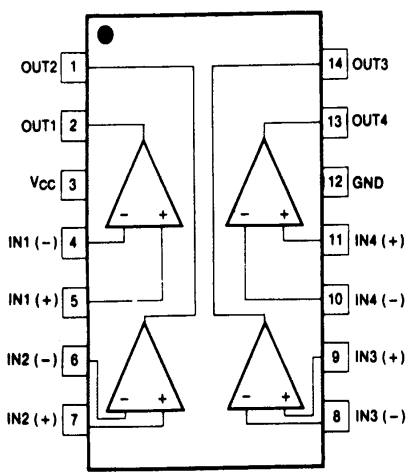
14 SOP



FEATURES

- Single or dual supply operation
- Wide range of supply voltage
  LM239/A, LM339/A, LM2901: 2 ~ 36V (or ±1 ~ ±18V)
  LM3302: 2 ~ 28V (or ±1 ~ ±14V)
- Low supply current drain 800µA Typ
- Open collector outputs for wired and connectors
- Low input bias current 25nA Typ
- Low Input offset current ±2.3nA Typ.
- Low input offset voltage ±1.4mV Typ.
- Common mode input voltage range includes ground.
- Low output saturation voltage
- Output compatible with TTL. DTL and MOS logic system

BLOCK DIAGRAM



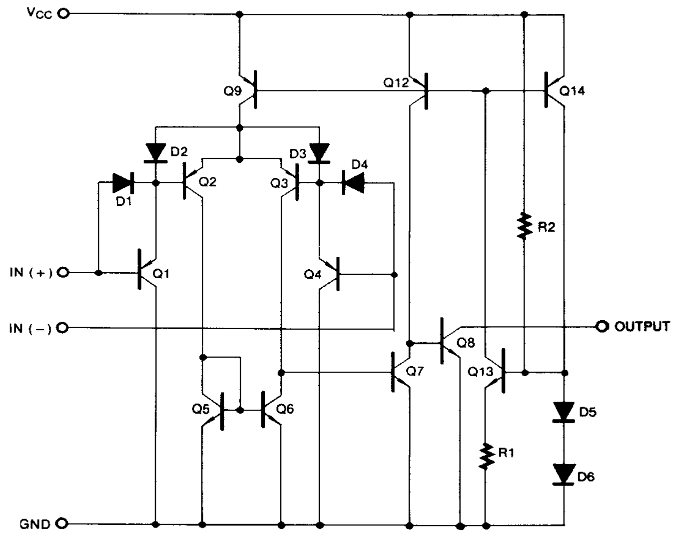
ORDERING INFORMATION

Device	Package	Operating Temperature
LM339N LM339AN	14 DIP	0 ~ +70°C
LM339M LM339AM	14 SOP	
LM239N LM239AN	14 DIP	-25 ~ + 85°C
LM239M LM239AM	14 SOP	
LM2901N	14 DIP	-40 ~ + 85°C
LM2901M	14 SOP	
LM3302N	14 DIP	
LM3302M	14 SOP	

FAIRCHILD
SEMICONDUCTOR TM

Rev. B

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18 or 36	V
Supply Voltage Only LM3302	V_{CC}	±14 or 28	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Differential Input Voltage Only LM3302	$V_{I(DIFF)}$	28	V
Input Voltage	V_I	- 0.3 to +36	V
Input Voltage Only LM3302	V_I	- 0.3 to +28	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM339/LM339A		0 ~ + 70	°C
LM239/LM239A	T_{OPR}	- 25 ~ + 85	°C
LM2901/LM3302		- 40 ~ + 85	°C
Storage Temperature	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM239A/LM339A			LM239/LM339			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V			±1	±2		±1.4	±5	mV
		$V_{O(P)}$ =1.4V, R_S =0Ω	NOTE 1			±4.0			±9.0	
Input Offset Current	I_{IO}				±2.3	±50		±2.3	±50	nA
			NOTE 1			±150			±150	
Input Bias Current	I_{BIAS}				57	250		57	250	nA
			NOTE 1			400			400	
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}		R_L = ∞		1.1	2.0		1.1	2.0	mA
Voltage Gain	G_V	V_{CC} =15V, R_L≥15KΩ(for large swing)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.4			1.4		µs
Output Sink Current	I_{SINK}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V, $V_{O(P)}$ ≤1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V			140	400		140	400	mV
		I_{SINK} =4mA	NOTE 1			700			700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V	$V_{O(P)}$ = 5V		0.1			0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0			1.0	µA
Differential Voltage	$V_{I(DIFF)}$		NOTE 1			36			36	V

Note 1.
LM339/A: 0≤T_A≤ +70°C
LM239/A: -25≤T_A≤ +85°C
LM2901/3302: -40≤T_A≤ +85°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2901			LM3302			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V			2	7		2	20	mV
		$V_{O(P)}$ =1.4V, R_S =0Ω	NOTE 1		9	15			40	
Input Offset Current	I_{IO}				2.3	50		3	100	nA
			NOTE 1		50	200			300	
Input Bias Current	I_{BIAS}				57	250		57	250	nA
			NOTE 1		200	500			1000	
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}		R_L =∞		1.1	2.0		1.1	2.0	mA
			R_L =∞, V_{CC} =30V		1.6	2.5				
Voltage Gain	G_V	V_{CC} =15V, R_L≥15KΩ(for large swing)		25	100		2	30		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.4			1.4		µs
Output Sink Current	I_{SINK}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V, $V_{O(P)}$ ≤1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V			140	400		140	400	mV
		I_{SINK} =4mA	NOTE 1			700			700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V	$V_{O(P)}$ = 5V		0.1			0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0			1.0	µA
Differential Voltage	$V_{I(DIFF)}$		NOTE 1			36			36	V

Note 1.
LM339/A: 0≤T_A≤ +70°C
LM239/A: -25≤T_A≤ +85°C
LM2901/3302: -40≤T_A≤ +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

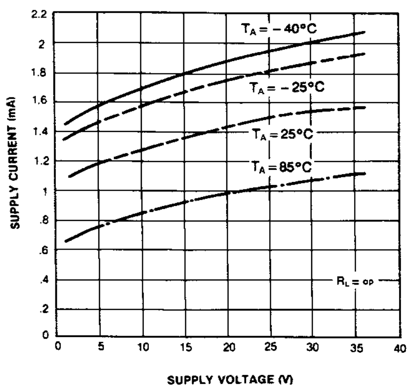


Fig. 2 INPUT CURRENT

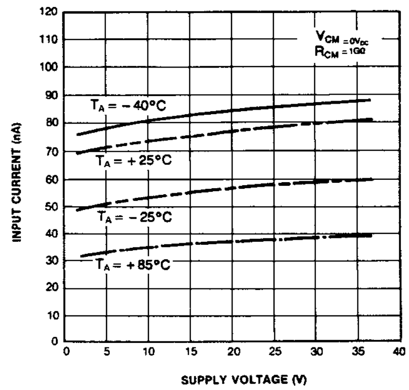


Fig. 3 OUTPUT SATURATION VOLTAGE

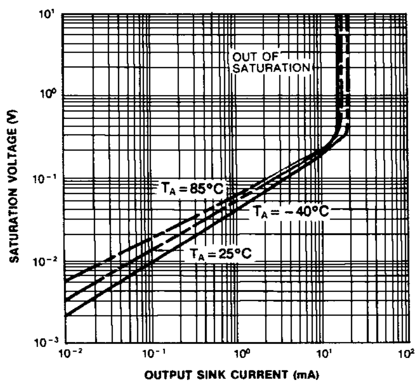


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

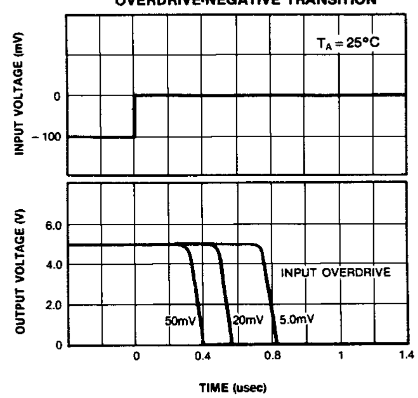
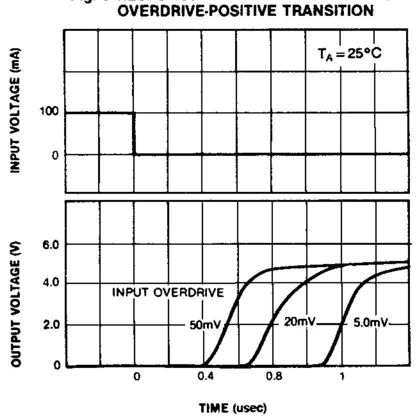


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



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E²CMOS™	PowerTrench™
FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
HiSeC™	TinyLogic™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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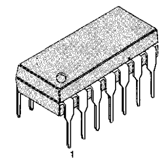
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

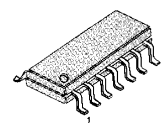
QUAD OPERATIONAL AMPLIFIERS

The LM248/LM348 is a true quad LM741. It consists of four independent, high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the Supply current of a single LM741 type OP Amp.
Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

14 DIP



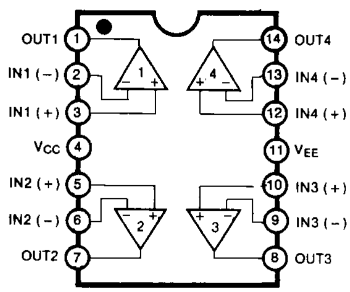
14 SOP



FEATURES

- LM741 OP Amp operating characteristics
- Low supply current drain
- Class AB output stage-no crossover distortion
- Pin compatible with the LM324 & LM3403
- Low input offset voltage: 1mV Typ.
- Low input offset current: 4nA Typ.
- Low input bias current: 30nA Typ.
- Gain bandwidth product for LM348 (unity gain): 1.0MHz Typ.
- High degree of isolation between amplifiers: 120dB
- Overload protection for inputs and outputs

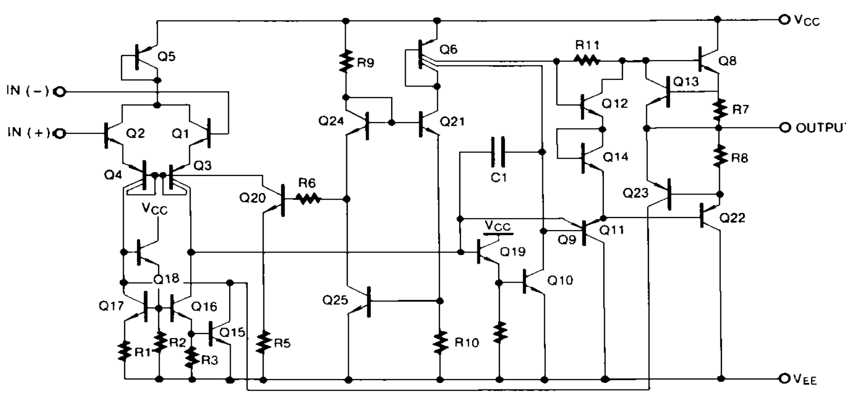
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM348N	14 DIP	0 ~ +70°C
LM348M	14 SOP	
LM248N	14 DIP	-25 ~ +85 °C
LM248M	14 SOP	

SCHEMATIC DIAGRAM (One Section Only)



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V_I	±18	V
Output Short Circuit Duration		Continuous	
Operating Temperature KA248	T_{OPR}	- 25 ~ +85	°C
KA348		0~ +70	°C
Storage Temperature	T_{STG}	- 65~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} =15V, V_{EE}= -15V, T_A=25 °C, unless otherwise specified)

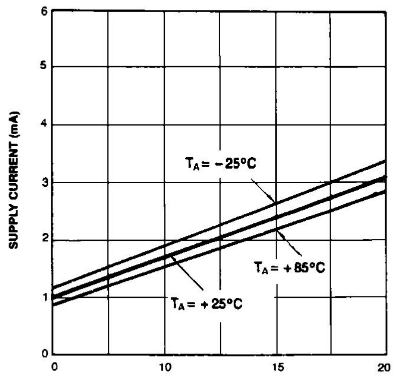
Characteristic	Symbol	Test Conditions		LM248			LM348			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤10KΩ			1	6.0		1	6.0	mV
			NOTE 1			7.5			7.5	
Input Offset Current	I_{IO}				4	50		4	50	nA
			NOTE 1			125			100	
Input Bias Current	I_{BIAS}				30	200		30	200	nA
			NOTE 1			500			400	
Input Resistance	R_I			0.8	2.5		0.8	2.5		MΩ
Supply Current (all Amplifiers)	I_{CC}				2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	G_V	R_L≥2KΩ		25	160		25	160		V/mV
			NOTE 1	15			15			
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB
Common Mode Input Voltage Range	$V_{I(R)}$	NOTE 1		±12			±12			V
Small Signal Bandwidth	BW	G_V = 1			1.0			1.0		MHz
Phase Margin	MPH	G_V = 1			60			60		Degree
Slew Rate	SR	G_V = 1			0.5			0.5		V/μs
Output Short Circuit Current	I_{SC}				25			25		mA
Output Voltage Swing	$V_{O(P.P)}$	R_L≥10KΩ	NOTE 1	±12	±13		±12	±13		V
		R_L≥2KΩ		±10	±12		+0	±12		
Common Mode Rejection Ratio	CMRR	R_S≥10KΩ	NOTE 1	70	90		70	90		dB
Power Supply Rejection Ratio	PSRR	R_S≥10KΩ	NOTE 1	77	96		77	96		dB

NOTE 1

LM348: 0 ≤ T_A ≤ +70°C
LM248: -25 ≤ T_A ≤ +85 °C

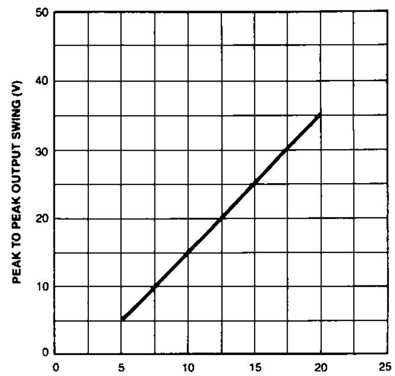
TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT



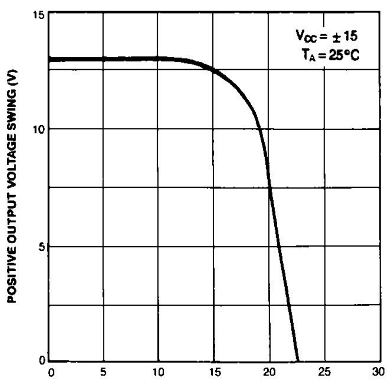
SUPPLY VOLTAGE (±V)

Fig. 2 VOLTAGE SWING



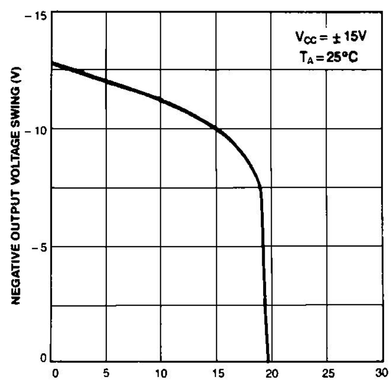
SUPPLY VOLTAGE (±V)

Fig. 3 SOURCE CURRENT LIMIT



OUTPUT SOURCE CURRENT (mA)

Fig. 4 SINK CURRENT LIMIT



OUTPUT SINK CURRENT (mA)

Fig. 5 OUTPUT IMPEDANCE

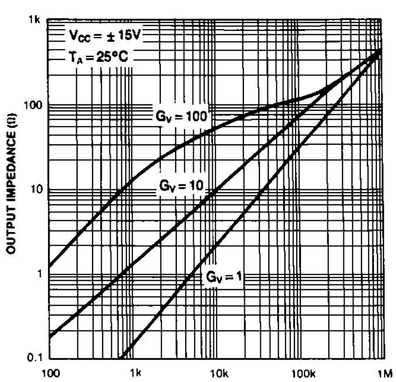


Fig. 6 COMMON-MODE REJECTION RATIO

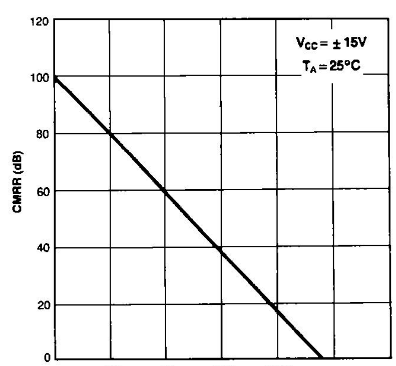
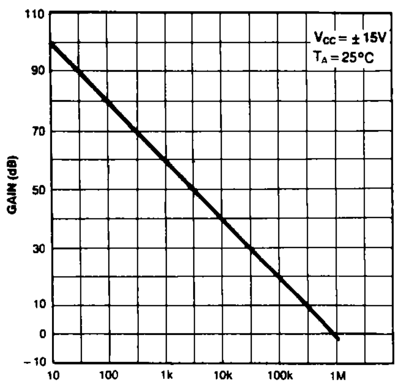
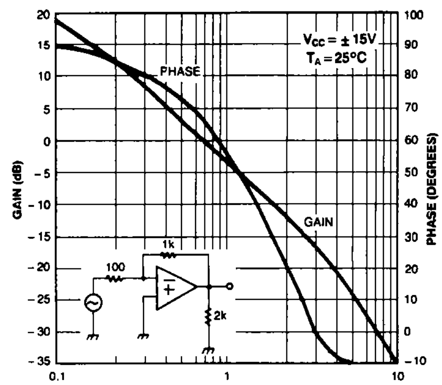


Fig. 7 OPEN LOOP FREGUENCV RESPONSE



FREQUENCYN (Hz)

Fig. 8 BODE PLOT



FREQUENCY (MHz)

Fig. 9 LARGE SIGNAL PULSE RESPONSE

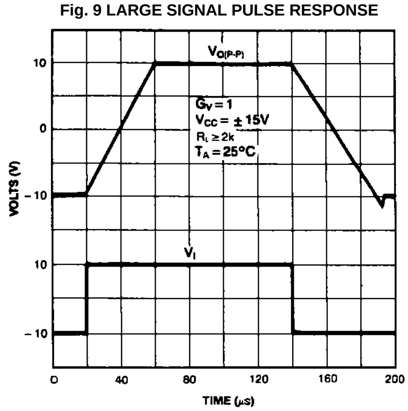


Fig. 10 SMALL SIGNAL PULSE RESPONSE

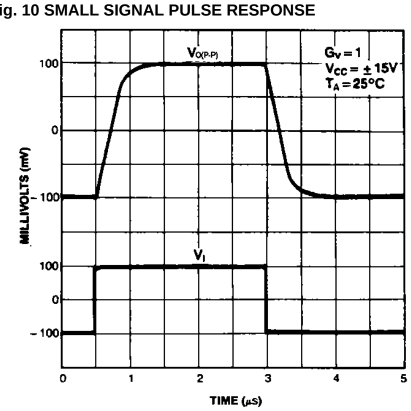
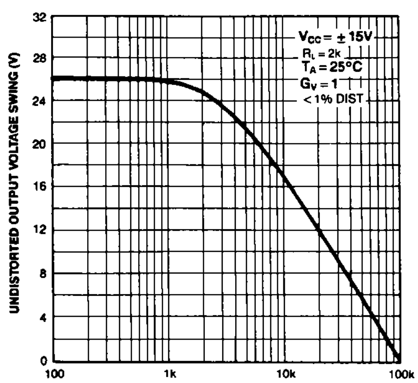
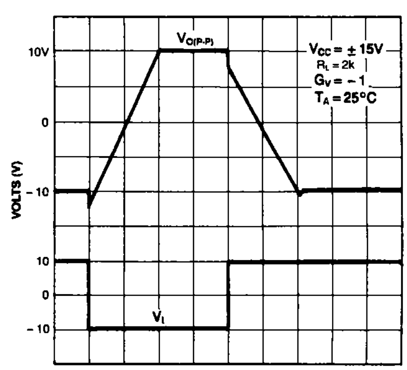


Fig. 11 UNDISTORTED OUTPUT VOLTAGE SWING



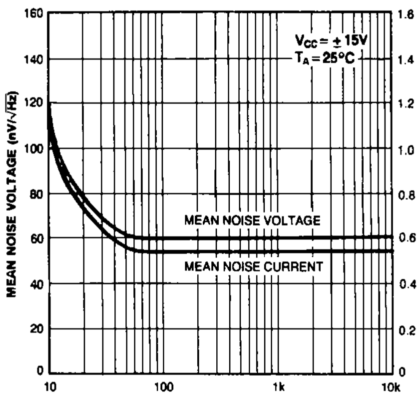
FREQUENCY (Hz)

Fig. 12 INVERTING LARGE SIGNAL PULSE RESPONSE



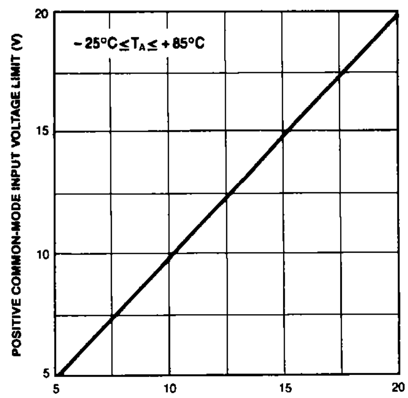
TIME (μs)

Fig. 13 INPUT NOISE VOLTAGE AND NOISE CURRENT



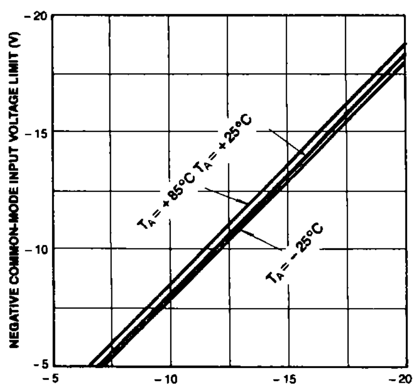
FREQUENCY (Hz)

Fig. 14 POSITIVE COMMON MODE INPUT VOLTAGE LIMIT



POSITIVE SUPPLY (V)

Fig. 15 NEGATIVE COMMON.MODE INPUT VOLTAGE LIMFY



NEGATIVE SUPPLY VOLTS(V)

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PRODUCT STATUS DEFINITIONS

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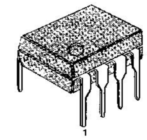
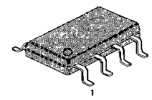
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

DUAL OPERATIONAL AMPLIFIERS

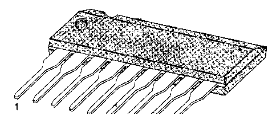
The LM258 series consists of four independent, high gain, internally Frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.
Operation from split power supplies is also possible and the low power Supply current drain is independent of the magnitude of the power Supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single 8 SOP power supply system.

8 DIP





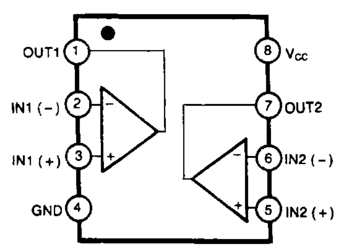
9 SIP

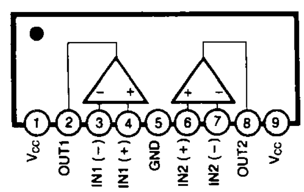


FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: LM258/A, LM358/A: 3V~32V (or ±1.5V~16V)
  LM2904: 3V~26V (or ±1.5V~13V)
- Input common-mode voltage range Includes ground
- Large output voltage swing: 0V DC to Vcc - 1.5V DC
- Power drain suitable for battery operation.

BLOCK DIAGRAM

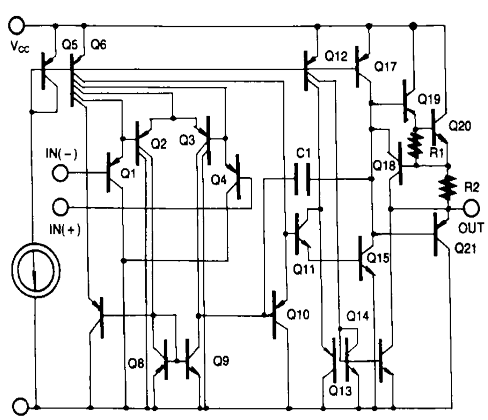




ORDERING INFORMATION

Device	Package	Operating Temperature
LM358N LM358AN	8 DIP	0 ~ + 70°C
LM358S LM358AS	9 SIP	
LM358M LM358AM	8 SOP	
LM258N LM258AN	8 DIP	-25 ~ + 85 °C
LM258S LM258AS	9 SIP	
LM258M LM258AM	8 SOP	
LM2904N	8 DIP	-40 ~ + 85 °C
LM2904S	9 SIP	
LM2904M	8 SOP	

SCHEMATIC DIAGRAM (One section only)



Rev. B

FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Supply Voltage	V_{CC}	±16 or 32	±16 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq V$, T_A = 25 °C(One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{OPR}	-25 ~ + 85	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	-65 ~ + 150	-65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, T = 25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM258			LM358			LM2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} -1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω		2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I_{IO}			3	30		5	50		5	50	nA
Input Bias Current	I_{BIAS}			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V (KA2904, V_{CC} = 26V)	0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V (KA2902, V_{CC} = 26V)		0.8	2.0		0.8	2.0		0.8	2.0	mA
		R_L = ∞,over full temperature range		0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ $V_{O(P)}$ = 1V to 11V	50	100		25	100		25	100		V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26			26			22			V
		V_{CC} = 26V for 2904, R_L = 10KΩ	27	28		27	28		23	24		V
	$V_{O(L)}$	V_{CC} = 5V, $R_L \geq 10K\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I_{SC}			40	60		40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30		10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	15		10	15		10	15		mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 200mA	12	100		12	100					μA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, V_{EE}=GND, unless otherwise specified)
The following specification apply over the range of - 25 °C ≤ T_A ≤ + 85 °C for the KA258; and the 0 °C ≤ T_A ≤ + 70 °C for the LM358; and the -40 °C ≤ T_A ≤ +85 °C for the LM2904

Characteristic	Symbol	Test Conditions		LM258			LM358			LM2904			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω				7.0			9.0			10.0	mV
Input Offset Voltage Drift	V_{IO}	R_S = 0Ω			7.0			7.0			7.0		μV/ °C
Input Offset Current	I_{IO}					100			150		45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10			10			10		pA/ °C
Input Bias Current	I_{BIAS}				40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V (KA2904,V_{CC} = 26V)		0		V_{CC} =2.0	0		V_{CC} =2.0	0		V_{CC} =2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2.0KΩ $V_{O(P)}$ = 1V to 11V		25			15			15			V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V	R_L = 2KΩ	26			26			26			V
		V_{CC} = 26V for 2904	R_L = 10KΩ	27	28		27	28		27	28		V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ			5	20		5	20		5	20	mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	30		10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V		5	8		5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$					V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V. V_{EE}=GND. T_A=25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM258A			LM358A			Unit
				Min	Typ	Max	MIn	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω			1.0	3.0		2.0	3.0	mV
Input Offset Current	I_{IO}				2	15		5	30	nA
Input Bias Current	I_{BIAS}				40	80		45	100	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V		0		V_{CC} =1.5	0		V_{CC} =1.5	V
Supply Current	I_{CC}	R_L = ∞,V_{CC} = 30V			0.8	2.0		0.8	2.0	mA
		RL = ∞,over full temperature range			0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2KΩ V_O = 1V to 11V		50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	R_L = 2KΩ	26			26			V
		V_{CC} = 26V for 2904	R_L = 10KΩ	27	28		27	28		V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ			5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	85		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB
Short Circuit to GND	I_{SC}				40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		20	30		20	30		mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	15		10	15		mA
		V_{in+} = 0V, V_{in-} = 1V $V_{O(P)}$ = 200mV		12	100		12	100		μA
Differential Input Voltage	$V_{I(DIFF)}$					V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_{EE} = GND. unless otherwise specified)

The following specification apply over the range of -25 °C ≤ T_A ≤ +85 °C for the LM258A; and the 0 °C ≤ T_A ≤ +70 °C for the LM358A

Characteristic	Symbol	Test Conditions		LM258A			LM358A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω				4.0			5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				7.0	15		7.0	20	μV/°C
Input Offset Current	I_{IO}					30			75	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10	200		10	300	pA/°C
Input Bias Current	I_{BIAS}				40	100		40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V		0		Vcc =2.0	0		Vcc =2.0	V
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V	R_L = 2KΩ	26			26			V
		V_{CC} = 30V	R_L = 10KΩ	27	28		27	28		V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ			5	20		5	20	mV
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2.0KΩ $V_{O(P)}$ = 1V to 11V		25			15			V/mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	30		10	30		mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$					V_{CC}			V_{CC}	V

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

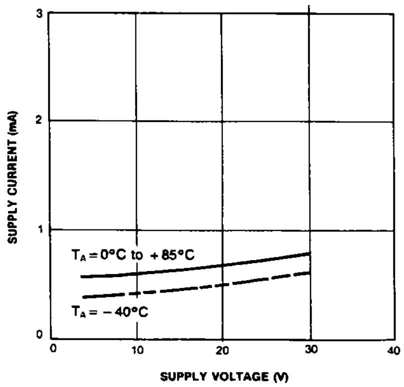


Fig. 2 VOLTAGE GAIN

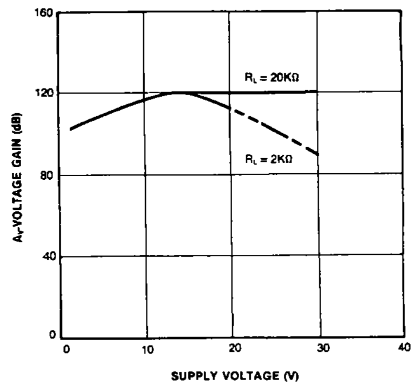


Fig. 3 OPEN LOOP FREQUENCY RESPONSE

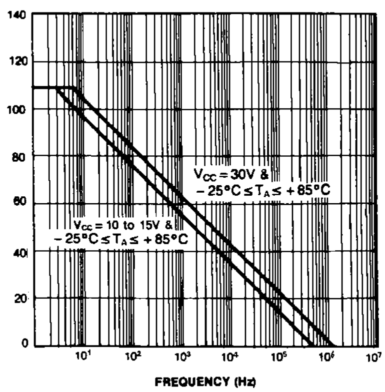


Fig. 4 LARGE SIGNAL FREQUENCY

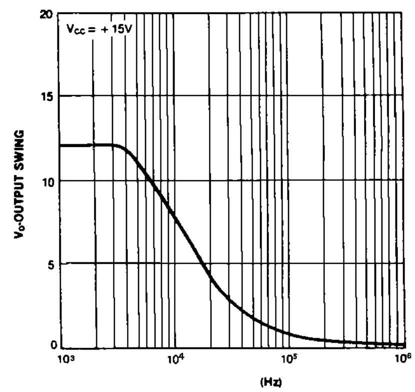


Fig. 5 OUTPUT CHARACTERISTICS CURRENT SOURCING

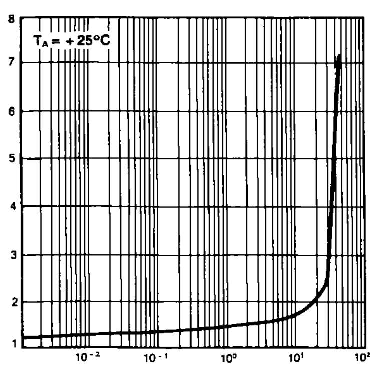


Fig. 6 OUTPUT CHARACTERISTICS CURRENT SINKING

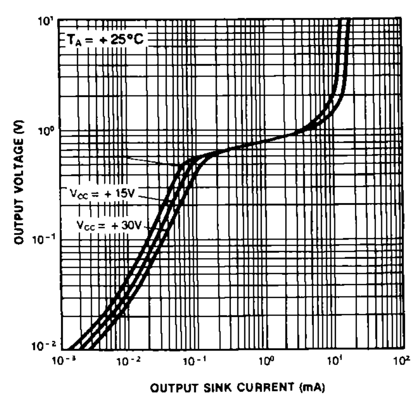


Fig. 7 INPUT VOLTAGE RANGE

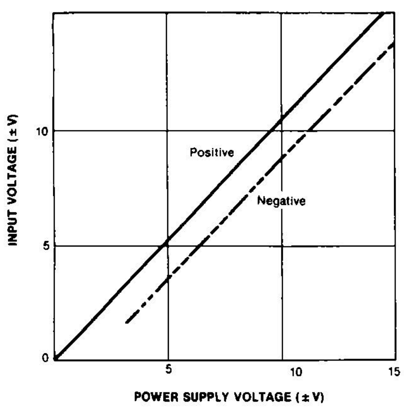


Fig. 8 COMMON-MODE REJECTION RATIO

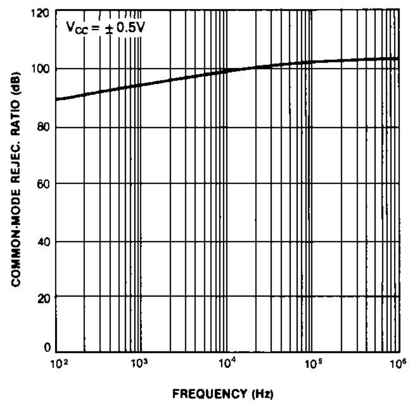


Fig. 9 CURRENT LIMITING

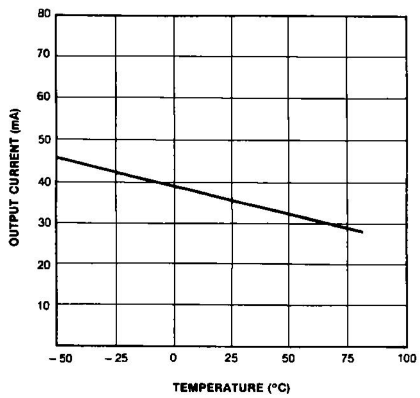


Fig. 10 INPUT CURRENT

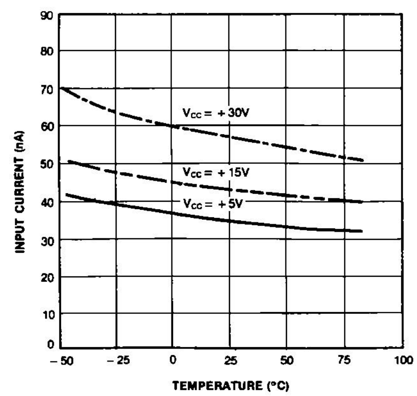


Fig. 11 VOLTAGE FOLLOWER PULSE RESPONSE

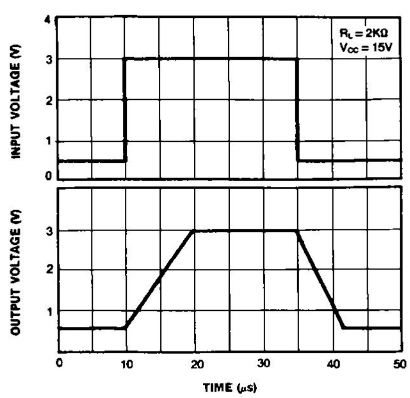
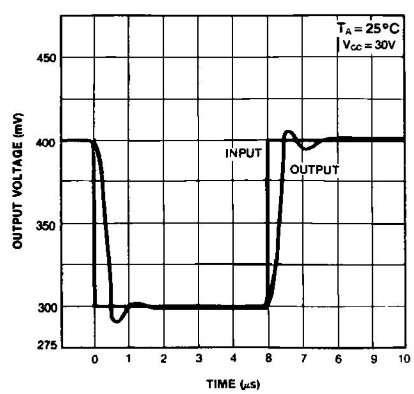


Fig. 12 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



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FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

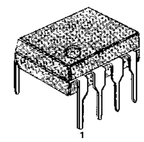
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

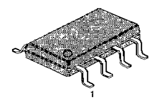
DUAL DIFFERENTIAL COMPARATOR

The LM/KA293 series consists of two independent voltage comparators designed to operate from a single power supply over a wide voltage range.

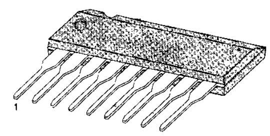
8 DIP



8 SOP



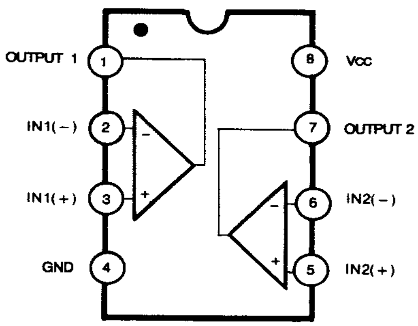
9 SIP

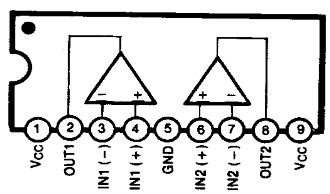


FEATURES

- Single Supply Operation: 2V to 36V
- Dual Supply Operation: ± 1V to ±18V
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800µA Typ
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ
- Low Input Offset Current ±5nA WP
- Low Offset Voltage ±1mV Typ

BLOCK DIAGRAM

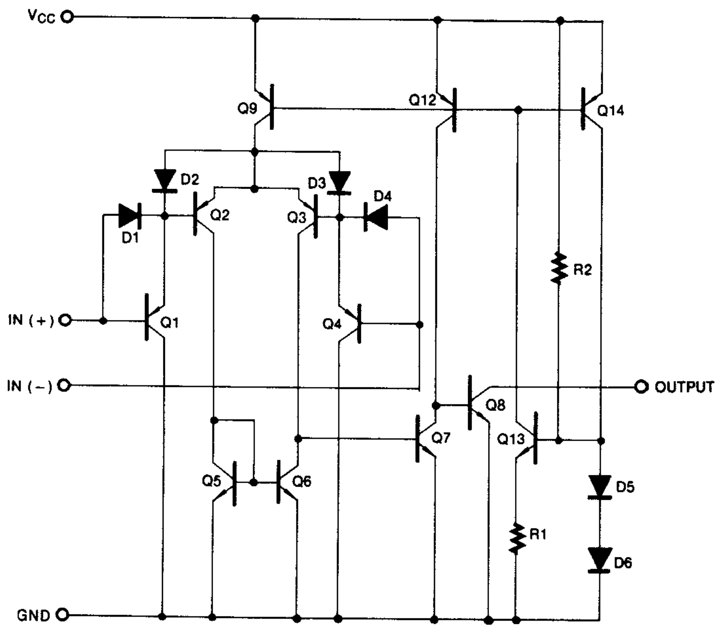




ORDERING INFORMATION

Device	Package	Operating Temperature
LM393N (KA393) LM393AN (KA393A)	8 DIP	0 ~ + 75°C
KA393S KA393AS	9 SIP	
LM393M (KA393D) KA393AD	8 SOP	
KA293 KA293A	8 DIP	-25 ~ + 85°C
KA293S KA293AS	9 DIP	
KA293D KA293AD	8 SOP	
KA2903	8 DIP	-40 ~ + 85°C
KA2903D	8 SOP	
KA2903S	9 SIP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V_I	- 0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM393/LM393A LM293/LM293A LM2903	T_{OPR}	0 ~ + 70 - 25 ~ + 85 - 40 ~ + 85	°C
Storage Temperature	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} =5V, T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM293A/LM393A Min	LM293A/LM393A Typ	LM293A/LM393A Max	LM293/LM393 Min	LM293/LM393 Typ	LM293/LM393 Max	Unit
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V			±1	±2		±1	±5	mV
		$V_{O(P)}$ =1.4V, R_S =0Ω	NOTE 1			±4.0			±9.0	
Input Offset Current	I_{IO}				±5	±50		±5	±50	nA
			NOTE 1			±150			±150	
Input Bias Current	I_{BIAS}				65	250		65	250	nA
			NOTE 1			400			400	
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}	R_L = ∞			0.6	1		0.6	1	mA
		R_L = ∞, V_{CC} = 30V			0.8	2.5		0.8	2.5	
Voltage Gain	G_V	V_{CC} =15V, R_L≥15KΩ (for large $V_{O(P-P)swing}$)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.4			1.4		µs
Output Sink Current	I_{SINK}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V, $V_{O(P)}$≤1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$≥1V, VI(+) =0V			160	400		160	400	mV
		I_{SINK} = 4mA	NOTE 1			700			700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V,	$V_{O(P)}$ = 5V		0.1			0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0			1.0	µA

NOTE 1
LM393/A: 0≤T_A≤ +70°C
LM293/A: -25≤T_A≤ +85°C
LM2903: -40≤T_A≤ +85°C

ELECTRICAL CHARACTERISTICS (V_{CC} =5V, T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2903 Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V			±1	±7	mV
		$V_{O(P)}$ =1.4V, R_S =0Ω	NOTE 1		±9	±15	
Input Offset Current	I_{IO}				±5	±50	nA
			NOTE 1		±50	±200	
Input Bias Current	I_{BIAS}				65	250	nA
			NOTE 1			500	
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	
Supply Current	I_{CC}	R_L = ∞			0.6	1	mA
		R_L = ∞, V_{CC} = 30V			1	2.5	
Voltage Gain	G_V	V_{CC} =15V, R_L≥15KΩ(for large $V_{O(P-P)swing}$)		25	100		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.5		μs
Output Sink Current	I_{SINK}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V, $V_{O(P)}$ ≤1.5V		6	16		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$≥1V, VI(+) =0V			160	400	mV
		I_{SINK} = 4mA	NOTE 1			700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V,	$V_{O(P)}$ = 5V		0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0	μA

NOTE 1
LM393/A: 0≤T_A≤ +70°C
LM293/A: -25≤T_A≤ +85°C
LM2903: -40≤T_A≤ +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

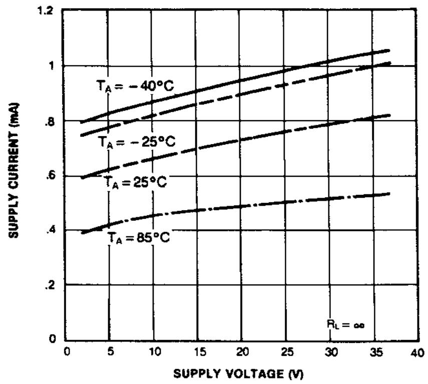


Fig. 2 INPUT CURRENT

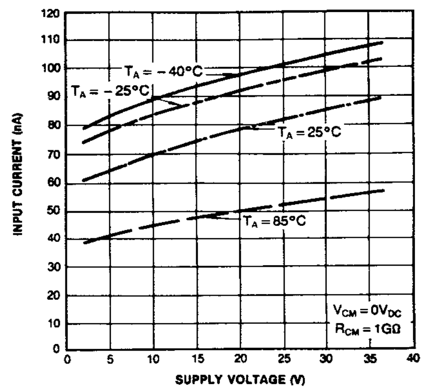


Fig. 3 OUTPUT SATURATION VOLTAGE

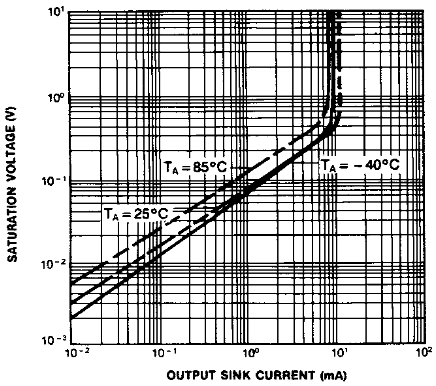


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

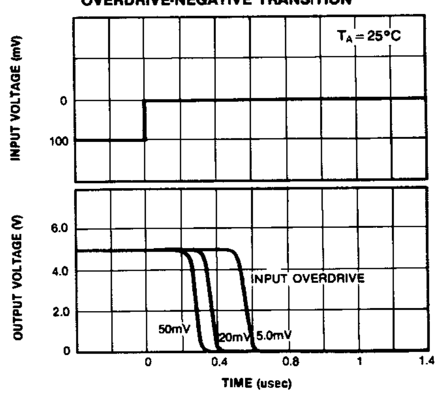
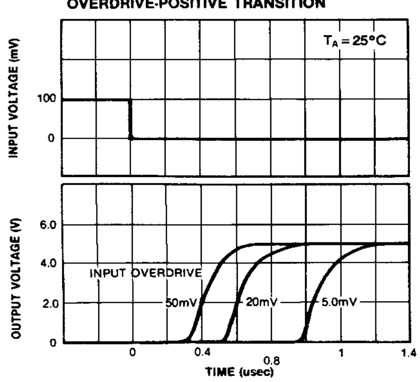


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



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As used herein:

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

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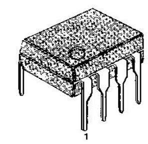
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

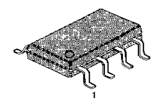
DUAL DIFFERENTIAL COMPARATOR

The LM293 series consists of two independent voltage comparators designed to operate from a single power supply over a wide voltage range.

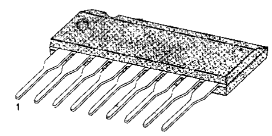
8 DIP

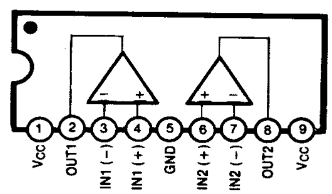


8 SOP



9 SIP

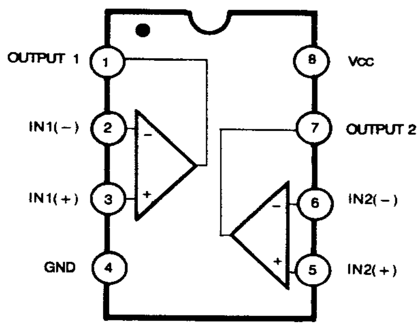




FEATURES

- Single Supply Operation: 2V to 36V
- Dual Supply Operation: ± 1V to ±18V
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800µA Typ
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ
- Low Input Offset Current ±5nA WP
- Low Offset Voltage ±1mV Typ

BLOCK DIAGRAM

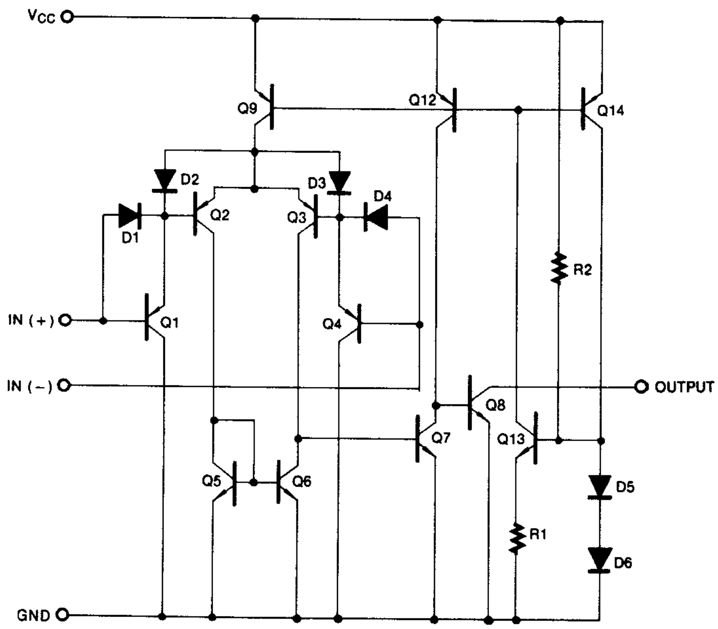


ORDERING INFORMATION

Device	Package	Operating Temperature
LM393N LM393AN	8 DIP	0 ~ + 75°C
LM393S LM393AS	9 SIP	
LM393M LM393AM	8 SOP	
LM293N LM293AN	8 DIP	-25 ~ + 85°C
LM293S LM293AS	9 DIP	
LM293M LM293AM	8 SOP	
LM2903N	8 DIP	-40 ~ + 85°C
LM2903M	8 SOP	
LM2903S	9 SIP	

FAIRCHILD SEMICONDUCTOR ™

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V_I	- 0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM393/LM393A LM293/LM293A LM2903	T_{OPR}	0 ~ + 70 - 25 ~ + 85 - 40 ~ + 85	°C
Storage Temperature	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} =5V, T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM293A/LM393A Min	LM293A/LM393A Typ	LM293A/LM393A Max	LM293/LM393 Min	LM293/LM393 Typ	LM293/LM393 Max	Unit
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V $V_{O(P)}$ =1.4V, R_S =0Ω			±1	±2		±1	±5	mV
			NOTE 1			±4.0			±9.0	mV
Input Offset Current	I_{IO}				±5	±50		±5	±50	nA
			NOTE 1			±150			±150	nA
Input Bias Current	I_{BIAS}				65	250		65	250	nA
			NOTE 1			400			400	nA
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	0		V_{CC}-2	V
Supply Current	I_{CC}	R_L = ∞			0.6	1		0.6	1	mA
		R_L = ∞, V_{CC} = 30V			0.8	2.5		0.8	2.5	mA
Voltage Gain	G_V	V_{CC} =15V, R_L≥15KΩ (for large $V_{O(P-P)swing}$)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.4			1.4		µs
Output Sink Current	I_{SINK}	$V_{I(-)}$≥1V, $V_{I(+)}$ =0V, $V_{O(P)}$≤1.5V		6	18		6	18		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$≥1V, VI(+) =0V			160	400		160	400	mV
		I_{SINK} = 4mA	NOTE 1			700			700	mV
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V,	$V_{O(P)}$ = 5V		0.1			0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0			1.0	µA

NOTE 1
LM393/A: 0≤T_A≤ +70°C
LM293/A: -25≤T_A≤ +85°C
LM2903: -40≤T_A≤ +85°C

ELECTRICAL CHARACTERISTICS (V_{CC} =5V, T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2903 Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	V_{CM} =0V to V_{CC} =1.5V			±1	±7	mV
		$V_{O(P)}$ =1.4V, R_S =0Ω	NOTE 1		±9	±15	
Input Offset Current	I_{IO}				±5	±50	nA
			NOTE 1		±50	±200	
Input Bias Current	I_{BIAS}				65	250	nA
			NOTE 1			500	
Input Common Mode Voltage Range	$V_{I(R)}$			0		V_{CC}-1.5	V
			NOTE 1	0		V_{CC}-2	
Supply Current	I_{CC}	$R_L = \infty$			0.6	1	mA
		$R_L = \infty$, V_{CC} = 30V			1	2.5	
Voltage Gain	G_V	V_{CC} =15V, $R_L \geq$15KΩ(for large $V_{O(P-P)swing}$)		25	100		V/mV
Large Signal Response Time	t_{RES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ			350		ns
Response Time	t_{RES}	V_{RL} =5V, R_L =5.1KΩ			1.5		µs
Output Sink Current	I_{SINK}	$V_{I(-)} \geq$1V, $V_{I(+)}$ =0V, $V_{O(P)} \leq$1.5V		6	16		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)} \geq$1V, VI(+) =0V			160	400	mV
		I_{SINK} = 4mA	NOTE 1			700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V,	$V_{O(P)}$ = 5V		0.1		nA
		$V_{I(+)}$ = 1V	$V_{O(P)}$ = 30V			1.0	µA

NOTE 1
LM393/A: 0≤T_A≤ +70°C
LM293/A: -25≤T_A≤ +85°C
LM2903: -40≤T_A≤ +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

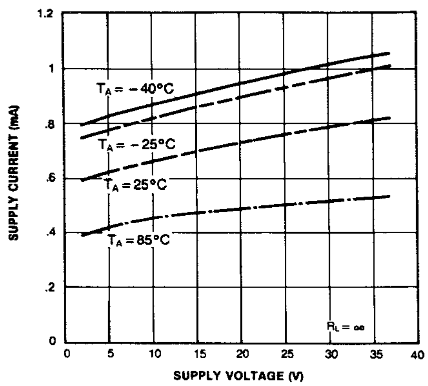


Fig. 2 INPUT CURRENT

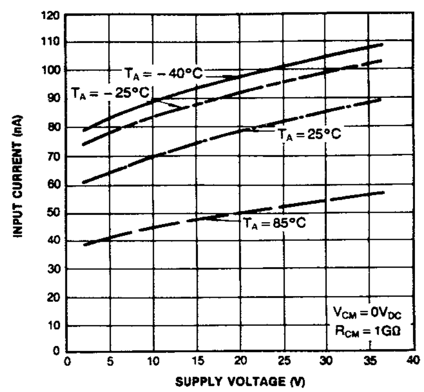


Fig. 3 OUTPUT SATURATION VOLTAGE

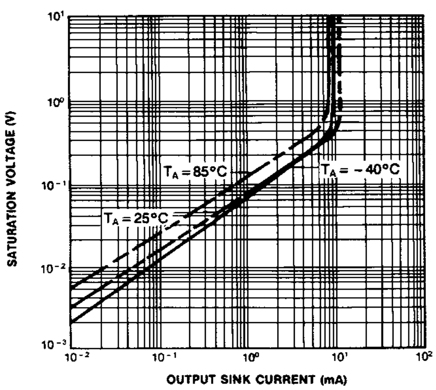


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

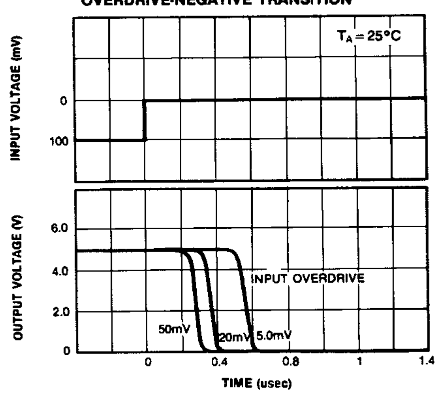
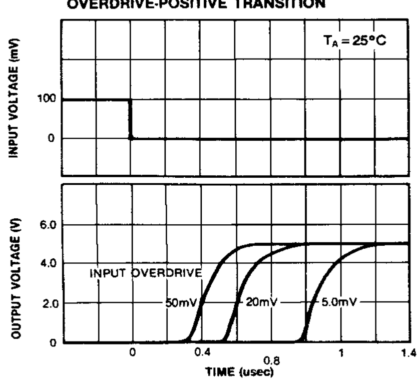


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



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LM311 (KA311) SINGLE COMPARATOR

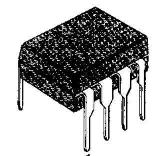
VOLTAGE COMPARATOR

The LM311 series is a monolithic, low input current voltage comparator.
The device is also designed to operate from dual or single supplies voltage

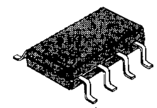
FEATURE

- Low input bias current : 250nA (Max)
- Low input offset current : 50nA (Max)
- Differential Input Voltage : ±30V.
- Power supply voltage : single 5.0V supply to ±15V.
- Offset voltage null capability.
- Strobe capability.

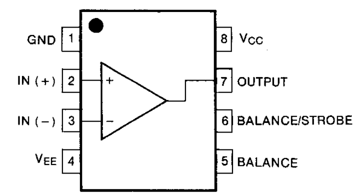
8 DIP



8 SOP



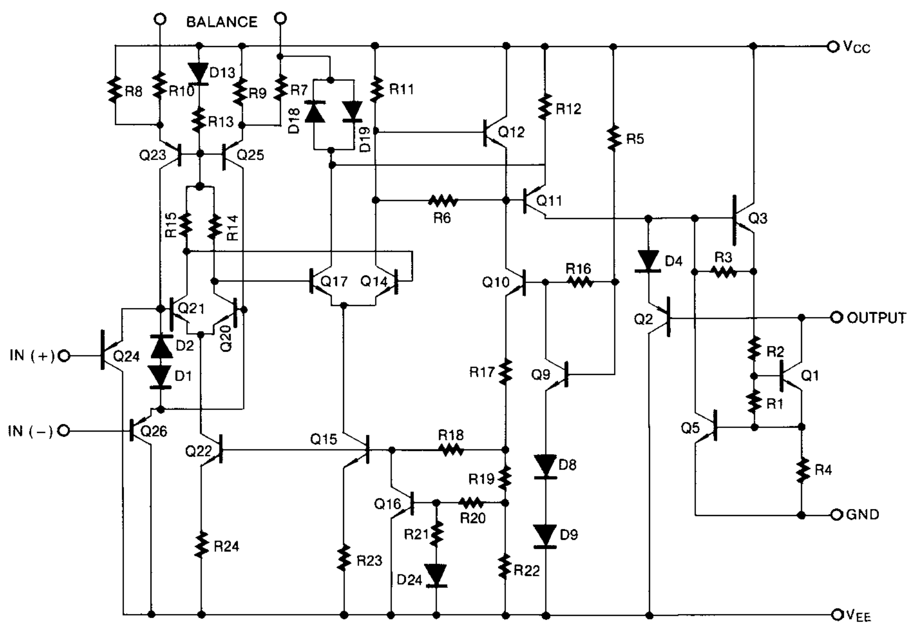
BLOCK DIAGRAM



ORDERING IN FORMATION

Device	Package	Operating Temperature
LM311N	8 DIP	0 ~ +70°C
LM311M	8 SOP	

SCHEMATIC DIAGRAM



Rev. B

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Total Supply Voltage	V_{CC}	36	V
Output to Negative Supply Voltage KA311	V_O - V_{EE}	40	V
Ground to Negative voltage	V_{EE}	-30	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration		10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	0 ~ +70	°C
Storage Temperature Range	T_{STG}	- 65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	R_S≤50KΩ		1.0	7.5	mV
		NOTE 1			10	
Input Offset Current	I_{IO}			6	50	nA
		NOTE 1			70	
Input Bias Current	I_{BIAS}			100	250	nA
		NOTE 1			300	
Voltage Gain	G_V		40	200		V/mV
Response Time	t_{RES}	NOTE 2		200		ns
Saturation Voltage	V_{SAT}	I_O =50mA, V_I≤-10mV		0.75	1.5	V
		V_{CC}≥4.5V, V_{EE} = 0V I_{SINK} =8mA, V_I≥-10mV, NOTE 1		0.23	0.4	
Strobe “NO” Current	$I_{STR(ON)}$			3		mA
Output Leakage Current	I_{SINK}	I_{STR} =3mA, V_I≥10mV $V_{O(P)}$ =35V, V_{EE} =V_{GND} =-5V		0.2	50	nA
Input Voltage Range	$V_{I(R)}$	NOTE 1	-14.5 to 13.0	-14.7 to 13.8		V
Positive Supply Current	I_{CC}			3.0	7.5	mA
Negative Supply Current	I_{EE}			-2.2	-5.0	mA
Strobe Current	I_{STR}			3		mA

NOTE 1. 0 ≤ T_A ≤ +70°C
2. The response time specified is for a 100mV input step with 5mV over drive.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 INPUT BIAS CURRENT

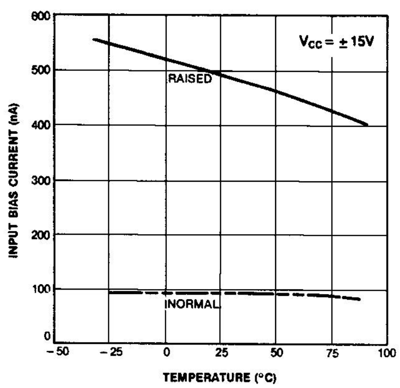


Fig. 2 INPUT OFFSET CURRENT

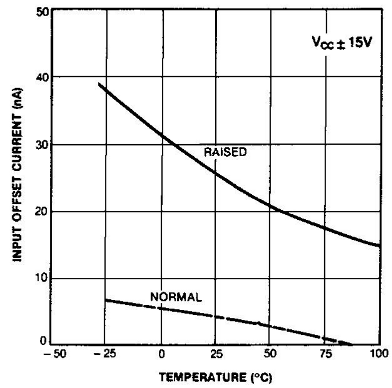


Fig. 3 OFFSET VOLTAGE VS INPUT RESISTANCE

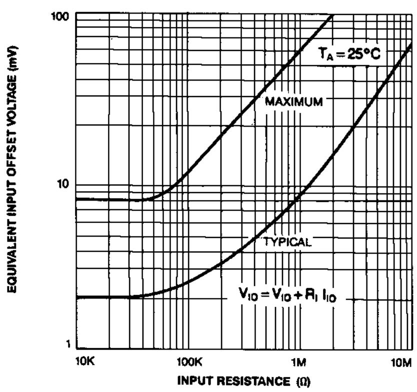


Fig. 4 INPUT BIAS CURRENT VS DIFFERENTIAL

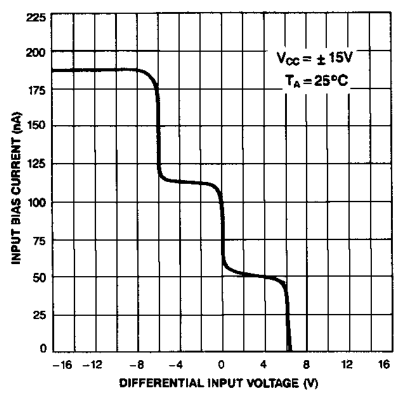


Fig. 5 COMMON MODE LIMITS VS TEMPERATURE

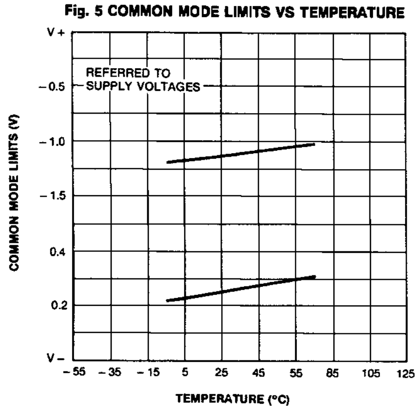


Fig. 6 OUTPUT VOLTAGE VS DIFFERENTIAL

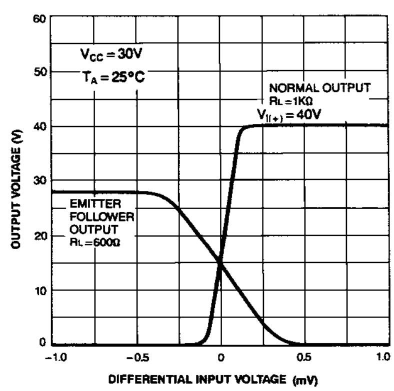


Fig. 7 SATURATION VOLTAGE VS CURRENT

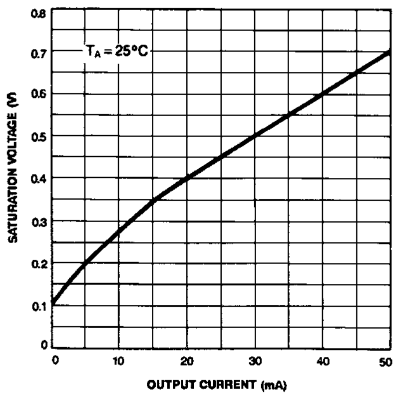


Fig. 8 SUPPLY CURRENT VS TEMPERATURE

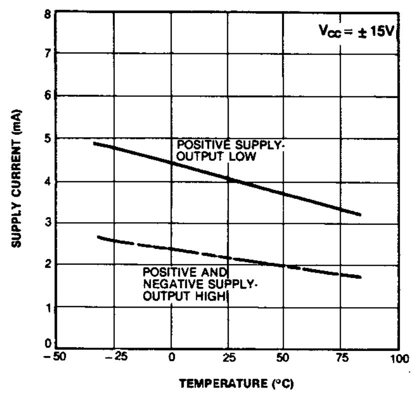


Fig. 9 LEAKAGE CURRENTS VS TEMPERATURE

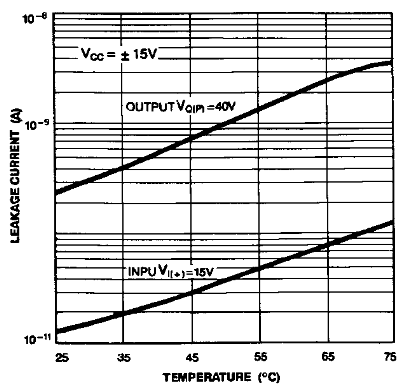


Fig. 10 SUPPLY CURRENT VS SUPPLY VOLTAGE

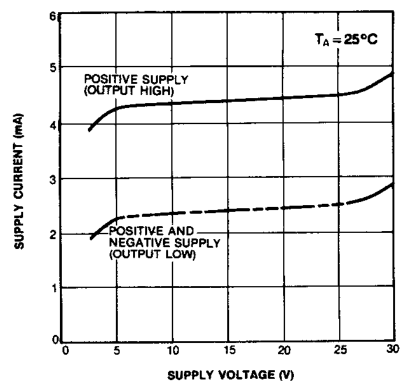


Fig. 11 OUTPUT SATURATION VOLTAGE

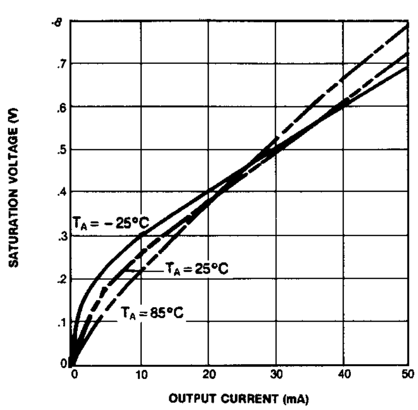
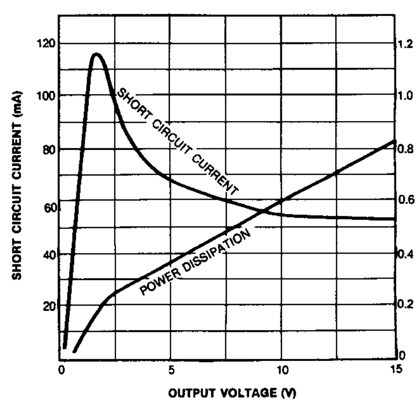


Fig. 12 OUTPUT LIMITING CHARACTERISTICS



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PRODUCT STATUS DEFINITIONS

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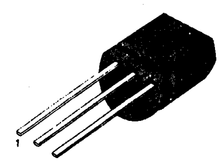
3-TERMINAL 0.1A POSITIVE ADJUSTABLE REGULATOR

The LM317L is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 100mA over an output voltage range of 1 .2V to 37V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage.

TO-92



1:Adj 2:Output 3:Input

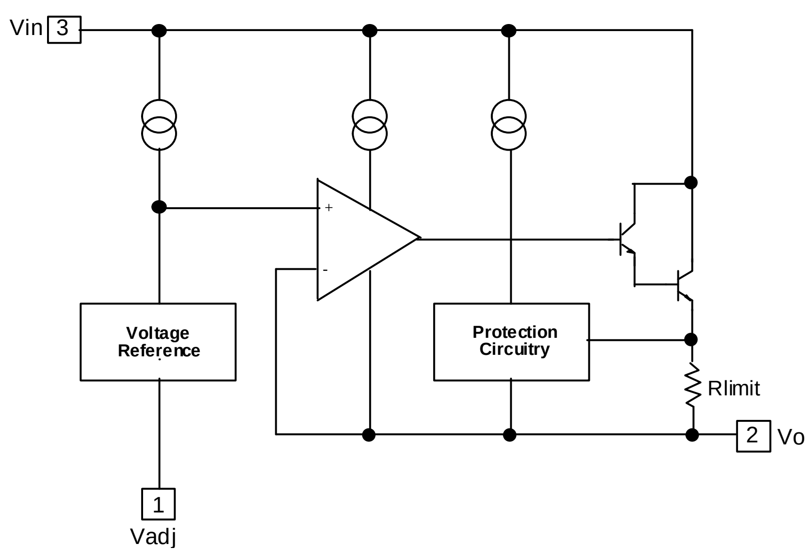
FEATURES

- Output current in excess of 100mA
- Output adjustable between 1.2V and 37V
- Internal thermal-overload protection
- Internal short-circuit current-limiting
- Output transistor safe-area compensation
- Floating operation for high-voltage applications

ORDERING INFORMATION

Device	Package	Operating Temperature
LM317LZ	TO-92	0 ~ 125°C

BLOCK DIAGRAM



ABLOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	V_I - V_O	40	V
Power Dissipation	P_D	Internally limited	W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~+125	°C

ELECTRICAL CHARACTERISTICS

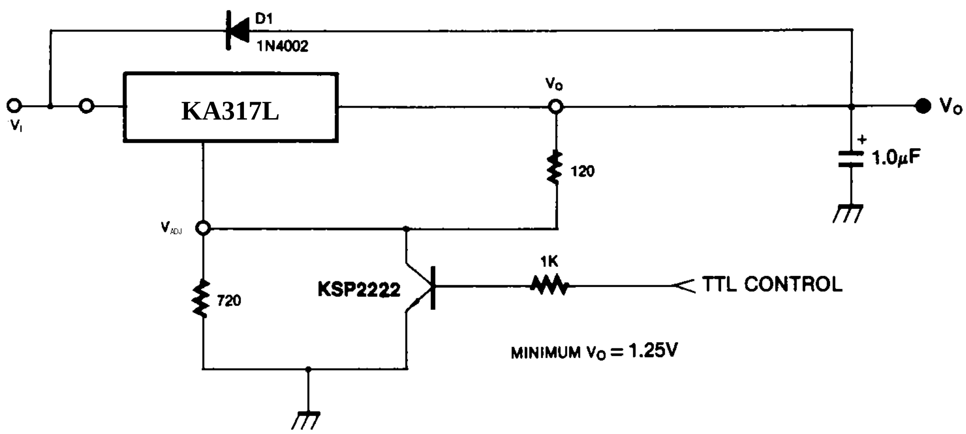
(V_I - V_O = 5V, I_O = 40mA, 0°C ≤ T_J ≤ +125°C, P_{DMAX} = 625mW, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
*Line Regulation	ΔV_O	T_A = +25°C 3V ≤ V_I ≤ V_O ≤ 40V		0.01	0.04	%/V
		3V ≤ V_I ≤ V_O ≤ 40V		0.02	0.07	
*Load Regulation	ΔV_O	T_A = +25°C 10mA ≤ I_O ≤100mA V_O ≤ 5V V_O ≥5V		5 0.1	25 0.5	mV %/ V_O
		10mA ≤ I_O ≤ 100mA V_O ≤ 5V V_O ≥ 5V		20 0.3	70 1.5	mV %/ V_O
Adjustment Pin Current	I_{ADJ}			50	100	μA
Adjustment Pin Current Change	ΔI_{ADJ}	3V ≤ V_I - V_O ≤ 40V 10mA ≤ I_O ≤ 100mA P_D < P_{DMAX}		0.2	5	μA
Reference Voltage	V_{REF}	3V < V_I - V_O <40V 10mA ≤ I_O ≤100mA P_D ≤ P_{DMAX}	1.20	1.25	1.30	V
Temperature Stability	ST_T			0.7		%
Minimum Load Current to Maintain Regulation	$I_{L(MIN)}$	V_I - V_O = 40V		3.5	10	mA
		V_I - V_O = 5V P_D < P_{DMAX}	100	200		
		V_I - V_O = 40V P_D < P_{DMAX}, T_A = +25°C	25	50		
RMS Noise, % of V_{OUT}	e_N	T_A =+ 25°C 10Hz < f <10KHz		0.003		%/ V_O
Ripple Rejection	RR	V_O = 10V, f = 120Hz without C_{ADJ} C_{ADJ} = 10μF	66	65 80		dB
Long-Term Stability	ST	T_J = +125 °C, 1000 Hours		0.3		%

* Load and Line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL APPLICATIONS

Fig. 1 5V Electronic Shutdown Regulator



D1 protects the device during an input short circuit.

Fig. 2 Slow Turn-On Regulator

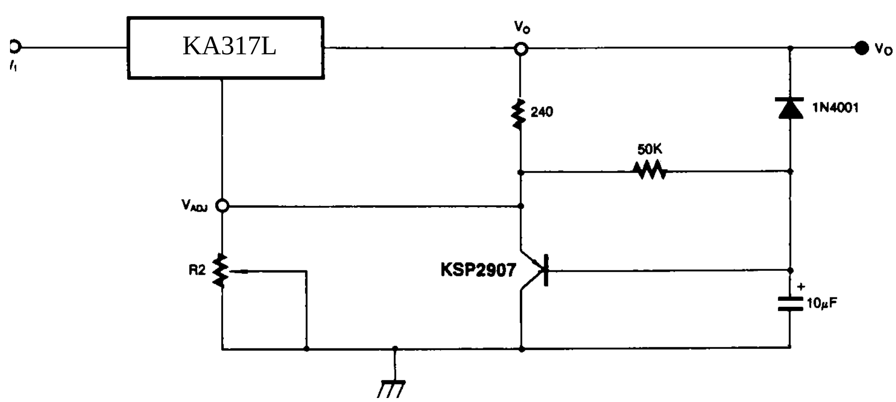
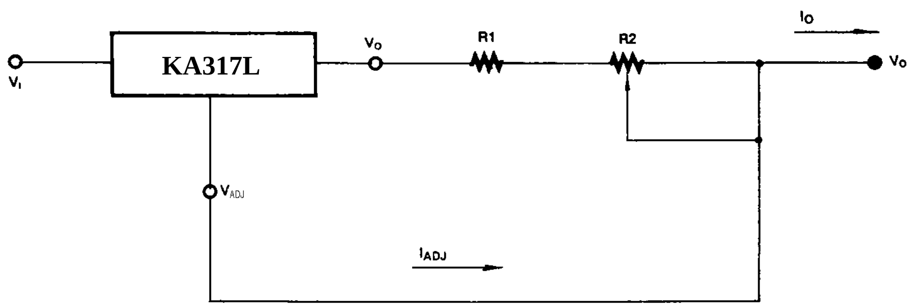


Fig. 3 Current Regulator



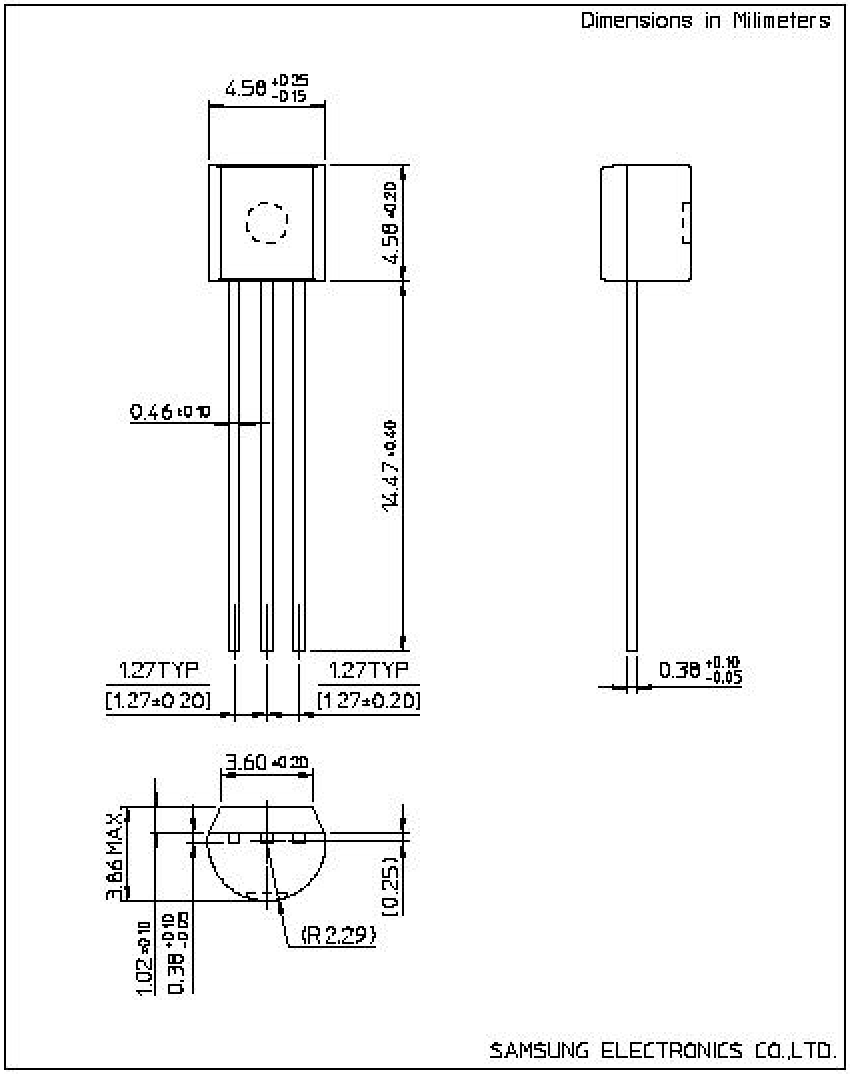
$$I_{OMAX} = \left(\frac{V_{REF}}{R1}\right) + I_{ADJ} \cong \frac{1.25V}{R1}$$

$$I_{OMIN} = \left(\frac{V_{REF}}{R1 + R2}\right) + I_{ADJ} \cong \frac{1.25V}{R1 + R2}$$

$$5mA < I_O < 500mA$$

PACKAGE DIMENSION

TO—92


Dimensions in Milimeters
4.50 +0.25 -0.15
4.58 ±0.20
0.46 ±0.10
14.47 ±0.40
1.27TYP
[1.27±0.20]
1.27TYP
[1.27±0.20]
0.38 +0.10 -0.05
3.60 ±0.20
3.86 MAX
1.02 ±0.10
0.38 +0.10 -0.05
(0.25)
(R2.29)
SAMSUNG ELECTRONICS CO.,LTD.

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FAST®	SuperSOT™-3
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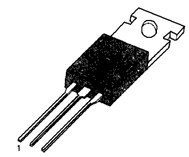
LM337 (KA337) ADJUSTABLE VOLTAGE REGULATOR (NEGATIVE)

3-TERMINAL 1.5A NEGATIVE ADJUSTABLE REGULATOR

The LM337 is a 3-terminal negative adjustable regulator. It supply in excess of 1.5A over an output voltage range of -1.2V to - 37V. This regulator requires only two external resistor to set the output voltage. Included on the chip are current limiting, thermal overload protection and safe area compensation.

TO-220



1:Adj 2:Intput 3:Output

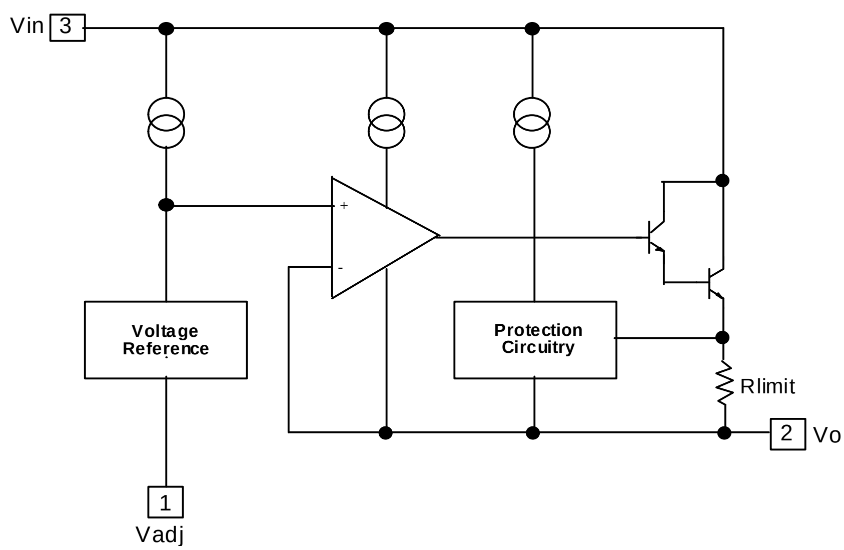
FEATURES

- Output current In excess of 1.5A
- Output voltage adjustable between -1.2V and - 37V
- Internal thermal-overload protection
- Internal short-circuit current limiting
- Output transistor safe-area compensation
- Floating operation for high-voltage applications
- Standard 3-pin TO-220 package

ORDERING INFORMATION

Device	Package	Operating Temperature
LM337T	TO-220	0 ~ + 125°C

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	V
Power Dissipation	P_D	Internally limited	W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~+125	°C

ELECTRICAL CHARACTERISTICS

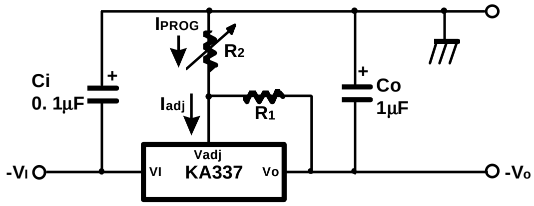
(V_I - V_O = 5V, I_O = 40mA, 0°C ≤ T_J ≤ +125°C, P_{DMAX} = 20W, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V_O	T_A = +25°C - 40V ≤V_O - V_I ≤ -3V		0.01	0.04	%/ V
		- 40V ≤ V_O - V_I ≤ -3V		0.02	0.07	
Load Regulation	V_O	T_A = +25°C 10mA ≤ I_O ≤0.5A		15	50	mV
		10mA ≤ I_O ≤1.5A		15	150	
Adjustable Pin Current	I_{ADJ}			50	100	µA
Adjustable Pin Current	ΔI_{ADJ}	T_A =+ 25°C 10mA ≤ I_O ≤1.5A - 40V ≤ V_O - V_I ≤ -3V		2	5	µA
Reference Voltage	V_{REF}	T_A =+ 25°C	-1.213	-1.250	-1.287	V
		- 40V ≤ V_O - V_I ≤ -3V 10mA ≤ I_O ≤ 1.5A	-1.200	-1.250	-1.300	
Temperature Stability	ST_T			0.6		%
Minimum Load Current to Maintain Rejection		- 40V ≤ V_O - V_I ≤ -3V		2.5	10	mA
		- 10V ≤ V_O - V_I ≤ -3V		1.5	6	
Output Noise	en	T_A =+25°C 10Hz ≤ f ≤10KHz		3 ×V_{OUT}		$V/10^6$
Ripple Rejection Ratio		V_O = -10V, f = 120Hz		60		dB
		C_{ADJ} = 10µF	66	77		
Long Term Stability	ST	T_J = 125°C ,1000Hours		0.3	1	%
Thermal Resistance Junction to Case	R_{EJC}			4		°C/ W

.
* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used

TYPICAL APPLICATIONS

Fig. 1 Programmable Regulator



* Ci is required if regulator is located more then 4 inches from power supply filter.
A 1.0µF solid tantalum or 10µF aluminum electrolytic is recommended.
Co is necessary for stability. A 1.0µF solid tantalum or 10µF aluminum electrolytic is recommended.

$$V_O = -1.25V\,(1 + R_2 / R_1)$$

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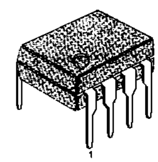
LF353 (LM353, KA353) DUAL OPERATIONAL AMPLIFIER (JFET)

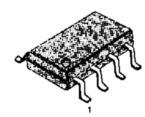
DUAL OPERATIONAL AMPLIFER

The LF353 is a JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides with bandwidth, low input bias currents and offset currents.

8 DIP



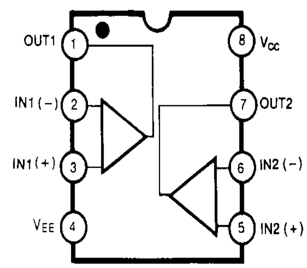
8 SOP



FEATURES

- Internally trimmed offset voltage: 10mV
- Low input bias current: 50pA
- Wide gain bandwidth: 4MHz
- High slew rate: 13V/μs
- High Input impedance: $10^{12}\Omega$

BLOCK DIAGRAM

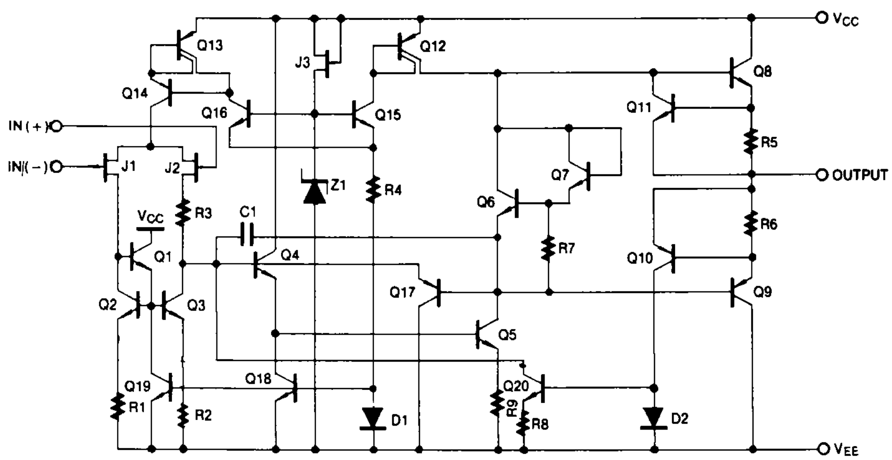


i

ORDERING IN FORMATION

Device	Package	Operating Temperature
LF353N	8 DIP	0 ~ + 70°C
LF353M	8 SOP	
LF353S	9 SIP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage Range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	0 ~ +70	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} =+15V, V_{EE}= -15V, T_A=25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	R_S=10KΩ			5.0	10	mV
			0 °C ≤T_A≤+70 °C				
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S=10KΩ	0 °C ≤T_A≤+70 °C		10		μV/ °C
Input Offset Current	I_{IO}				25	100	pA
			0 °C ≤T_A≤+70 °C			4	nA
Input Bias Current	I_{BIAS}				50	200	pA
			0 °C ≤T_A≤+70 °C			8	nA
Input Resistance	R_I				10^{12}		Ω
Large Signal Voltage Gain	G_V	$V_{O(P-P)}$ = ±0V		25	100		V/mV
		R_L = 2KΩ	0 °C ≤T_A≤+70 °C	15			
Output Voltage Swing	$V_{O(P.P)}$	R_L = 10KΩ		±12	±13.5		V
Input Voltage Range	$V_{I(R)}$			±11	±15/-12		V
Common Mode Rejection Ratio	CMRR	R_S≥10KΩ		70	100		dB
Power Supply Rejection Ratio	PSRR	R_S≥10KΩ		70	100		dB
Power Supply Current	I_{CC}				3.6	6.5	mA
Slew Rate	SR	G_V = 1			13		V/μs
Gain-Bandwidth Product	GBM				4		MHz
Channel Seperation	CS	f = 1Hz ~ 20Khz (Input referenced)		120	120		dB
Equivalent Input Noise Voltage	V_{NI}	R_S = 100Ω f = 1KHz		16	16		nV/√Hz
Equivalent Input Noise Current	I_{NI}	f = 1KHz		0.01	0.01		pA/√Hz

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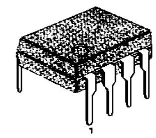
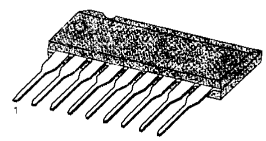
DUAL JFET INPUT OPERATIONAL

8 DIP



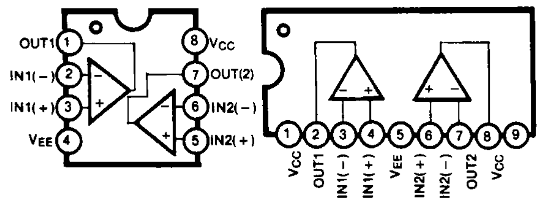
9 SIP



FEATURES

- Low supply current: 400pA MAX
- Low input bias Current: 50pA MAX
- Low input offset voltage: 1mV MAX
- High slew rate: 1V/μs
- High gain bandwidth: 1MHz

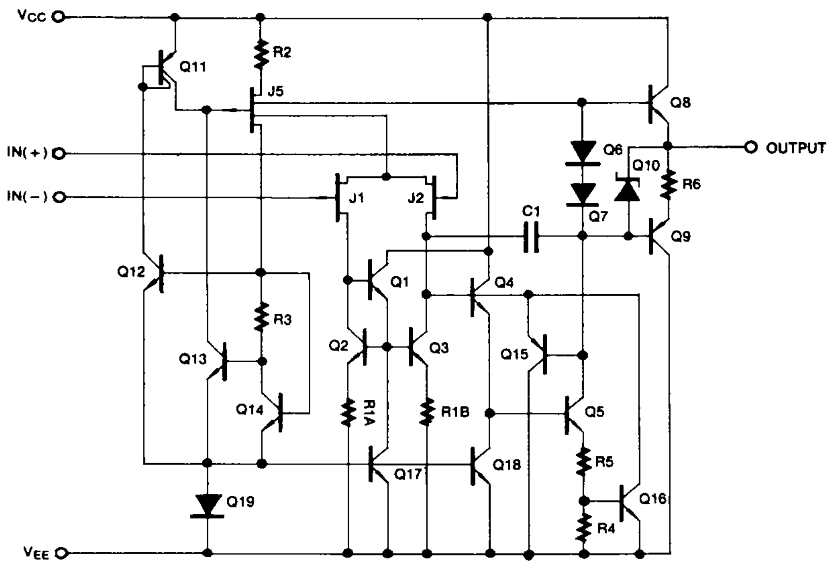
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM442N LM442AN	8 DIP	0 ~ +70°C
LM442S LM442AS	9 SIP	

SCHEMATIC DIAGRAM (One Section Only)



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage LM442	V_{CC}	±18	V
LM442A		±20	
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	670	mW
Operating Temperature Range LM442/A	T_{OPR}	0 ~ + 70	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(T_A=25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM442A			LM442			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S =10KΩ			0.5	1.0		1.0	5.0	mV
			Note 1						7.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 10KΩ			7	10		7		µV/ °C
Input Offset Current	I_{IO}				5	25		5	50	pA
			Note 1			15			15	
Large Signal Voltage Gain	I_{BIAS}				10	50		10	100	pA
			Note 1			30			30	
Large Signal Voltage Gain	G_V	R_L = 10KΩ		50	200		25	200		V/mV
		$V_{O(P.P)}$= ±0V	Note 1	25	200		15	200		
Output Voltage Swing	$V_{O(P-P)}$	R_S = 10KΩ		±17	±18		±12	±13		V
Input Voltage Range	$V_{I(R)}$			±16	+18 -17		±11	+15 -12		V
Common-Mode Rejection Ratio	CMRR	R_S≤10KΩ		80	100		70	95		dB
Power Supply Rejection Ratio	PSRR	R_S≤10KΩ		80	100		70	90		dB
Input Resistance	R_I				10^{12}		10^{12}			Ω
Supply Current	I_{CC}				300	400		400	500	µA
Slew Rate	SR			0.8	1		0.6	1		V/µS
Gain Bandwidth Product				0.8	1		0.6	1		MHz
Channel Separation	CS	f = 1Hz-20KHz (input referenced)			120			120		dB
Equivalent Input Noise Voltage	V_{NI}	R_S = 100Ω f = 1KHz			35			35		$nV/\sqrt{Hz}$
Equivalent Input Noise Current	I_{NI}	f = 1KHz			0.01			0.01		$pA/\sqrt{Hz}$

NOTE 1. LM442/A : 0≤T_A≤+70 °C

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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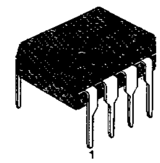
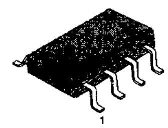
SINGLE TIMER

The LM555/I is a highly stable controller capable of producing accurate timing pulses. With monostable operation, the time delay is controlled by one external and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

8 DIP



8 SOP



FEATURES

- High Current Drive Capability (= 200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From µSec To Hours
- Turn Off Time Less Than 2µSec

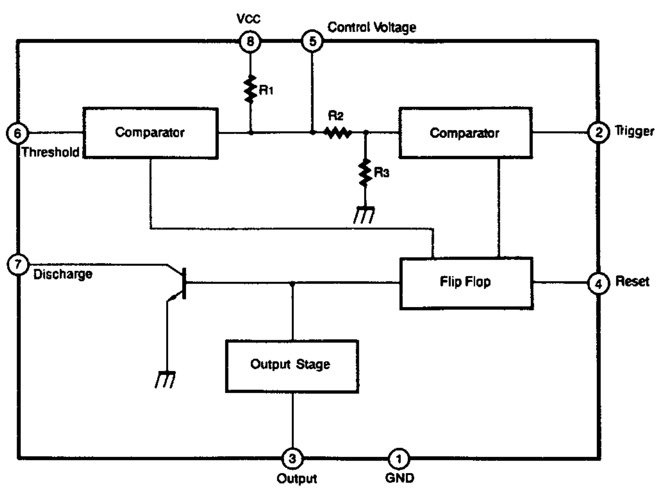
APPLICATIONS

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

ORDERING INFORMATION

Device	Package	Operating Temperature
LM555CN	8 DIP	0 ~ +70°C
LM555CM	8 SOP	
LM555CIN	8 DIP	-40 ~ +85°C
LM555CIM	8 SOP	

BLOCK DIAGRAM



Rev. B

FAIRCHILD SEMICONDUCTOR ™

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10sec)	T_{LEAD}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range LM555C LM555CI	T_{OPR}	0 ~ + 70 - 40 ~ + 85	°C °C
Storage Temperature Range	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current *[1](low stable)	I_{CC}	V_{CC} = 5V, R_L = ∞		3	6	mA
		V_{CC} = 15V, R_L = ∞		7.5	15	mA
*Timing Error (Monostable) [2]Initial Accuracy Drift with Temperature Drift with Supply Voltage	ACCUR Δt/ΔT Δt/ΔV_{CC}	R_A = 1KΩ to 100KΩ C = 0.1µF		1.0 50 0.1	3.0 0.5	% ppm/°C %/V
*Timing Error (astable) [2]Intial Accuracy Drift with Temperature Drift with Supply Voltage	ACCUR Δt/ΔT Δt/ΔV_{CC}	R_A = 1KΩ to 100KΩ C = 0.1µF		2.25 150 0.3		% ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15 V		10.0		V
		V_{CC} = 5V		3.33		V
*[3]Threshold Current	I_{TH}			0.1	0.25	µA
Trigger Voltage	V_{TR}	V_{CC} = 5V	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_{TR} = 0V		0.01	2.0	µA
Reset Voltage	V_{RST}		0.4	0.7	1.0	V
Reset Current	I_{RST}			0.1	0.4	mA

ELECTRICAL CHARACTERISTICS

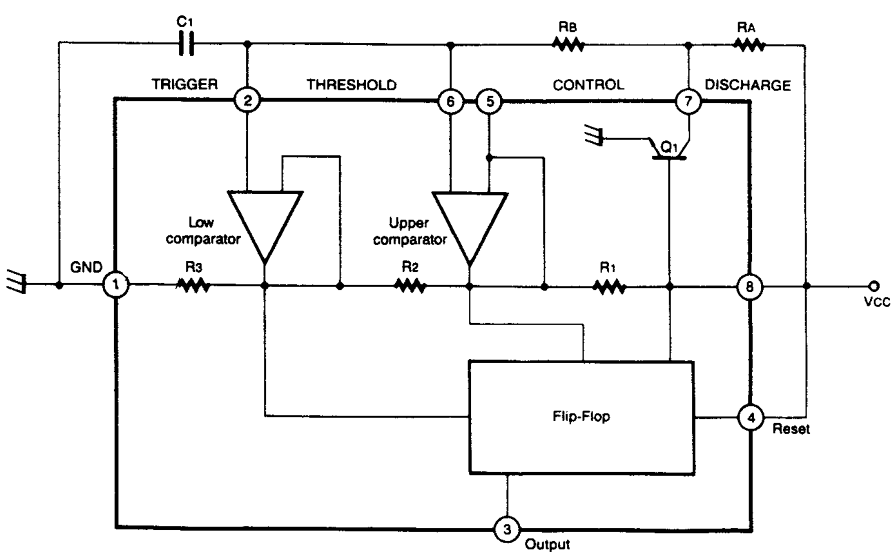
(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Output Voltage	V_{OL}	V_{CC} = 15V I_{SINK} = 10mA I_{SINK} = 50mA		0.06 0.3	0.25 0.75	V V
		V_{CC} = 5V I_{SINK} = 5mA		0.05	0.35	V
High Output Voltage	V_{OH}	V_{CC} = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA	12.75	12.5 13.3		V V
		V_{CC} = 5V I_{SOURCE} = 100mA	2.75	3.3		V
Rise Time of Output	t_R			100		ns
Fall Time of Output	t_F			100		ns
Discharge Leakage Current	I_{LKG}			20	100	nA

Notes:

1. Supply current when output is high is typically 1mA less at V_{CC} = 5V
2. Tested at V_{CC} = 5.0V and V_{CC} = 15V
3. This will determine maximum value of R_A + R_B for 15V operation, the max. total R = 20MΩ, and for 5V operation the max. total R = 6.7MΩ

APPLICATION CIRCUIT



APPLICATION NOTE

The application circuit shows astable mode.
Pin 6 (threshold) is tied to Pin 2 (trigger) and Pin 4 (reset) is tied to V_{CC} (Pin 8).
The external capacitor C_1 of Pin 6 and Pin 2 charges through R_A, R_B and discharges through R_B only.
In the internal circuit of the LM555 one input of the upper comparator is the 2/3 V_{CC} (*$R_1 = R_2 = R_3$, another input if it If it is connected Pin 6.
As soon as charging C_1 is higher than 2/3 Vcc, discharge transistor Q_1 turns on and C_1 discharges to collector of transistor Q_1.
Therefore, the flip-flop circuit is reset and output is low.
One input of lower comparator is the 1/3 V_{CC}, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B.
Therefore, the flip-flop circuit is set and output is high.
So to say, when C_1 charges through R_A and R_1 output is high and when C_1 discharges through R_B output is low.
The charge time (output is high) T_1 is 0.693 (R_A+R_B) C_1 and the discharge time (output is low) T_2 is 0.693 $(R_B C_1)$.

$$\left(l_n \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}} 0.693\right)$$

Thus the total period time T is given by
$T=T_1 + T_2 = 0.693\ (R_A + 2R_B)\ C_1$.
Then the frequency of astable mode is given by

$$f = \ = \frac{1}{T} \quad \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

$$D.C = \ = \frac{T_2}{T} \quad \frac{R_B}{R_A + 2R_B}$$

If you make use of the LM556 you can make two astable modes.

Astable Operation

The LM555 can free run as a mulitivibrator by triggering itself; refer to Fig.2. The output can swing from V_{DD} to GND and have 50 duty cycle square wave. Less than 1% frequency deviation can be observed, over a voltage range of 2 to 5V. f-1/1.4RC

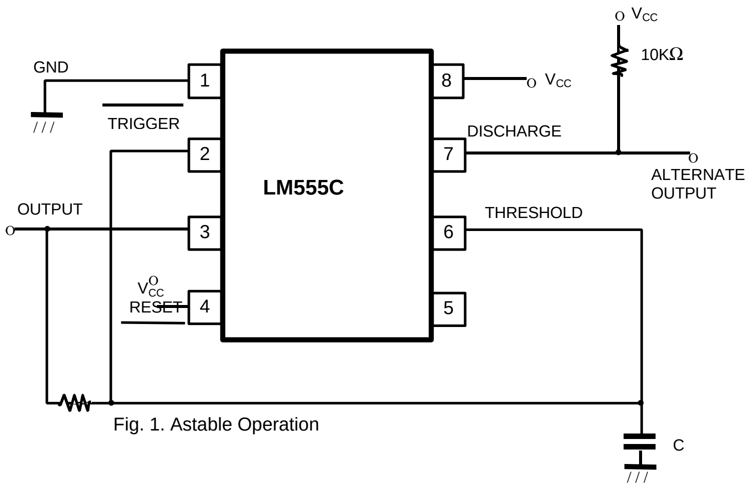


Fig. 1. Astable Operation

Monostable Operation

The LM555 can be used as a one-short, i.e. monostable multivibrator. Initially, because the inside discharge transistor is on state, external timing capacitor is held to GND potential. Upon application of a negative TRIGGER pulse pin 2, the intern discharge transistor is off state and the voltage across the capacitor increases with time constant T = R_AC and OUTPUT goes to high state. When the voltage across the capacitor equals 2/3V_{CC} the inner comparator is reset by THRESHOLD input and the discharge transistor goes to on state, which in turn discharges the capacitor rapidly and drives the OUTPUT to its low state.

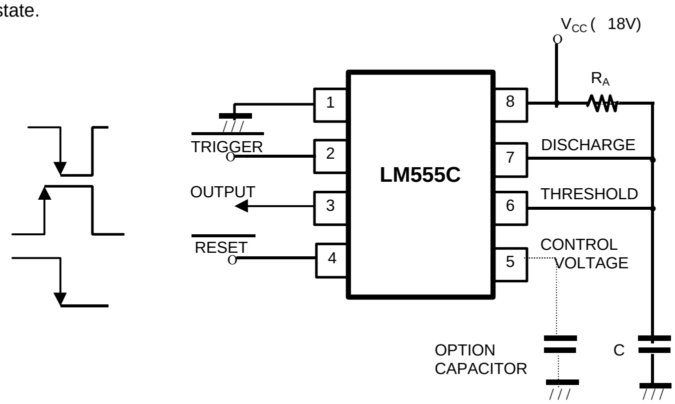


Fig. 2. Monostable Operation

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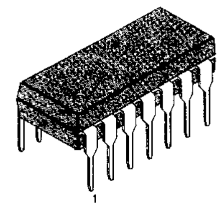
DUAL TIMER

The LM556/I series dual monolithic timing circuits are a highly stable controller capable of producing accurate time delays or oscillation. The LM556 is a dual LM555. Timing is provided an external resistor and capacitor for each timing function.
The two timers operate independently of each other, sharing only V_{CC} and ground.
The circuits may be triggered and reset on falling wave forms. The output structures may sink or source 200mA.

14 DIP



FEATURES

- Replaces Two LM555C Timers
- Operates in Both Astable and Monostable Modes
- High Output Current
- TTL Compatible
- Timing From Microsecond to Hours
- Adjustable Duty Cycle
- Temperature Stability Of 0.005% Per °C

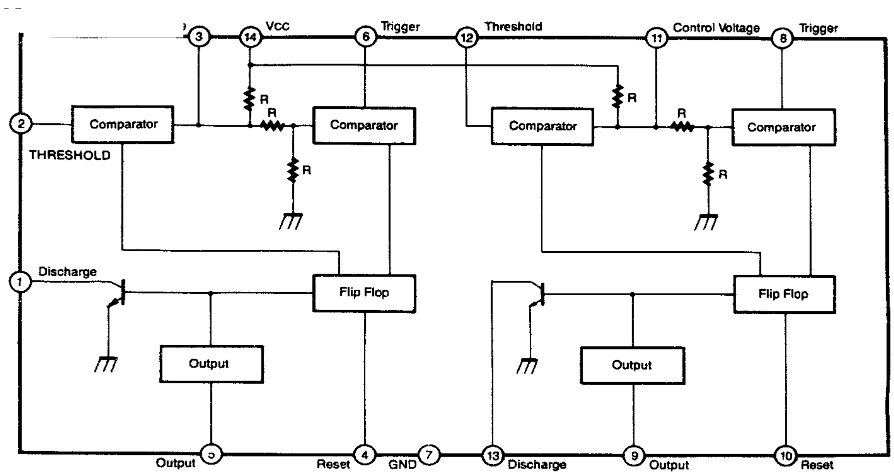
ORDERING INFORMATION

Device	Package	Operating Temperature
LM556CN	14 DIP	0 ~ + 70°C
LM556ICN	14 DIP	-40 ~ + 85°C

APPLICATIONS

- Precision Timing
- Pulse Shaping
- Pulse Width Modulation
- Frequency Division
- Traffic Light Control
- Sequential Timing
- Pulse Generator
- Time Delay Generator
- Touch Tone Encoder
- Tone Burst Generator

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10sec)	T_{LEAD}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range LM556 LM556I	T_{OPR}	0 ~ + 70 - 40 ~ + 85	°C °C
Storage Temperature Range	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
*1 Supply Current (two timers) (low state)	I_{CC}	V_{CC} = 5V, R_L = ∞		5	12	mA
		V_{CC} = 15V, R_L = ∞		16	30	mA
*2 Timing Error (monostable)		R_A = 2kΩ to 100kΩ				
Initial Accuracy	ACCUR	C = 0.1µF		0.75		%
Drift with Temperature	Δt/ΔT	T = 1.1RC		50		ppm/°C
Drift with Supply Voltage	$\Delta t/\Delta V_{CC}$			0.1		%/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V	8.8	10.0	11.2	V
		V_{CC} = 5V	2.4	3.33	4.2	V
*3 Threshold Voltage	I_{TH}			30	250	nA
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5.0	5.6	V
		V_{CC} = 5V	1.1	1.6	2.2	V
Trigger Current	I_{TR}	V_{TH} = 0V		0.01	2.0	µA
*5 Reset Voltage	V_{RST}		0.4	0.6	1.0	V
Reset Current	I_{RST}			0.03	0.6	mA
Low Output Voltage	V_{OL}	V_{CC} = 15V				
		I_{SINK} = 10mA		0.1	0.25	V
		I_{SINK} = 50mA		0.4	0.75	V
		I_{SINK} = 100mA		2.0	3.2	V
		I_{SINK} = 200mA		2.5		V
		V_{CC} = 5V				
		I_{SINK} = 8mA		0.25	0.35	V
		I_{SINK} = 5mA		0.15	0.25	V

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
High Output Voltage	V_{OH}	V_{CC} = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA	 12.75	 12.5 13.3		 V V
		V_{CC} = 5V I_{SOURCE} = 100mA	 2.75	 3.3		 V
Rise Time of Output	t_R			100	300	ns
Fall Time of Output	t_F			100	300	ns
Discharge Leakage Current	I_{LKG}			10	100	nA
*4 Matching Characteristics Initial Accuracy Drift with Temperature Drfit with Supply Voltage	 ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$			 1.0 10 0.2	 2.0 0.5	 % ppm/°C %/V
*2 Timing Error (astable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	 ACCUR $\Delta t/\Delta T$	R_A,R_B = 1kΩ to 100kΩ C = 0.1μF V_{CC} = 15V		 2.25 150 0.3		 % ppm/°C %/V

Notes:

*1. Supply current when output is high is typically 1.0mA less at V_{CC} = 5V

*2. Tested at V_{CC} = 5V and V_{CC} = 15V

*3. This will determine the maximum value of R_A + R_B for 15V operation.
The maximum total R = 20MΩ, and for 5V operation the maximum total R = 6.6MΩ.

*4. Matching characteristics refer to the difference between performance characteristics of each timer section in the monostable mode.

*5. As reset voltage lowers, timing is inhibited and then the output goes low.

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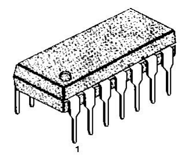
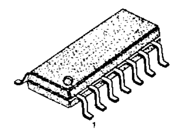
HIGH SPEED VOLTAGE COMPARATOR

The LM710/I is a high speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance.
The output of the comparator is compatible with all integrated logic forms.
The LM710/I is useful as pulse height discriminators. a variable threshold Schmitt trigger, voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver.

14 DIP



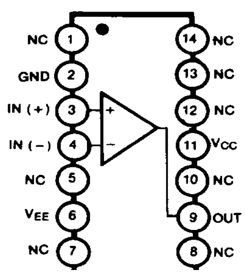
14SOP



FEATURES

- Low offset voltage: 5mV
- High gain: 1000 V/V
- High speed: 40ns Typ

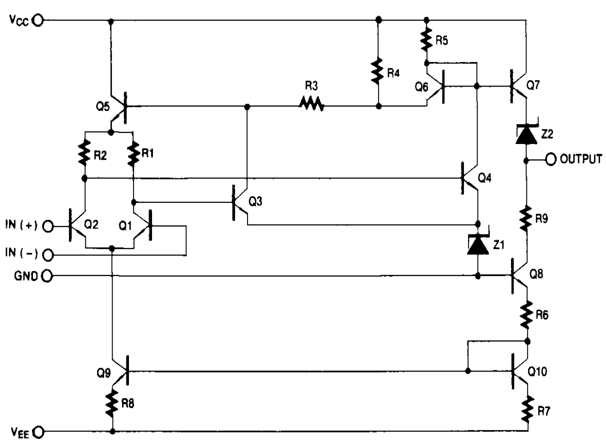
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM710N	14 DIP	0 ~ 70°C
LM710M	14 SOP	
LM710IN	14 DIP	-25 ~ 85°C
LM710IM	14 SOP	

SCHEMATIC DIAGRM



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+14	V
Negative Supply Voltage	V_{EE}	-7	V
Peak Output Current	I_{PK}	10	mA
Output Short Circuit Duration		10	Sec
Differential Input Voltage	$V_{I(DIFF)}$	5	V
Input Voltage	V_I	± 7	V
Power Dissipation	P_D	500	mW
Operating Temperature Range LM710	T_{STG}	0 ~ + 70	°C
LM710I		- 25 ~ + 85	°C
Storage Temperature Range	T_{STG}	- 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12V, V_{EE}= -6V, T = 25°C, unless otherwise specified)

Characteristics	Symbol	Test Conditions		LM710I			LM710			UNIT
				Min	Typ	Max	Min	Typ	Max	
Input Offset voltage	V_{IO}	R_S≤200Ω,	Note1		0.6	2.0		1.6	5.0	mV
			Note 2			3.0			6.5	
Input Offset Current (Note 1)	I_{IO}	NOTE 1			0.75	3.0		1.8	5.0	nA
			Note 2		1.8	7.0			7.5	
Input Bias Current	I_{BIAS}				5.0	20		7.0	25	nA
			Note 2		27	45		25	40	
Large Signal Voltage Gain	G_v			1250	1800		1000	1700		V/V
			Note 2							
Input Voltage Range	$V_{I(R)}$	V_{CC} = -7V		± 5.0			± 5.0			V
Common Mode Rejection Ratio	CMRR	R_S≤200Ω, NOTE 2		80	95		70	94		dB
Differential Input Voltage Range	$V_{ID(R)}$			± 5.0			± 5.0			V
Positive Output Level	$V_{O(H)}$	0 ≤ I_O ≤5mA, V_I ≥ 5mV		2.5	2.9	4.0	2.5	2.9	4.0	V
Negative Output Level	$V_{O(L)}$	V_I≥5mV		-1.0	-0.5	0	-1.0	-0.5	0	V
Output Sink Current	I_{SINK}	$V_{O(P)}$ =0V, V_I ≥ 5mV		2.0	2.2		1.6	2.2		mA
Positive Supply Current	I_{CC}	$V_{O(P)}$ ≤ 0V			4.7	9.0		4.7	9.0	mA
Negative Supply Current	I_{EE}	$V_{O(P)}$ = 0V, V_I = 5mV			4.0	7.0		4.0	7.0	mA
Power Consumption	P_D	$V_{O(P)}$ = 0V, V_I =10mV			80	150			150	mV
Response Time	t_{RES}	(Note 3)			40			40		ns

Note 1. The input offset voltage and input offset current are specified for a logic threshold voltage as follows:
For 710I, 1.65V at -25°C, 1.4V at +25°C, 1.15V at +85°C. For 710, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.
Note 2. LM710: 0≤ TA≤ +70°C
LM710I:-25≤ TA≤ +85°C
Note 3. The response time specified is a 100mV input step with 5mV overdrive (LM710).

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

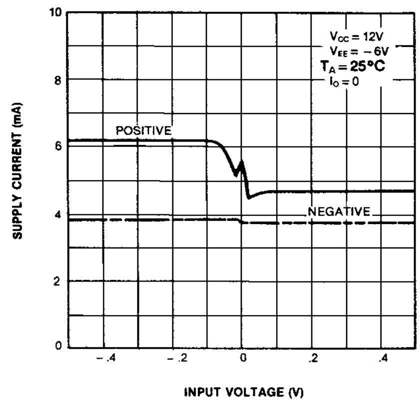


Fig. 2 VOLTAGE GAIN

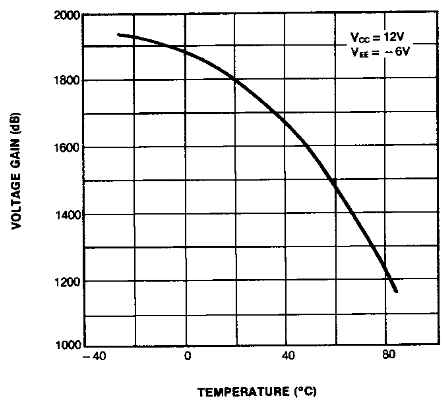


Fig. 3 INPUT OFFSET CURRENT

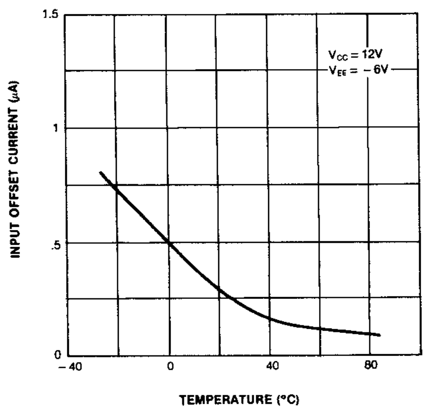


Fig. 4 INPUT BIAS CURRENT

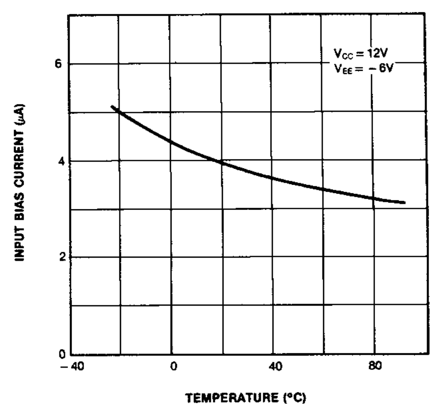


Fig. 5 OUTPUT VOLTAGE LEVEL

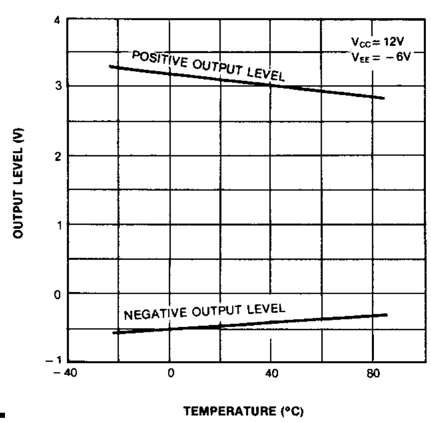
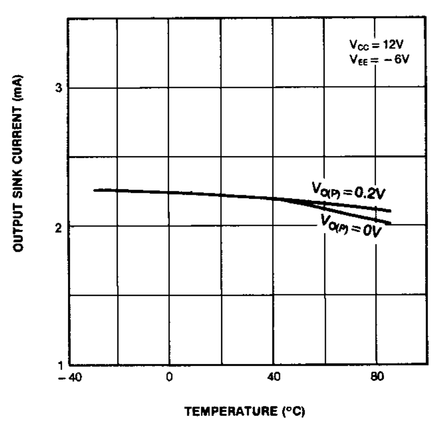


Fig. 6 OUTPUT SINK CURRENT



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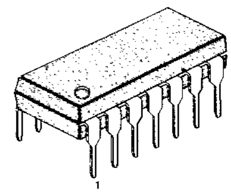
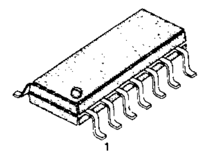
DUAL HIGH-SPEED DIFFERENT COMPARATOR

The LM711/I consists of two voltage comparators with the separate differential inputs, a common output and provision for strobing each side independently. The device features high accuracy, fast response, low offset voltage, a large input voltage range, low power consumption and compatibility with practically all integrated logic forrns.
The LM711/I can be used as a sense amplifier for memories, and a dual comparator with OR'ed outputs is required, such as a double-ended limit detector.

14 DIP



14 SOP



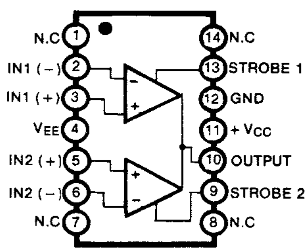
FEATURES

- Fast response time: 40ns (Typ)
- Output compatible with most TTL circuits
- Independent strobing of each comparator
- Low offset voltage

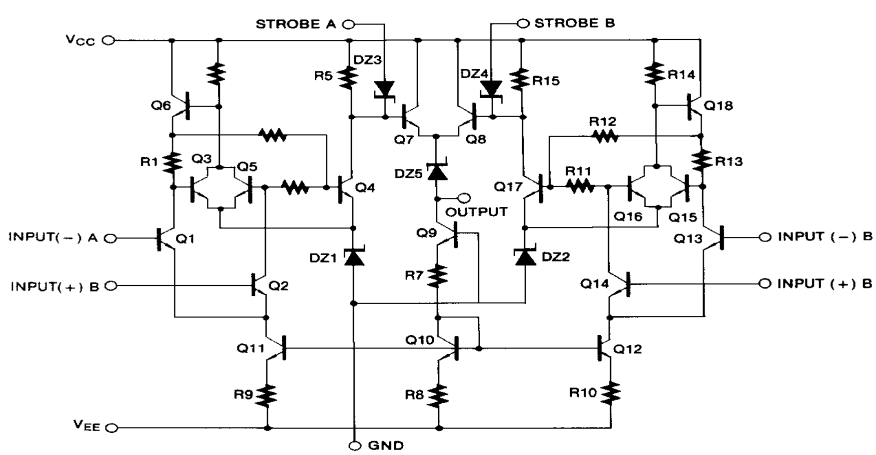
ORDERING INFORMATION

Device	Package	Operating Temperature
LM711N	14 DIP	0 ~ + 70°C
LM711M	14 SOP	
LM711IN	14 DIP	-25 ~ + 85°C
LM711IM	14 SOP	

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+14	V
Negative Supply Voltage	V_{EE}	-7	V
Differential Input Voltage	$V_{I(DIFF)}$	5	V
Input Voltage	V_I	±7	V
Storbe Voltage	V_{STR}	0 ~ 6	V
Peak Output Current	$I_{O(P)}$	50	mA
Continuous Total Power Dissipation	P_D	500	mW
Operating Temperature Range LM711		0 ~ + 70	
LM711I	T_{OPR}	-65 ~ + 150	°C
Storage Temperature Range	T_{STG}	-25 ~ + 85	°C

ELECTRICAL CHARACTERISTICS

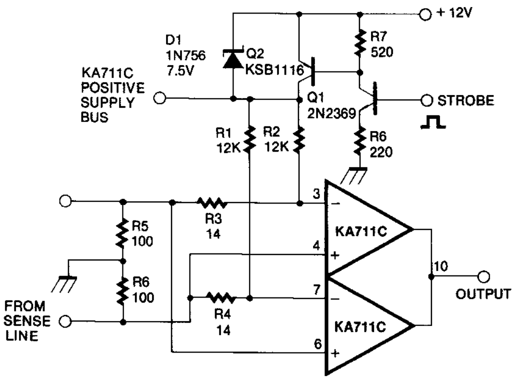
(V_{CC} = +12V, V_{EE} = -6V, T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM711I			LM711			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤200Ω, V_{CH} =0V			1.0	3.5		1.0	5.0	mV
		$V_{O(P)}$=1.4V	Note 2			4.5			6.0	
Input Offset Current (Note 1)	I_{IO}	$V_{O(P)}$=1.4V			0.5	10.0		0.5	15	μA
			Note 2			20			25	
Input Bias Current	I_{BIAS}				25	75		25	100	μA
			Note 2			150			150	
Large Signal Voltage Gain	G_V			750	1500		700	1500		V/V
			Note 2	500			500			
Input Voltage Range	$V_{I(R)}$	V_{EE} = -7.0V		±5.0			±5.0			V
Differential Input Voltage Range	$V_{ID(R)}$			±5.0			±5.0			V
Output Resistance	R_O				200			200		Ω
Output Voltage (High)	$V_{O(H)}$	V_I≥10mV			4.5	5.0		4.5	5.0	V
Output Voltage (Low)	$V_{O(L)}$	V_I≤10mV		-1.0		0	-1.0	-0.5	0	V
Loaded Output High Level	V_{OH}	V_I≥5mV, I_O = 5mA		2.5	3.5		2.5	3.5		mA
Strobed Output Level	V_{STR}	V_{STROBE}≥3V		-1.0		0	-1.0		0	V
Output Sink Current	I_{SINK}	V_I≥10mV, $V_{O(P)}$ ≥0V		0.5	0.8		0.5	0.8		mA
Positive Supply Current	I_{CC}	$V_{O(P)}$ =0V, V_I = 10mV			8.6			8.6		mA
Negative Supply Current	I_{EE}	$V_{O(P)}$ =0V, V_I =5mV			3.9			3.9		mA
Strobe Current	I_{STR}	V_{STROBE} = 100mV			1.2	2.5		1.2	2.5	mA
Power Consumption	P_D	$V_{O(P)}$ =0V, V_I≥10mV			130	200		130	230	mW
Response Time	t_{RES}	(NOTE 1)			40			40		ns
Strobe Release Time	T_{RE}				12			12		ns

Note: 1. The response time specified is for a 100mV input step with 10mV overdrive
2. LM711: 0≤T_A≤ +70°C
LM711I: -25≤T_A≤ +85°C
3. The input offset voltage and input offset current are specified for a logic threshold voltage of 711I, 1.65V at -25°C, 1.4V at +25°C, 1.15V at +85°C, for 711, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.

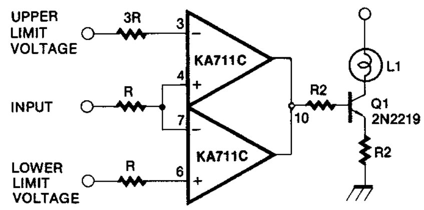
TYPICAL APPLICATIONS

Fig. 1 Sense Amplifier With Supply Strobing for Reduced Power Consumption*



* Standby dissipation is about 40mW

Fig. 2 Double-Ended Limit Detactor With Lamp Driver



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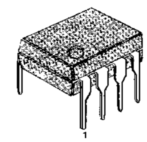
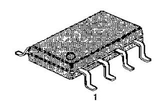
SINGLE OPERATIONAL AMPLIFIERS

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications.
The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.

8 DIP



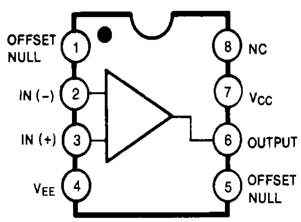
8 SOP



FEATURES

- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset

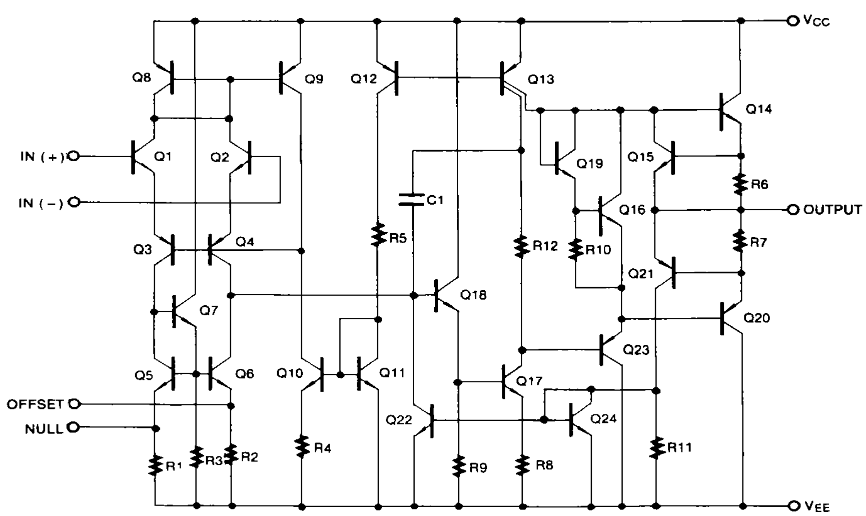
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM741N LM741EN	8 DIP	0 ~ + 70°C
LM741M LM741EM	8 SOP	
LM741IN LM741EIN	8 DIP	-40 ~ +85 °C
LM741IM LM741EIM	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A=25 °C)

Characteristic	Symbol	LM741	LM741E	LM741I	Unit
Supply Voltage	V_{CC}	±18	±22	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	30	30	V
Input Voltage	V_I	±15	±15	±15	V
Output Short Circuit Duration		Indefinite	Indefinite	Indefinite	
Power Dissipation	P_D	500	500	500	mW
Operating Temperature Range	T_{OPR}	0 ~ + 70	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	-65 ~ + 150	-65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$						2.0	6.0	mV
		$R_S \leq 50\Omega$			0.8	3.0				
Input Offset Voltage Adjustment Range	$V_{IO(R)}$	V_{CC} = ±20V		±10				±15		mV
Input Offset Current	I_{IO}				3.0	30		20	200	nA
Input Bias Current	I_{BIAS}				30	80		80	500	nA
Input Resistance	R_I	V_{CC} =±20V		1.0	6.0		0.3	2.0		MΩ
Input Voltage Range	$V_{I(R)}$			±12	±13		±12	±13		V
Large Signal Voltage Gain	G_V	$R_L \geq 2K\Omega$	V_{CC} =±20V, $V_{O(P.P)}$ =±15V	50						V/mV
			V_{CC} =±15V, $V_{O(P.P)}$ =±10V				20	200		
Output Short Circuit Current	I_{SC}			10	25	35		25		mA
Output Voltage Swing	$V_{O(P.P)}$	V_{CC} = ±20V	$R_L \geq 10K\Omega$	±16						V
			$R_L \geq 10K\Omega$	±15						
		V_{CC} = ±15V	$R_L \geq 10K\Omega$				±12	±14		
			$R_L \geq 10K\Omega$				±10	±13		
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$, V_{CM} = ±12V					70	90		dB
		$R_S \leq 50K\Omega$, V_{CM} = ±12V		80	95					
Power Supply Rejection Ratio	PSRR	V_{CC} = ±15V to V_{CC} = ±15V $R_S \leq 50\Omega$		86	96					dB
		V_{CC} = ±15V to V_{CC} = ±15V $R_S \leq 10K\Omega$					77	96		

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	LM741E			LM741/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Transient Response	Rise Time	t_R	Unity Gain		0.25	0.8		0.3		μs
	Overshoot	OS			6.0	20		10		%
Bandwidth		BW		0.43	1.5					MHz
Slew Rate		SR	Unity Gain	0.3	0.7			0.5		V/μs
Supply Current		I_{CC}	$R_L = \infty\Omega$					1.5	2.8	mA
Power Consumption		P_C	$V_{CC} = \pm 20V$		80	150				mW
			$V_{CC} = \pm 15V$					50	85	

ELECTRICAL CHARACTERISTICS

(-40 °C ≤T_A≤85 °C for the KA741I °C ≤T_A≤70 °C for the LM741 and LM741E. V_{CC} = ±15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \le 50\Omega$				4.0				mV
		$R_S \le 10K\Omega$							7.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				15					μV/ °C
Input Offset Current	I_{IO}					70			300	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$					0.5				nA/ °C
Input Bias Current	I_{BIAS}					0.21			0.8	μA
Input Resistance	R_I	$V_{CC} = \pm 20V$		0.5						MΩ
Input Voltage Range	$V_{I(R)}$			±12	±13		±12	±13		V
Output Voltage Swing	$V_{O(P.P)}$	$V_{CC} = \pm 20V$	$R_S \ge 10K\Omega$	±16						V
			$R_S \ge 2K\Omega$	±15						
		$V_{CC} = \pm 15V$	$R_S \ge 10K\Omega$				±12	±14		
			$R_S \ge 2K\Omega$				±10	±13		
Output Short Circuit Current	I_{SC}			10		40	10		40	mA
Common Mode Rejection Ratio	CMRR	$R_S \le 10K\Omega$, $V_{CM} = \pm 12V$					70	90		dB
		$R_S \le 50K\Omega$, $V_{CM} = \pm 12V$		80	95					
Power Supply Rejection Ratio	PSRR	$V_{CC} = \pm 20V$ to ±5V	$R_S \le 50\Omega$	86	96					dB
			$R_S \le 10K\Omega$				77	96		
Large Signal Voltage Gain	G_V	$R_S \ge 2K\Omega$	$V_{CC} = \pm 20V$, $V_{O(P-P)} = \pm 15V$	32						V/mV
			$V_{CC} = \pm 15V$, $V_{O(P.P)} = \pm 10V$				15			
			$V_{CC} = \pm 15V$, $V_{O(P-P)} = \pm 2V$	10						

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 7 OUTPUT RESISTANCE vs FREQUENCY

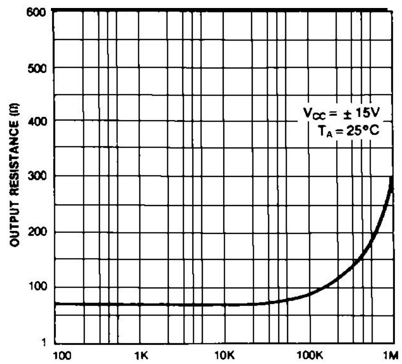


Fig. 8 INPUT RESISTANCE AND INPUT CAPACITANCE vs FREQUENCY

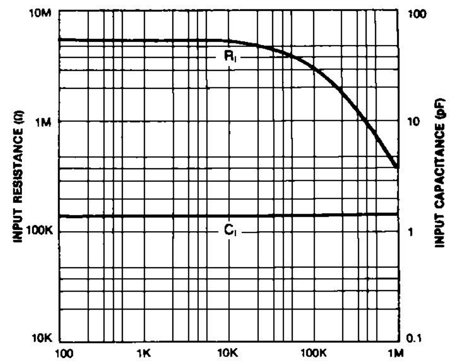


Fig. 9 INPUT BIAS CURRENT vs AMBIENT TEMPERATURE

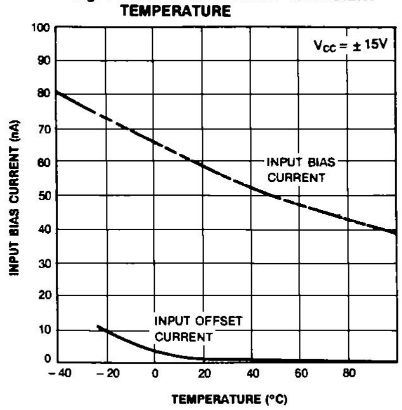


Fig. 10 POWER CONSUMPTION vs AMBIENT TEMPERATURE

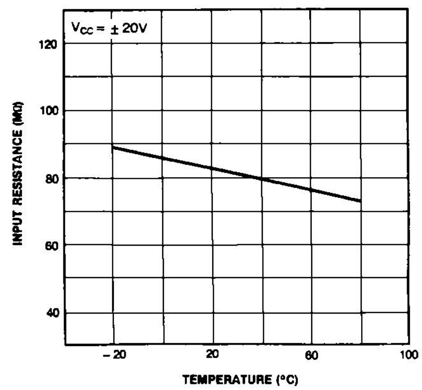


Fig. 11 INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE

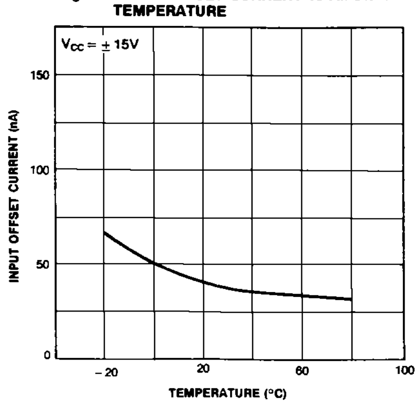


Fig. 12 INPUT RESISTANCE vs AMBIENT TEMPERATURE

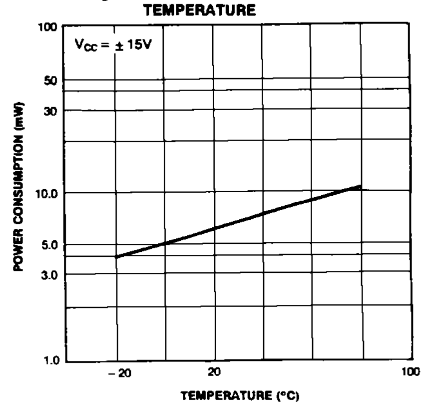


Fig. 13 NORMALIZED DC PARAMETERS vs AMBIENT TEMPERATURE

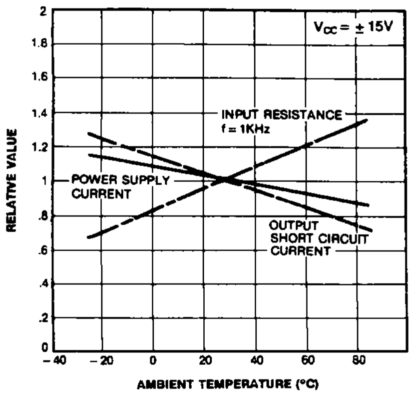


Fig. 14 FREQUENCY CHARACTERISTICS vs AMBIENT TEMPERATURE

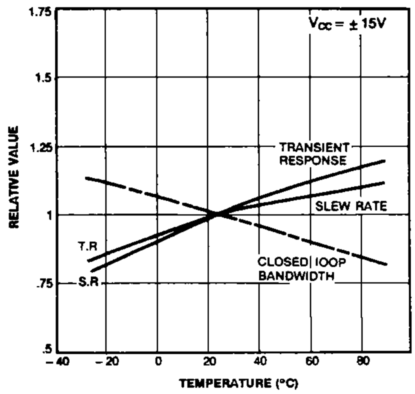


Fig. 15 FREQUENCY CHARACTERISTICS vs SUPPLY VOLTAGE

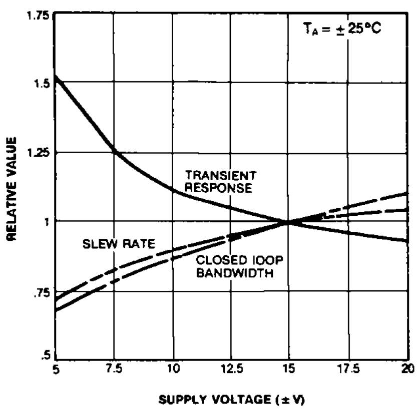


Fig. 16 OUTPUT SHORT CIRCUIT CURRENT vs AMBIENT TEMPERATURE

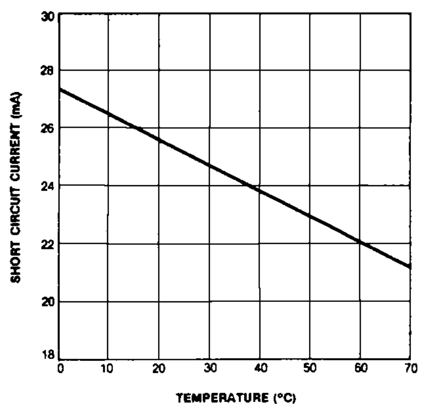


Fig. 17 TRANSIENT RESPONSE

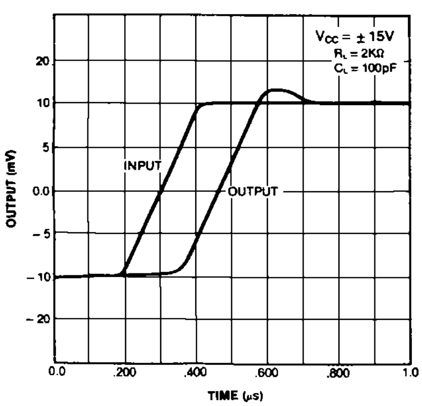


Fig. 18 COMMON-MODE REJECTION RATIO vs FREQUENCY

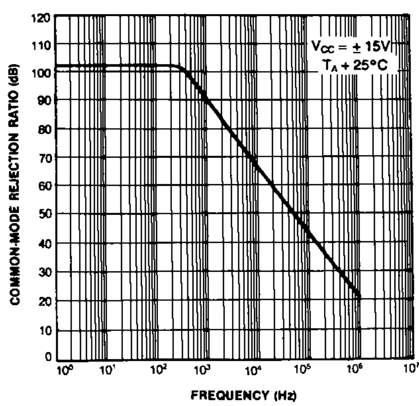


Fig. 18 VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

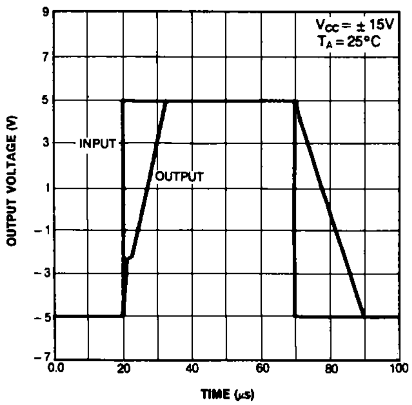
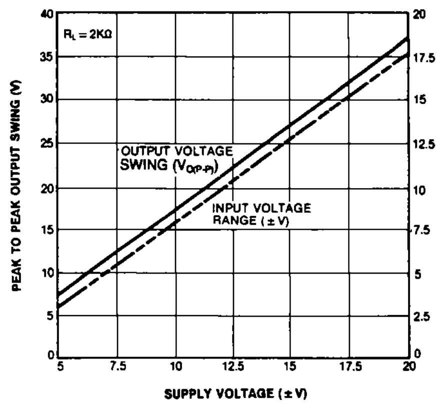


Fig. 19 OUTPUT SWING AND INPUT RANGE vs SUPPLY VOLTAGE



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

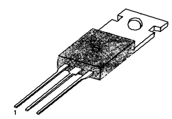
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

LM78XX (KA78XX, MC78XX) FIXED VOLTAGE REGULATOR (POSITIVE)

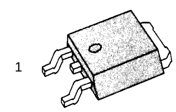
3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The LM78XX series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



D-PAK



1: Input 2: GND 3: Output

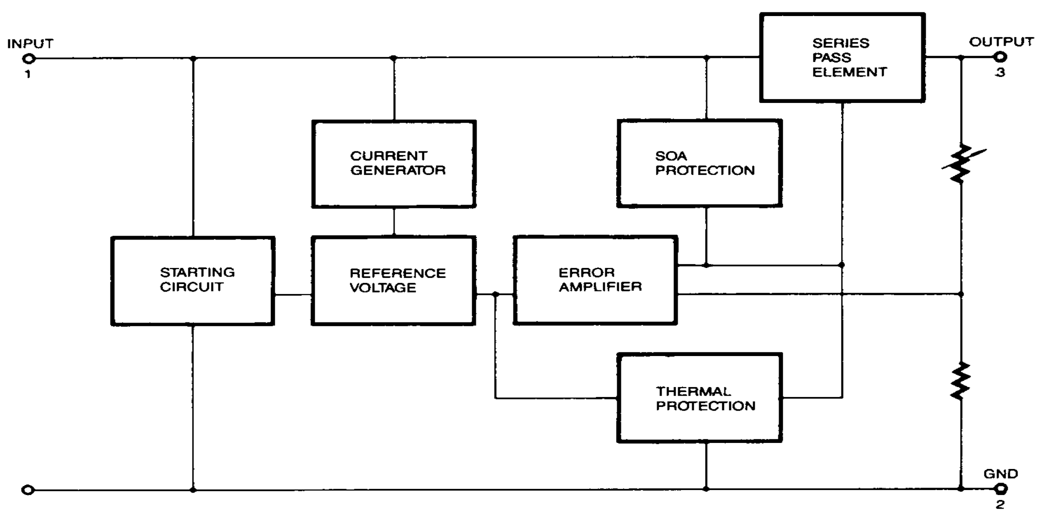
FEATURES

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection

ORDERING INFORMATION

Device	Output Voltage Tolerance	Packag e	Operating Temperature
KA78XXCT	± 4%	TO-220	0 ~ +125 °C
KA78XXAT	± 2%		
KA78XXIT	± 4%		-40 ~ +125 °C
KA78XXR		D-PAK	0 ~ +125 °C
KA78XXAR	± 2%		
KA78XXIR	± 4%		-40 ~ +125 °C

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range KA78XX/A/R/RA KA78XXI/RI	T_{OPR}	0 ~ +125 -40 ~ +125	°C °C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

LM7805/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, I_O = 500mA, V_I = 10V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7805I			LM7805			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤1.0A, P_O ≤ 15W V_I = 7V to 20V V_I = 8V to 20V		4.75	5.0	5.25	4.75	5.0	5.25	
Line Regulation	ΔV_O	T_J=+25°C	V_O = 7V to 25V		4.0	100		4.0	100	mV
			V_I = 8V to 12V		1.6	50		1.6	50	
Load Regulation	ΔV_O	T_J=+25°C	I_O = 5.0mA to1.5A		9	100		9	100	mV
			I_O =250mA to 750mA		4	50		4	50	
Quiescent Current	I_Q	T_J =+25 °C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A			0.03	0.5		0.03	0.5	mA
		V_I= 7V to 25V						0.3	1.3	
		V_I= 8V to 25V			0.3	1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA			-0.8			-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A=+25 °C			42			42		µV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8 to 18V		62	73		62	73		dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			15			15		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C			230			230		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7806/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, I_O=500mA, V_I= 11V C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7806I			LM7806			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		5.75	6.0	6.25	5.75	6.0	6.25	V
		5.0mA ≤ I_O ≤1.0A, P_D ≤ 15W V_I = 8.0V to 21V					5.7	6.0	6.3	
		V_I = 9.0V to 21V		5.7	6.0	6.3				
Line Regulation	ΔV_O	T_J=+25 °C	V_I = 8V to 25V		5	120		5	120	mV
			V_I = 9V to 13V		1.5	60		1.5	60	
Load Regulation	ΔV_O	T_J=+25 °C	I_O =5mA to 1.5A		9	120		9	120	mV
			I_O =250mA to750A		3	60		3	60	
Quiescent Current	I_Q	T_J =+25 °C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A				0.5			0.5	mA
		V_I = 8V to 25V							1.3	
		V_I = 9V to 25V				1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.8			-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			45			45		µV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 9V to 19V		59	75		59	75		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2			2		V
Output Resistance	R_D	f = 1KHz			19			19		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A=+25°C			250			250		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7808/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test Circuit, $T_{MIN} < T_J < T_{MAX}$, I_O = 500mA, V_I = 14V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7808I			LM7808			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		7.7	8.0	8.3	7.7	8.0	8.3	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 10.5V to 23V					7.6	8.0	8.4	
		V_I = 11.5V to 23V		7.6	8.0	8.4				
Line Regulation	ΔV_O	T_J =+ 25°C	V_I = 10.5V to 25V		5.0	160		5.0	160	mV
			V_I = 11.5V to 17V		2.0	80		2.0	80	
Load Regulation	ΔV_O	T_J = +25°C	I_O = 5.0mA to 1.5A		10	160		10	160	mV
			I_O= 250mA to 750mA		5.0	80		5.0	80	
Quiescent Current	I_Q	T_J =+25 °C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A			0.05	0.5		0.05	0.5	mA
		V_I = 10.5A to 25V						0.5	1.0	
		V_I = 11.5V to 25V			0.5	1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.8			-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			52			52		µV/Vo
Ripple Rejection	RR	f = 120Hz, V_I= 11.5V to 21.5		56	73		56	73		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			17			17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			230			230		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7809/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit. $T_{MIN} < T_J < T_{MAX}$, I_O= 500mA, V_I= 15V, C_I = 0.33µF, C_O = 0.1µF. unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7809I			LM7809			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		8.65	9	9.35	8.65	9	9.35	V
		5.0mA ≤ I_O ≤1.0A, P_D ≤15W V_I= 11.5V to 24V V_I = 12.5V to 24V		8.6	9	9.4	8.6	9	9.4	
Line Regulation	ΔV_O	T_J=+25 °C	V_I = 11.5V to 25V		6	180		6	180	mV
			V_I = 12V to 25v		2	90		2	90	
Load Regulation	ΔV_O	T_J=+25 °C	I_O = 5mA to 1.5A		12	180		12	180	mV
			I_O = 250mA to 750mA		4	90		4	90	
Quiescent Current	I_Q	T_J=+25 °C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A				0.5			0.5	mA
		V_I = 11.5V to 26V							1.3	
		V_I = 12.5V to 26V				1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			58			58		µV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 13V to 23V		56	71		56	71		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			17			17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250			250		mA
Peak Current	I_{PK}	T_J= +25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7810/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, I_O= 500mA, V_I =16V, C_I = 0.33μF, C_O= 0.1μF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7810I			LM7810			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		9.6	10	10.4	9.6	10	10.4	V
		5.0mA ≤ I_O ≤1.0A, P_D ≤15W V_I = 12.5V to 25V V_I= 13.5V to 25V		9.5	10	10.5	9.5	10	10.5	
Line Regulation	ΔV_O	T_J =+25°C	V_I = 12.5V to 25V		10	200		10	200	mV
			V_I = 13V to 25V		3	100		3	100	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5mA to 1.5A		12	200		12	200	mV
			I_O = 250mA to 750mA		4	400		4	400	
Quiescent Current	I_Q	T_J =+25 °C			5.1	8		5.1	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A				0.5			0.5	mA
		V_I = 12.5V to 29V							1.0	
		V_I = 13.5V to 29V				1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			58			58		μV/Vo
Ripple Rejection	RR	f = 120Hz V_I = 13V to 23V		56	71		56	71		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			17			17		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			250			250		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7811/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN}<T_J<T_{MAX}$, I_O = 500mA, V_I=18V, C_I=0.33µF, C_O = 0.IµF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7811I			LM7811			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		10.6	11	11.4	10.6	11	11.4	V
		5.0mA ≤ I_O ≤1.0A, P_D ≤15W V_I = 13.5V to 26V					10.5	11	11.5	
		V_I= 14.5V to 26V		10.5	11	11.5				
Line Regulation	ΔV_O	T_J =+25°C	V_I = 13.5V to 25V		10	220		10	220	mV
			V_I = 14V to 21V		3.0	110		3	110	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5.0mA to 1.5A		12	220		12	220	mV
			I_O = 250mA to 750mA		4	110		4	110	
Quiescent Current	I_Q	T_J =+25 °C			5.1	8		5.1	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A				0.5			0.5	mA
		V_I = 13.5V to 29V							1.0	
		V_I = 14.5V to 29V				1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			70			70		µV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 14V to 24V		55	71		55	71		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			18			18		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			250			250		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7812/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, I_O=500mA, V_I=19V, C_I= 0.33µF, C_O= 0.1.µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7812I			LM7812			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		11.5	12	12.5	11.5	12	12.5	V
		5.0mA ≤ I_O≤1.0A, P_D≤15W V_I = 14.5V to 27V V_I= 15.5V to 27V		11.4	12	12.6	11.4	12	12.6	
Line Regulation	ΔV_O	T_J =+25°C	V_I = 14.5V to 30V		10	240		10	240	mV
			V_I = 16V to 22V		3.0	120		3.0	120	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5mA to 1.5A		11	240		11	240	mV
			I_O = 250mA to 750mA		5.0	120		5.0	120	
Quiescent Current	I_Q	T_J =+25 °C			5.1	8		5.1	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A			0.1	0.5		0.1	0.5	mA
		V_I = 14.5V to 30V						0.5	1.0	
		V_I = 15V to 30V				1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		0.5	-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			76			76		mV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 15V to 25V		55	71		55	71		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			18			18		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			230			230		mA
Peak Current	I_{PK}	T_J = +25 °C			2.2			2.2		A

$T_{MIN} < T_J < T_{MAX}$
LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7815/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN}<T_J<T_{MAX}$, I_O =500mA, V_I =23V, C_I =0.33μF, C_O =0.1μF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7815I			LM7815			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		14.4	15	15.6	14.4	15	15.6	V
		5.0mA ≤ I_O≤1.0A, P_D≤15W V_I = 17.5V to 30V V_I= 18.5V to 30V		14.25	15	15.75	14.25	15	15.75	
Line Regulation	ΔV_O	T_J =+25°C	V_I = 17.5V to 30V		11	300		11	300	mV
			V_I = 20V to 26V		3	150		3	150	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5mA to 1.5A		12	300		12	300	mV
			I_O = 250mA to 750mA		4	150		4	150	
Quiescent Current	I_Q	T_J =+25 °C			5.2	8		5.2	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A				0.5			0.5	mA
		V_I = 17.5V to 30V							1.0	
		V_I = 18.5V to 30V				1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			90			90		μV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 18.5V to 28.5V		54	70		54	70		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			19			19		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			250			250		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN}<T_J<T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7818/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN}<T_J<T_{MAX}$, I_O =500mA, V_I =27V, C_I =0.33µF, C_O =0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7818I			LM7818			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		17.3	18	18.7	17.3	18	18.7	V
		5.0mA ≤ I_O ≤1.0A, P_D ≤15W, V_I = 21V to 33V					17.1	18	18.9	
		5.0mA ≤ I_O ≤1.0A, P_D ≤15W, V_I= 22V to 33V		17.1	18	18.9				
Line Regulation	ΔV_O	T_J =+25°C	V_I = 21V to 33V		15	360		15	360	mV
			V_I = 24V to 30V		5	180		5	180	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5mA to 1.5A		15	360		15	360	mV
			I_O = 250mA to 750mA		5.0	180		5.0	180	
Quiescent Current	I_Q	T_J =+25 °C			5.2	8		5.2	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A				0.5			0.5	mA
		V_I = 21V to 33V							1	
		V_I = 22V to 33V				1.0				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1			-1		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A =+25 °C			110			110		µV/V_O
Ripple Rejection	RR	f = 120Hz, V_I = 22V to 32V		53	69		53	69		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			22			22		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			250			250		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7824/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN}<T_J<T_{MAX}$, I_O = 500mA, V_I = 33V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7824I			LM7824			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25 °C		23	24	25	23	24	25	V
		5.0mA ≤ I_O ≤ 1.0A, P_D ≤ 15W V_I = 27V to 38V V_I= 28V to 38V		22.8	24	25.2	22.8	24	25.25	
Line Regulation	ΔV_O	T_J =+25°C	V_I = 27V to 38V		17	480		17	480	mV
			V_I = 30V to 36V		6	240		6	240	
Load Regulation	ΔV_O	T_J =+25°C	I_O = 5mA to 1.5A		15	480		15	480	mV
			I_O = 250mA to 750mA		5.0	240		5.0	240	
Quiescent Current	I_Q	T_J =+25 °C			5.2	8		5.2	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A			0.1	0.5		0.1	0.5	mA
		V_I = 27V to 38V						0.5	1	
		V_I = 28V to 38V			0.5	1				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.5			-1.5		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25 °C			160			60		µV/V_O
Ripple Rejection	RR	f = 120Hz V_I = 28V to 38V		50	67		50	67		dB
Dropout Voltage	V_D	I_O = 1A, T_J=+25 °C			2			2		V
Output Resistance	R_O	f = 1KHz			28			28		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A=+25 °C			230			230		mA
Peak Current	I_{PK}	T_J =+25 °C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40 °C, T_{MAX} = +125 °C
  LM78XX/R: T_{MIN}= 0 °C, T_{MAX}= +125 °C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7805A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +I25 °C, I_O = 1A, V_I = 10V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		4.9	5	5.1	V
		I_O = 5mA to 1A, $P_D \leq$ 5W V_I = 7.5 to 20V		4.8	5	5.2	
Line Regulation	ΔV_O	V_I = 7.5 to 25V I_O = 500mA			5	50	V
		V_I = 8V to 12V			3	50	
		T_J =+25 °C	V_I= 7.3V to 25V		5	50	
			V_I= 8V to 12V		1.5	25	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			9	100	V
		I_O = 5mA to 1A			9	100	
		I_O = 250 to 750mA			4	50	
Quiescent Current	I_Q	T_J =+25 °C			5.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A				0.5	mA
		V_I = 8 V to 25V, I_O = 500mA				0.8	
		V_I = 7.5V to 20V, T_J =+25 °C				0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA			-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 8V to 18V			68		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2		V
Output Resistance	R_O	f = 1KHz			17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J= +25 °C			2.2		A

*Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7806A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to+150 °C, I_O = 1A, V_I = 11V, C_I= 0.33µF, C_O= 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C	5.58	6	6.12	V
		I_O = 5mA to 1A, $P_D \leq$ 15W V_I = 8.6 to 21V	5.76	6	6.24	
Line Regulation	ΔV_O	V_I= 8.6 to 25V I_O = 500mA		5	60	mV
		V_I= 9V to 13V		3	60	
		T_J =+25 °C, V_I= 8.3V to 21V		5	60	
		T_J =+25 °C, V_I= 9V to 13V		1.5	30	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A		9	100	mV
		I_O = 5mA to 1A		4	100	
		I_O = 250 to 750mA		5.0	50	
Quiescent Current	I_Q	T_J =+25 °C		4.3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.5	mA
		V_I = 9V to 25V, I_O = 500mA			0.8	
		V_I= 8.5V to 21V, T_J =+25 °C			0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA		-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		10		µ V/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 9V to 19V		65		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C		2		V
Output Resistance	R_O	f = 1KHz		17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		250		mA
Peak Current	I_{PK}	T_J=+25 °C		2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7808A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to+150 °C, I_O = 1A, V_I = 14V, C_I = 0.33µF, C_O=0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		7.84	8	8.16	V
		I_O = 5mA to 1A, $P_D \leq$15W V_I = 8.6 to 21V		7.7	8	8.3	
Line Regulation	ΔV_O	V_I= 10.6 to 25V I_O = 500mA			6	80	mV
		V_I= 11to 17V			3	80	
		T_J =+25 °C	V_I= 10.4V to 23V		6	80	
			V_I= 11V to 17V		2	40	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			12	100	mV
		I_O = 5mA to 1A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25 °C			5.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A				0.5	mA
		V_I = 11V to 25V, I_O = 500mA				0.8	
		V_I= 10.6V to 23V, T_J =+25 °C				0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA			-0.8		mV /°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 11.5V to 21.5V			62		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2		V
Output Resistance	R_O	f = 1KHz			18		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25°C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7809A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +125 °C, I_O = 1A, V_I = 15V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		8.82	9.0	9.18	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 11.2 to 24V		8.65	9.0	9.35	
Line Regulation	ΔV_O	V_I= 11.7 to 25V I_O = 500mA			6	90	mV
		V_I= 12.5 to 19V			4	45	
		T_J =+25 °C	V_I= 11.5V to 24V		6	90	
			V_I= 12.5V to 19V		2	45	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.0A			12	100	mV
		I_O = 5mA to 1.0A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25 °C			5.0	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 11.7V to 25V, T_J=+25 °C				0.8	mA
		V_I = 12V to 25V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.5	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 12V to 22V			62		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2.0		V
Output Resistance	R_O	f = 1KHz			17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7810A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to+125 °C, I_O = 1A, V_I = 16V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		9.8	10	10.2	V
		I_O = 5mA to 1A, $P_D \leq$ 15W V_I =12.8 to 25V		9.6	10	10.4	
Line Regulation	ΔV_O	V_I= 12.8 to 26V I_O = 500mA			8	100	mV
		V_I= 13to 20V			4	50	
		T_J =+25 °C	V_I= 12.5V to 25V		8	100	
			V_I= 13V to 20V		3	50	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			12	100	mV
		I_O = 5mA to 1.0A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25 °C			5.0	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 13V to 26V, T_J=+25 °C				0.5	mA
		V_I = 12.8V to 25V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.5	
Output Voltage Drift	ΔV/ΔT	I_O = 5mA			-1.0		mV °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 14V to 24V			62		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2.0		V
Output Resistance	R_O	f = 1KHz			17		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7811A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +125°C, I_O = 1A, V_I = 18V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25°C		10.8	11.0	11.2	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 13.8 to 26V		10.6	11.0	11.4	
Line Regulation	ΔV_O	V_I= 12.8 to 26V I_O = 500mA			10	110	mV
		V_I= 15 to 21V			4	55	
		T_J =+25°C	V_I= 13.5V to 26V		10	110	
			V_I= 15V to 21V		3	55	
Load Regulation	ΔV_O	T_J =+25°C I_O = 5mA to 1.5A			12	100	mV
		I_O = 5mA to 1.0A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25°C			5.1	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 13.8V to 26V, T_J=+25°C				0.8	mA
		V_I = 14V to 27V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.5	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV /°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25°C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 14V to 24V			61		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25°C			2.0		V
Output Resistance	R_O	f = 1KHz			18		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25°C			250		mA
Peak Current	I_{PK}	T_J=+25°C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7812A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +125 °C, I_O = 1A, V_I = 19V, C_I = 0.33µF, C_O= 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		11.75	12	12.25	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 14.8 to 27V		11.5	12	12.5	
Line Regulation	ΔV_O	V_I= 14.8 to 30V I_O = 500mA			10	120	mV
		V_I= 16 to 22V			4	120	
		T_J =+25°C	V_I= 14.5V to 27V		10	120	
			V_I= 16V to 22V		3	60	
Load Regulation	ΔV_O	T_J =+25°C I_O = 5mA to 1.5A			12	100	mV
		I_O = 5mA to 1.0A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25 °C			5.1	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 15V to 30V, T_J=+25 °C				0.5	mA
		V_I = 14V to 27V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.8	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 14V to 24V			60		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2.0		V
Output Resistance	R_O	f = 1KHz			18		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7815A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +150 °C, I_O =1A, V_I=23V, C_I = 0.33µF, C_O=0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		14.7	15	15.3	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 17.7 to 30V		14.4	15	15.6	
Line Regulation	ΔV_O	V_I= 17.9 to 30V I_O = 500mA			10	150	mV
		V_I= 20 to 26V			5	150	
		T_J =+25 °C	V_I= 17.5V to 30V		11	150	
			V_I= 20V to 26V		3	75	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			12	100	mV
		I_O = 5mA to 1.0A			12	100	
		I_O = 250 to 750mA			5	50	
Quiescent Current	I_Q	T_J =+25 °C			5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 17.5V to 30V, T_J =+25 °C				0.5	mA
		V_I = 17.5V to 30V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.8	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 18.5V to 28.5V			58		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2.0		V
Output Resistance	R_O	f = 1KHz			19		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7818A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +150 °C, I_O=1A, V_I = 27V, C_I= 0.33µF, C_O = 0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		17.64	18	18.36	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 21 to 33V		17.3	18	18.7	
Line Regulation	ΔV_O	V_I= 21 to 33V I_O = 500mA			15	180	mV
		V_I= 21 to 33V			5	180	
		T_J =+25 °C	V_I= 20.6V to 33V		15	180	
			V_I= 24V to 30V		5	90	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			15	100	mV
		I_O = 5mA to 1.0A			15	100	
		I_O = 250 to 750mA			7	50	
Quiescent Current	I_Q	T_J =+25 °C			5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 21V to 33V, T_J=+25 °C				0.5	mA
		V_I = 21V to 33V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.8	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 18.5V to 28.5V			57		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25 °C			2.0		V
Output Resistance	R_O	f = 1KHz			19		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7824A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits. T_J = 0 to +150 °C, I_O =1A, V_I = 33V, C_I= 0.33µF, C_O=0.1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25 °C		23.5	24	24.5	V
		I_O = 5mA to 1A, P_D ≤15W V_I = 27.3 to 38V		23	24	25	
Line Regulation	ΔV_O	V_I= 27 to 38V I_O = 500mA			18	240	mV
		V_I= 21 to 33V			6	240	
		T_J =+25 °C	V_I= 26.7V to 38V		18	240	
			V_I= 30V to 36V		6	120	
Load Regulation	ΔV_O	T_J =+25 °C I_O = 5mA to 1.5A			15	100	mV
		I_O = 5mA to 1.0A			15	100	
		I_O = 250 to 750mA			7	50	
Quiescent Current	I_Q	T_J =+25 °C			5.2	6.0	mA
Quiescent Current Change	ΔI_Q	V_I = 27.3V to 38V, T_J =+25 °C				0.5	mA
		V_I = 27.3V to 38V, I_O = 500mA				0.8	
		I_O = 5mA to 1.0A				0.8	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.5		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A = 25 °C			10		µV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 18.5V to 28.5V			54		dB
Dropout Voltage	V_D	I_O = 1A, T_J =+25°C			2.0		V
Output Resistance	R_O	f = 1KHz			20		mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C			250		mA
Peak Current	I_{PK}	T_J=+25 °C			2.2		A

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 Quiescent Current

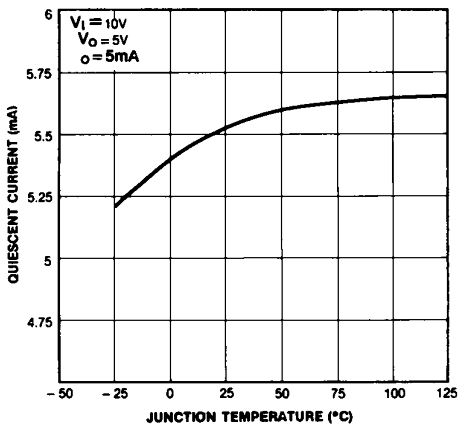


Fig. 2 Peak Output Current

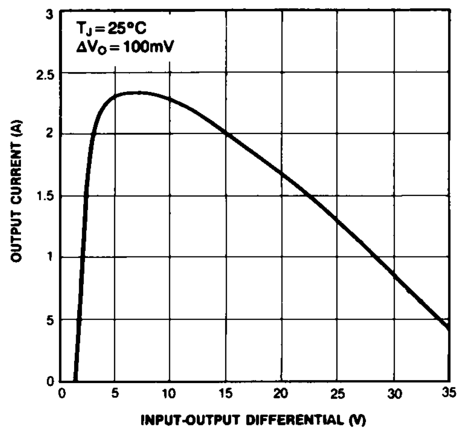


Fig. 3 Output Voltage

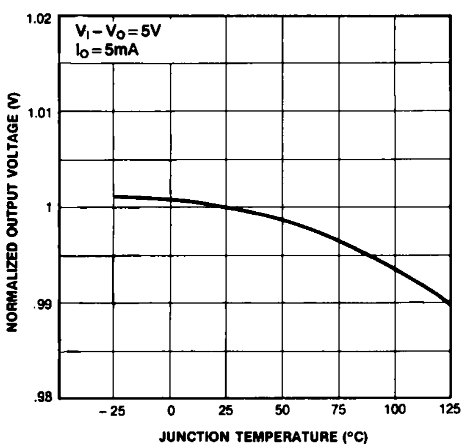
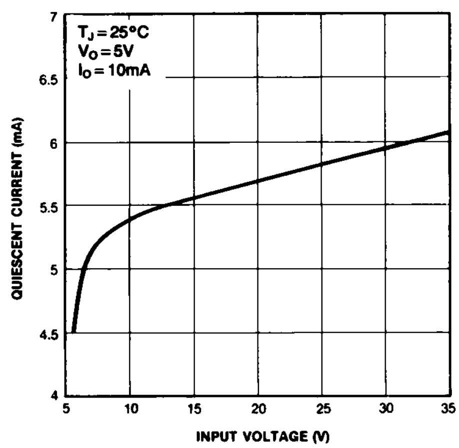


Fig. 4 Quiescent Current



TYPICAL APPLICATIONS

Fig. 5 DC Parameters

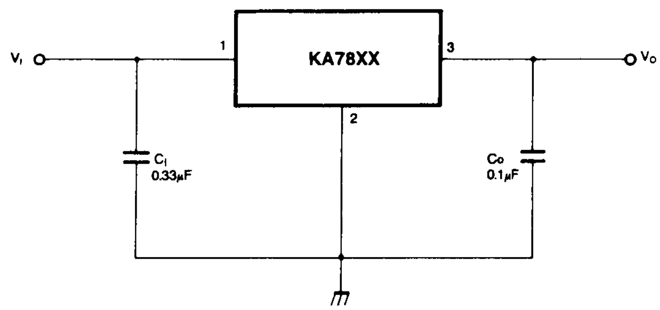


Fig. 6 Load Regulation

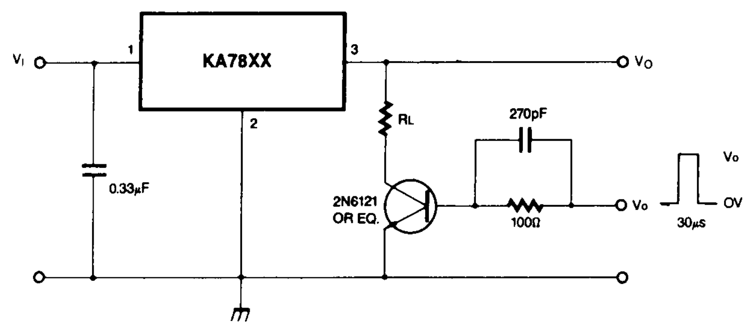
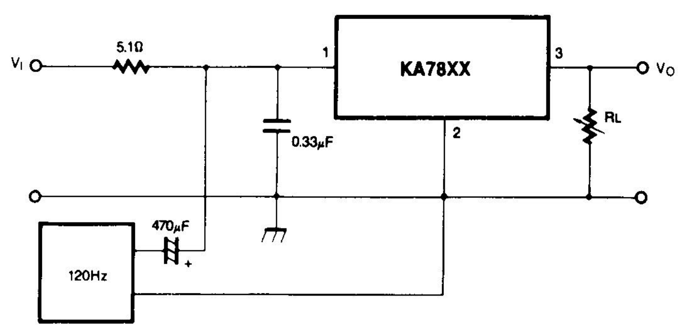


Fig. 7 Ripple Rejection



TYPICAL APPLICATIONS (Continued)

Fig. 8 Fixed Output Regulator

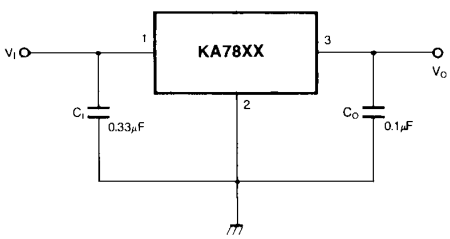
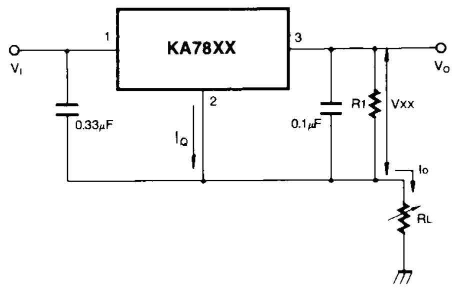


Fig. 9 Constant Current Regulator



$I_O = \frac{}{R_1} + I_Q$

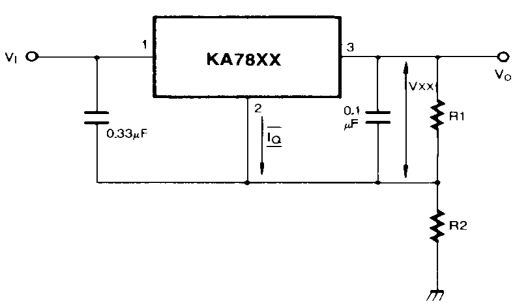
Notes:

(1) To specify an output voltage. substitute voltage value for "XX."
A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

(2) C_I is required if regulator is located an appreciable distance from power Supply filter.

(3) C_O improves stability and transient response.

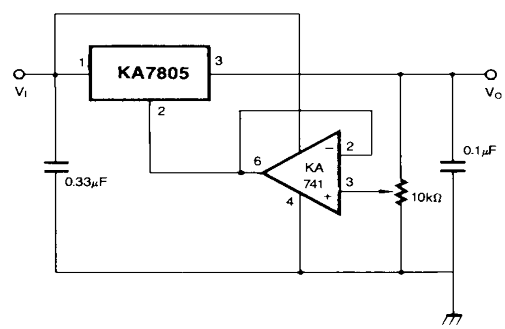
Fig. 10 Circuit for Increasing Output Voltage



$I_{RI} \geq 5\ I_Q$

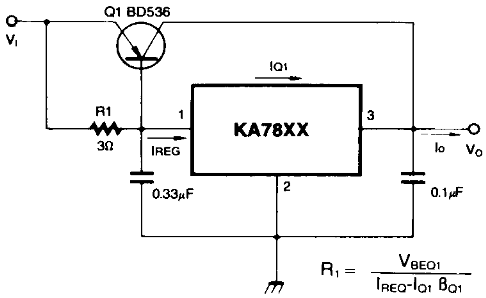
$V_O = V_{XX}\,(1+R_2/R_1)+I_QR_2$

Fig. 11 Adjustable Output Regulator (7 to 30V)



TYPICAL APPLICATIONS (Continued)

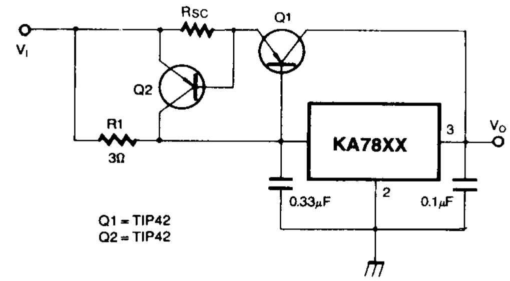
Fig. 12 High Current Voltage Regulator



$$R_1 = \frac{V_{BEQ1}}{I_{REG} - I_{Q1}\,\beta_{Q1}}$$

$$I_O = I_{REG} + \beta_{Q1}\,(I_{REG} - V_{BEQ1}/R_1)$$

Fig. 13 High Output Current with Short Circuit Protection



$$R_{SC} = \frac{V_{BEQ2}}{I_{SC}}$$

Fig. 14 Tracking Voltage Regulator

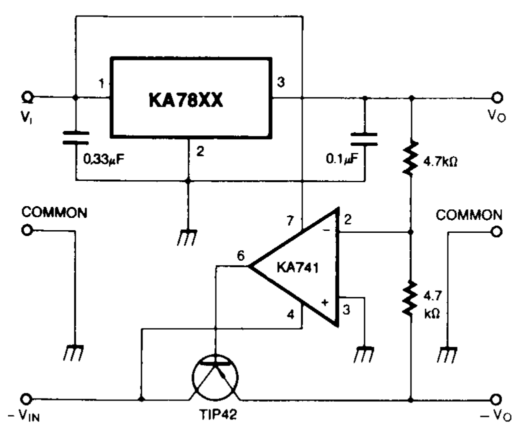
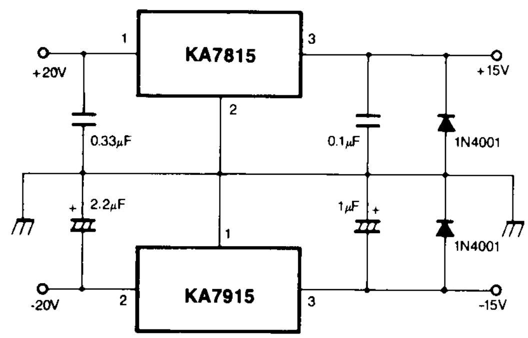


Fig. 15 Split Power Supply (±15V-1A)



TYPICAL APPLICATIONS (Continued)

Fig. 16 Negative Output Voltage Circuit

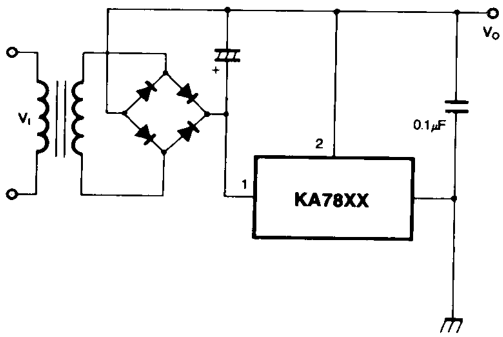
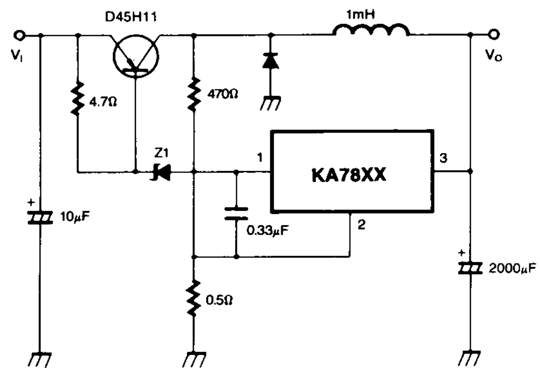


Fig. 17 switching Regulator



PRODUCT STATUS DEFINITIONS

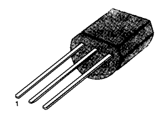
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

3-TERMINAL 0.1A POSITIVE VOLTAGE REGULATORS

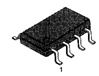
The LM78LXX series of fixed voltage monolithic integrated circuit voltage regulators are suitable for application that required supply up to 100mA.

TO-92



1: Output 2: GND 3: Input

8 SOP



1: Output 2: GND 3: GND 4: NC
5: NC 6: GND 7: GND 8: Input

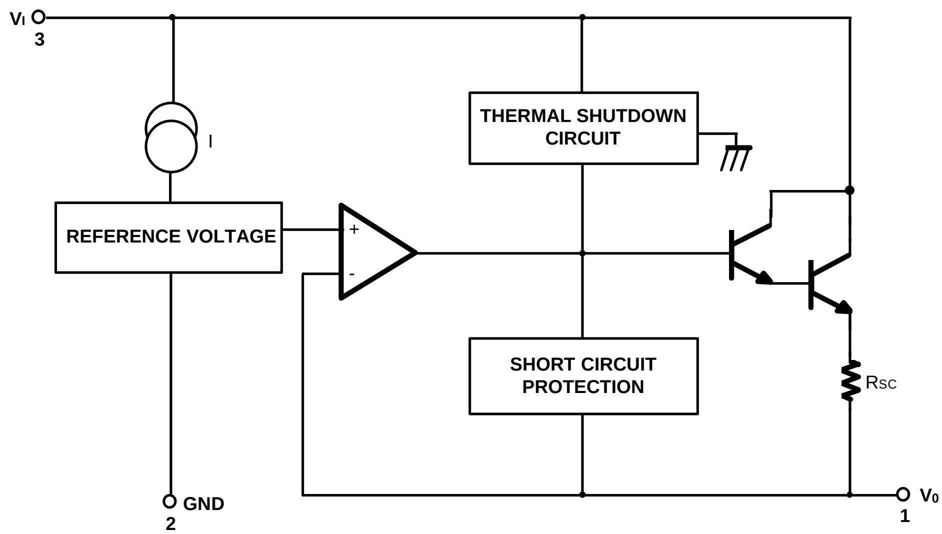
FEATURES

- Maximum Output Current of 100mA
- Output Voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V and 24V
- Thermal Overload Protection
- Short Circuit Current Limiting
- Output Voltage Offered in ± 5% Tolerance

ORDERING INFORMATION

Device	Package	Operating Temperature
LM78LXXACZ	TO-92	- 45 ~ + 125°C
LM78LXXM	8 SOP	0 ~ + 125°C

BLOCK DIAGRAM



Rev. B

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V, 8V) (for V_O = 12V, 15V)	V_I	30 35	V V
Operating Junction Temperature Range	T_J	0 ~ +150	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

LM78L05 ELECTRICAL CHARACTERISTICS

(V_I = 10V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 μF, C_O = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		ΔV_O	T_J = 25°C	7V ≤ V_I ≤ 20V		8	150	mV
				8V ≤ V_I ≤ 20V		6	100	mV
Load Regulation		ΔV_O	T_J = 25°C	1mA ≤ I_O ≤ 100mA		11	60	mV
				1mA ≤ I_O ≤ 40mA		5.0	30	mV
Output Voltage		V_O	7V ≤V_I ≤ 0V	1mA ≤ I_O ≤ 40mA			5.25	V
			7V ≤V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	4.75		5.25	V
Quiescent Current		I_Q	T_J = 25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_Q	8V ≤V_I ≤ 20V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40 mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25 °C, 10Hz ≤ f ≤ 100KHz			40		μV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-0.65		mV/°C
Ripple Rejection		RR	f = 120Hz, 8V ≤ V_I ≤ 18V, T_J = 25°C		41	80		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L06 ELECTRICAL CHARACTERISTICS

(V_I = 12V, I_O = 40mA, 0°C ≤ T_J ≤ 125 °C , C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		ΔV_O	T_J =25°C	8.5V < V_I < 20V		64	175	mV
				9V ≥ V_I ≥ 20V		54	125	mV
Load Regulation		ΔV_O	T_J =25°C	1mA < I_O < 100mA		12.8	80	mV
				1mA < I_O < 70mA		5.8	40	mV
Output Voltage		V_O	8.5 < V_I < 20V, 1mA < I_O < 40mA		5.7		6.3	V
			8.5 < V_I < V_{MAX}(Note), 1mA < I_O < 70mA		5.7		6.3	
Quiescent Current		I_Q	T_J = 25°C			3.9	6.0	mA
			T_J = 125°C				5.5	
Quiescent Current Change	with line	ΔI_Q	9 < V_I < 20V				1.5	mA
	with load	ΔI_Q	1mA < I_O< 40mA				0.1	
Output Noise Voltage		V_N	T_A = 25°C, 10Hz < f < 100KHz			40		μV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			0.75		mV/°C
Ripple Rejection		RR	f = 120Hz, 10V < V_I < 20V, T_J = 25°C		40	46		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L08 ELECTRICAL CHARACTERISTICS

(V_I = 14V, I_O = 40mA, 0°C ≤ T_J ≤ 125 °C, C_I = 0.33 μF, C_O = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		ΔV_O	T_J =25°C	10.5V ≤ V_I ≤ 23V		10	175	mV
				11V ≤ V_I ≤ 23V		8	125	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O ≤ 100mA		15	80	mV
				1mA ≤ I_O ≤ 40mA		8.0	40	mV
Output Voltage		V_O	10.5V ≤ V_I ≤ 23V	1mA ≤ I_O ≤ 40mA	7.6		8.4	V
			10.5V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	7.6		8.4	V
Quiescent Current		I_Q	T_J = 25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_Q	11V ≤ V_I ≤ 23V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤100KHz			60		μV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-0.8		mV/°C
Ripple Rejection		RR	f = 120Hz, 11V ≤ V_I ≤ 21V, T_J = 25°C		39	70		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L09 ELECTRICAL CHARACTERISTICS

(V_I = 15V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		8.64	9.0	9.36	V
Line Regulation		ΔV_O	T_J =25°C	11.5V ≤ V_I ≤ 24V		90	200	mV
				13V ≤ V_I ≤ 24V		100	150	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O ≤ 100mA		20	90	mV
				1mA ≤ I_O ≤ 40mA		10	45	mV
Output Voltage		V_O	11.5V ≤ V_I ≤ 24V	1mA ≤ I_O ≤ 40mA	8.55		9.45	V
			11.5V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	8.55		9.45	V
Quiescent Current		I_Q	T_J = 25°C			2.1	6.0	mA
Quiescent Current Change	with line	ΔI_Q	13V ≤ V_I ≤ 24V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤ 100KHz			70		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-0.9		mV/°C
Ripple Rejection		RR	f = 120Hz, 12V ≤ V_I ≤ 22V, T_J = 25°C		38	44		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L10 ELECTRICAL CHARACTERISTICS

(V_I = 16V, I_O = 40mA, 0°C < T_J < 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		9.6	10.0	10.4	V
Line Regulation		ΔV_O	T_J =25°C	12.5 < V_I < 25V		100	220	mV
				14V ≥ V_I ≥ 25V		100	170	mV
Load Regulation		ΔV_O	T_J =25°C	1mA < I_O< 100mA		20	94	mV
				1mA < I_O < 70mA		10	47	mV
Output Voltage		V_O	12.5 < V_I < 25V, 1mA < I_O < 40mA		9.5		10.5	V
			12.5 < V_I < V_{MAX}(Note), 1mA < I_O < 70mA		9.5		10.5	
Quiescent Current		I_Q	T_J = 25°C			4.2	6.5	mA
			T_J = 125°C				6.0	
Quiescent Current Change	with line	ΔI_Q	12.5 < V_I < 25V				1.5	mA
	with load	ΔI_Q	1mA < I_O < 40mA				0.1	
Output Noise Voltage		V_N	T_A = 25°C, 10Hz < f < 100KHz			74		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			0.95		mV/°C
Ripple Rejection		RR	f = 120Hz, 15V < V_I < 25V, T_J = 25°C		38	43		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L12 ELECTRICAL CHARACTERISTICS

(V_I = 19V, I_O = 40mA, 0°C ≤T_J ≤ 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		11.5	12	12.5	V
Line Regulation		ΔV_O	T_J =25°C	14.5V ≤ V_I ≤ 27V		20	250	mV
				16V ≤ V_I ≤ 27V		15	200	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O ≤ 100mA		20	100	mV
				1mA ≤ I_O ≤ 40mA		10	50	mV
Output Voltage		V_O	14.5V ≤ V_I ≤ 27V	1mA ≤ I_O ≤ 40mA	11.4		12.6	V
			14.5V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	11.4		12.6	V
Quiescent Current		I_Q	T_J = 25°C			2.1	6.0	mA
Quiescent Current Change	with line	ΔI_Q	16V ≤ V_I ≤ 27V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤ 100KHz			80		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/°C
Ripple Rejection		RR	f = 120Hz, 15V ≤ V_I ≤ 25V, T_J = 25°C		37	65		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L15 ELECTRICAL CHARACTERISTICS

(V_I = 23V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		14.4	15	15.6	V
Line Regulation		ΔV_O	T_J =25°C	17.5V ≤ V_I ≤ 30V		25	300	mV
				20V ≤ V_I ≤ 30V		20	250	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O ≤ 100mA		25	150	mV
				1mA ≤ I_O ≤ 40mA		12	75	mV
Output Voltage		V_O	17.5V ≤ V_I ≤ 30V	1mA ≤ I_O ≤ 40mA	14.25		15.75	V
			17.5V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	14.25		15.75	V
Quiescent Current		I_Q	T_J = 25°C			2.1	6.0	mA
Quiescent Current Change	with line	ΔI_Q	20V ≤ V_I ≤ 30V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤ 100KHz			90		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-1.3		mV/°C
Ripple Rejection		RR	f = 120Hz, 18.5V ≤ V_I ≤ 28.5V, T_J = 25°C		34	60		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L18 ELECTRICAL CHARACTERISTICS

(V_I = 27V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		17.3	18	18.7	V
Line Regulation		ΔV_O	T_J =25°C	21V ≤ V_I ≤ 33V		145	300	mV
				22V ≤ V_I ≤ 33V		135	250	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O≤100mA		30	170	mV
				1mA ≤ I_O ≤ 40mA		15	85	mV
Output Voltage		V_O	21V ≤ V_I ≤ 33V	1mA ≤ I_O ≤ 40mA	17.1		18.9	V
			21V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	17.1		18.9	V
Quiescent Current		I_Q	T_J = 25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_Q	21V ≤ V_I ≤ 33V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤ 100KHz			150		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-1.8		mV/°C
Ripple Rejection		RR	f = 120Hz, 23V ≤ V_I ≤ 33V, T_J = 25°C		34	48		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

LM78L24 ELECTRICAL CHARACTERISTICS

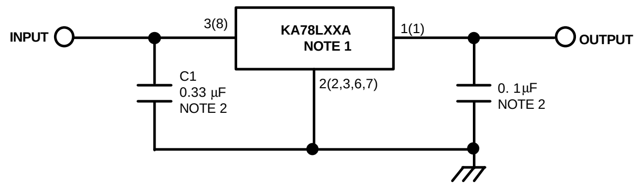
(V_I = 33V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33 µF, C_O = 0.1µF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = 25°C		23	24	25	V
Line Regulation		ΔV_O	T_J =25°C	27V ≤ V_I ≤ 38V		160	300	mV
				28V ≤ V_I ≤ 38V		150	250	mV
Load Regulation		ΔV_O	T_J =25°C	1mA ≤ I_O ≤ 100mA		40	200	mV
				1mA ≤ I_O ≤ 40mA		20	100	mV
Output Voltage		V_O	27V ≤ V_I ≤ 38V	1mA ≤ I_O ≤ 40mA	22.8		25.2	V
			27V ≤ V_I ≤ V_{MAX} (Note 2)	1mA ≤ I_O ≤ 70mA	22.8		25.2	V
Quiescent Current		I_Q	T_J = 25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_Q	28V ≤ V_I ≤ 38V				1.5	mA
	with load	ΔI_Q	1mA ≤ I_O ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_A = 25°C, 10Hz ≤ f ≤ 100KHz			200		µV/V_O
Temperature Coefficient of V_O		$\Delta V_O/\Delta T$	I_O = 5mA			-2.0		mV/°C
Ripple Rejection		RR	f = 120Hz, 28V ≤ V_I ≤ 38V, T_J = 25°C		34	45		dB
Dropout Voltage		V_D	T_J = 25°C			1.7		V

Notes

1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperature as indicated at the initiation of tests.
2. Power dissipation ≤ 0.75W.

TYPICAL APPLICATION



'( )' : 8SOP Type

Notes

1. To specify an output voltage, substitute voltage value for “XX”.
2. Bypass Capacitors are recommend for optimum stability and transient response and should be located as close as possible to the regulator

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

MC78MXX (LM78MXX) (KA78MXX)

3-Terminal 0.5A Positive Voltage Regulators

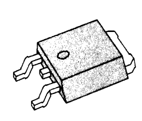
Features

- Output Current up to 0.5A
- Output Voltages of 5, 6, 8, 10, 12, 15, 18, 20, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection
- Industrial and commercial temperature range

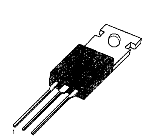
Description

The MC78MXX (LM78MXX) (KA78MXX) series of three-terminal positive regulators are available in the TO-220/ D-PAK package with several fixed output voltages making it useful in a wide range of applications.

TO-220

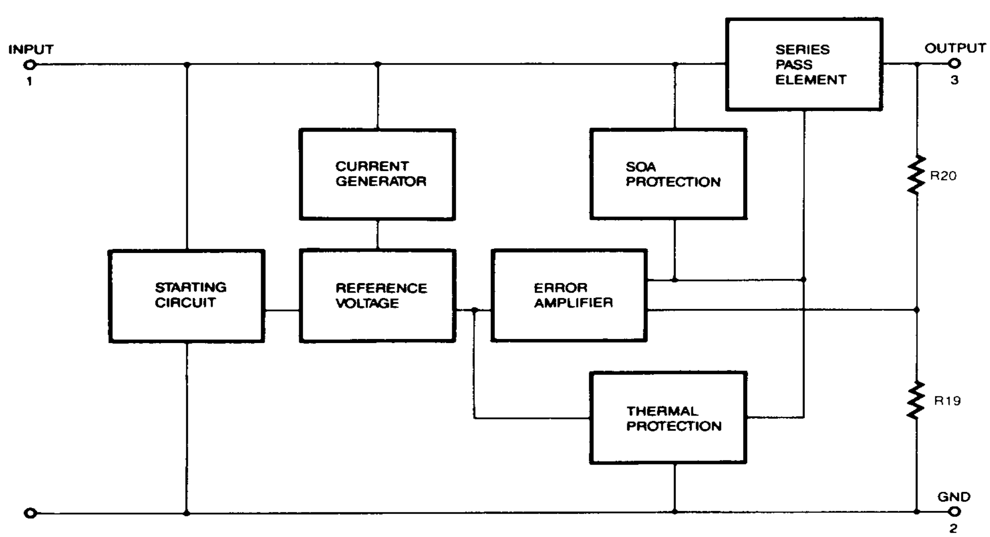


D-PAK



1. Input 2. GND 3. Output

Internal Block Diagram



Absolute Maximum Ratings (Ta=+25°C, Unless otherwise specified)

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range KA78MXXI/RI KA78MXX/R	T_{OPR}	-40~ + 125 0~ + 125	°C °C
Storage Temperature Range	T_{STG}	-65~ + 150	°C

KA78M05/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \le T_J \le$ +125°C, I_O=350mA, V_I=10V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C		4.8	5	5.2	V
		I_O = 5 to 350mA V_I= 7 to 20V		4.75	5	5.25	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 7 to 25V	-	-	100	mV
			V_I = 8 to 25V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	100	mV
		I_O = 5mA to 200mA, T_J =+25 °C		-	-	50	
Quiescent Current	I_Q	T_J=+25°C		-	4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 8 to 25V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	40	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 8 to 18V		62	-	-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J=+25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. $T_{MIN}<T_J<T_{MAX}$
   KA78MXX/RI: T_{MIN}= -40°C, T_{MAX} = +125°C
   KA78MXX/R: T_{MIN}= 0°C, T_{MAX} = +125°C
2. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M06/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I =11V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)(

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C		5.75	6	6.25	V
		I_O = 5 to 350mA V_I= 8 to 21V		5.7	6	6.3	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 8 to 25V	-	-	100	mV
			V_I = 9 to 25V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	120	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	60	
Quiescent Current	I_Q	T_J=+25°C		-	4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 9 to 25V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	45	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 9 to 19V		59	-	-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M08/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, $T_{MIN} \le T_J \le +125°C$, I_O=350mA, V_I=14V, unless otherwise specified, C_I =0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25 °C		7.7	8	8.3	V
		I_O = 5 to 350mA V_I= 10.5 to 23V		7.6	8	8.4	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 10.5 to 25V	-	-	100	mV
			V_I = 11 to 25V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	160	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	80	
Quiescent Current	I_Q	T_J=+25°C		-	4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 10.5 to 25V		-	-	0.8	
Output Voltage Drift	RR	I_O = 5mA T_J = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	52	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 9 to 19V		56	-	-	dB
Dropout Voltage	V_D	T_J =+25°C,I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J =+25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Fixed Voltage Regulator (Positive)

KA78M10/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I=17V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J= +25°C		9.6	10	10.4	V
		I_O = 5 to 350mA V_I= 12.5 to 25V		9.5	10	10.5	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 12.5 to 25V	-	-	100	mV
			V_I = 13 to 25V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	200	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	100	
Quiescent Current	I_Q	T_J=+25°C		-	4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 12.5 to 25V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	65	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 13 to 23V		55	-	-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M12/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq 125°C$, I_O=350mA, V_I =19V, unless otherwise specified, C_I =0.33mF, C_O =0.1mF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C	11.5	12	12.5	V
		I_O = 5 to 350mA V_I= 14.5 to 27V	11.5	12	12.6	
Line Regulation	ΔV_O	I_O = 200mA, T_J =+25°C, V_I= 14.5 to 30V	-	-	100	mV
		I_O = 200mA, T_J =+25°C, V_I = 16 to 30V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C	-	-	240	mV
		I_O = 5mA to 200mA, T_J =+25°C	-	-	120	
Quiescent Current	I_Q	T_J=+25°C	-	4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA	-		0.5	mA
		I_O = 200mA V_I = 14.5 to 30V	-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C	-	- 0.5	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz	-	75	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 15 to 25V	55		-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA	-	2	-	V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I= 35V	-	300	-	mA
Peak Current	I_{PK}	T_J = +25°C	-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M15/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I =23V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C		14.4	15	15.6	V
		I_O = 5 to 350mA V_I= 17.5 to 30V		14.25	15	15.75	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 17.5 to 30V	-	-	100	mV
			V_I = 20 to 30V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	300	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	150	
Quiescent Current	I_Q	T_J=+25°C		-	4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 17.5 to 30V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	- 1	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	100	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 18.5 to 28.5V		54			dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J = + 25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M18/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I =26V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C		17.3	18	18.7	V
		I_O = 5 to 350mA V_I= 20.5 to 33V		17.1	18	18.9	
Line Regulation	ΔV_O	I_O = 200mA	V_I= 21 to 33V	-	-	100	mV
		T_J =+25°C	V_I = 24 to 33V	-	-	50	
Load Regulation	ΔVO	I_O = 5mA to 0.5A, T_J =+25°C		-	-	360	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	180	
Quiescent Current	I_Q	T_J =+25°C		-	4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 21 to 33V		-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I_O =5mA T_J =0 to 125°C		-	-1.1	-	mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz			100	-	µV/V_O
Ripple Rejection	RR	f=120Hz, I_O=300mA		53		-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O=500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J =+25°C, V_I=35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/R: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M20/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I =29V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J= +25°C		19.2	20	20.8	V
		I_O = 5 to 350mA V_I= 23 to 35V		19	20	21	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 23 to 35V	-	-	100	mV
			V_I = 24 to 35V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	400	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	200	
Quiescent Current	I_Q	T_J=+25°C		-	4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 23 to 35V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	-1.1	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	110	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 24 to 34V		53	-	-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J = +25°C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J = +25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA78M24/I/R/RI Electrical Characteristics

(Refer to the test circuits, $T_{MIN} \leq T_J \leq +125°C$, I_O=350mA, V_I=33V, unless otherwise specified, C_I = 0.33mF, C_O=0.1mF)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Voltage	V_O	T_J=+25°C		23	24	25	V
		I_O = 5 to 350mA V_I= 27 to 38V		22.8	24	25.2	
Line Regulation	ΔV_O	I_O = 200mA T_J =+25°C	V_I= 27 to 38V	-	-	100	mV
			V_I = 28 to 38V	-	-	50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J =+25°C		-	-	480	mV
		I_O = 5mA to 200mA, T_J =+25°C		-	-	240	
Quiescent Current	I_Q	T_J=+25°C		-	4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA		-	-	0.5	mA
		I_O = 200mA V_I = 27 to 38V		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	I_O = 5mA T_J = 0 to +125°C		-	- 1.2	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		-	170	-	mV/V_O
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 28 to 38V		50	-	-	dB
Dropout Voltage	V_D	T_J =+25°C, I_O = 500mA		-	2	-	V
Short Circuit Current	I_{SC}	T_J= +25 °C, V_I= 35V		-	300	-	mA
Peak Current	I_{PK}	T_J =+25°C		-	700	-	mA

NOTE:

1. T_{MIN}:
   KA78MXX/RI: T_{MIN} = -40°C
   KA78MXX/R: T_{MIN} = 0°C
2. Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Applications

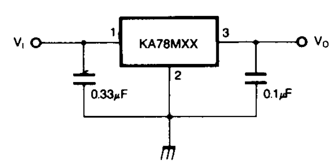


Figure 1. Fixed Output Regulator

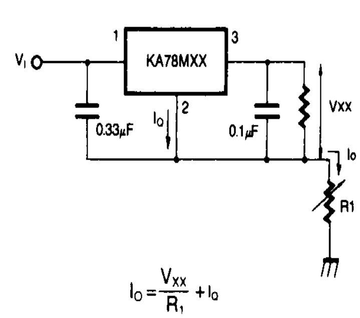


Figure 2. Constant Current Regulator

Notes:
1. To specify an output voltage, substitute voltage value for "XX"
2. Although no output capacitor is needed for stability, it does improve transient response.
3. Required if regulator is located an appreciable distance from power Supply filter

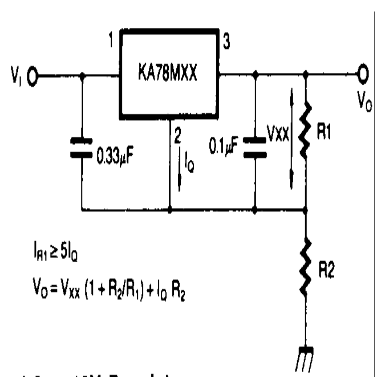


Figure 3. Circuit for Increasing Output Voltage

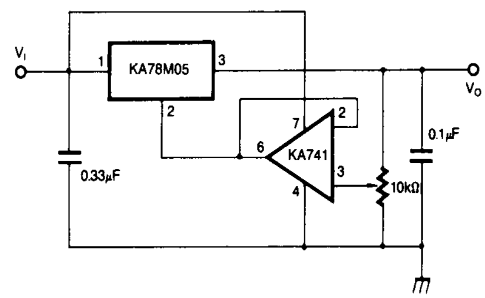
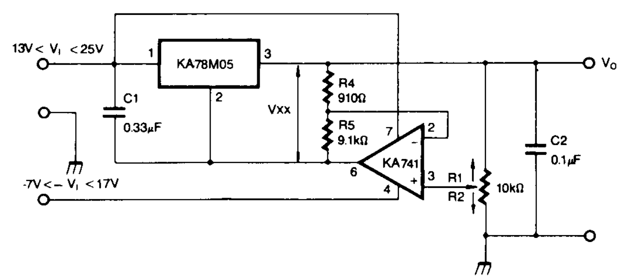


Figure 4. Adjustable Output Regulator (7 to 30V)



$$V_O = V_{XX} \frac{R_4}{R_1}$$

Figure 5. 0.5 to 10V Regulator

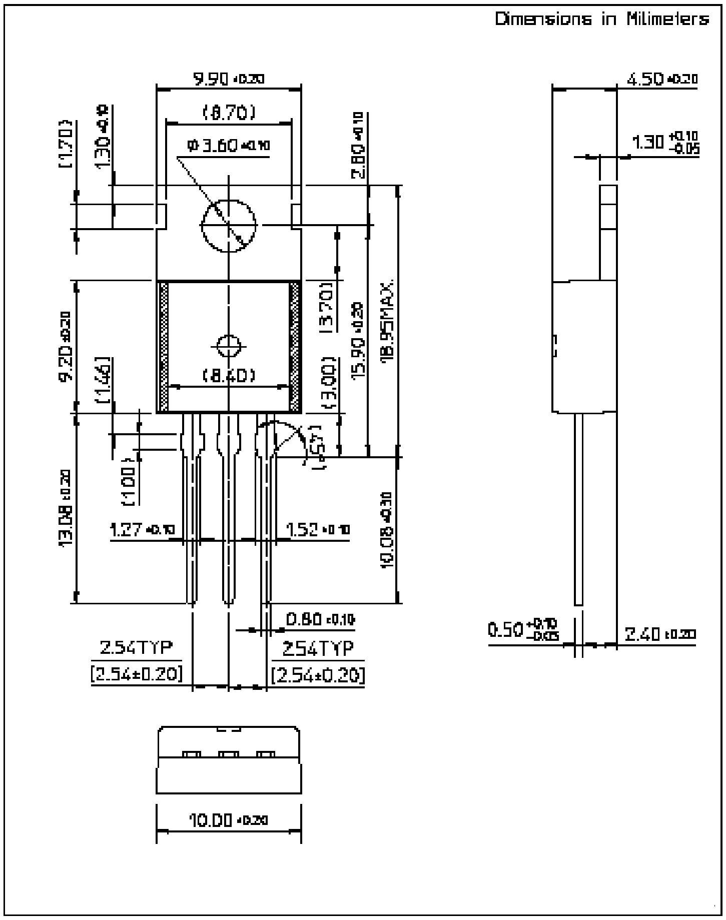
Fixed Voltage Regulator (Positive)

Ordering Information

Device	Package	Operating Temperature
MC78MXXCT (LM78XXCT) (KA78MXX)	TO-220	0 ~ + 125°C
KA78MXXI		-40 ~ +125°C
MC78MXXCDT (KA78MXXR)	D-PAK	0 ~ + 125°C
KA78MXXRI		-40 ~ + 125°C

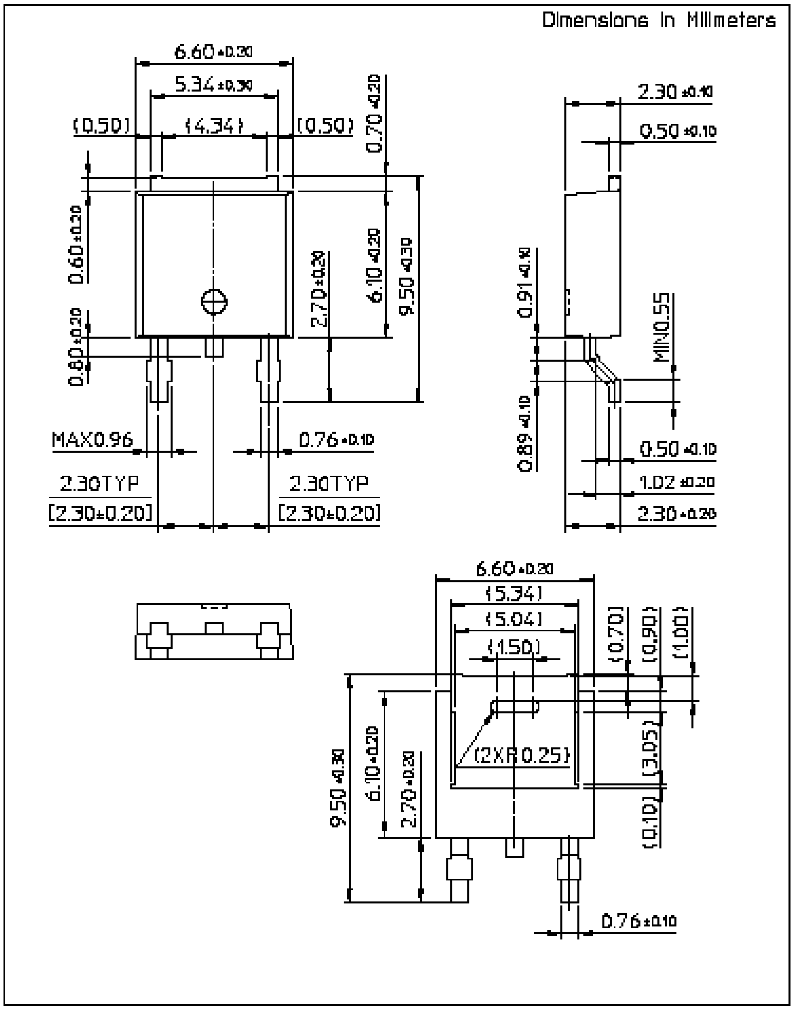
Package Dimensions

TO-220



Package Dimensions (Continued)

D-PAK



Fixed Voltage Regulator (Positive)

Fixed Voltage Regulator (Positive)

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

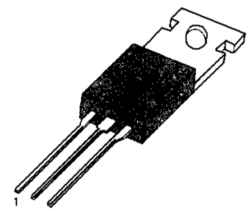
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

1/18/00 0.0m 001
Stock#DSxxxxxxxx

3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATORS

The LM78MXXC/I series of three-terminal positive regulators are available in the TO-220 package with several fixed output voltages making it useful in a wide range of applications.

TO-220



1:Input 2: GND 3: Output

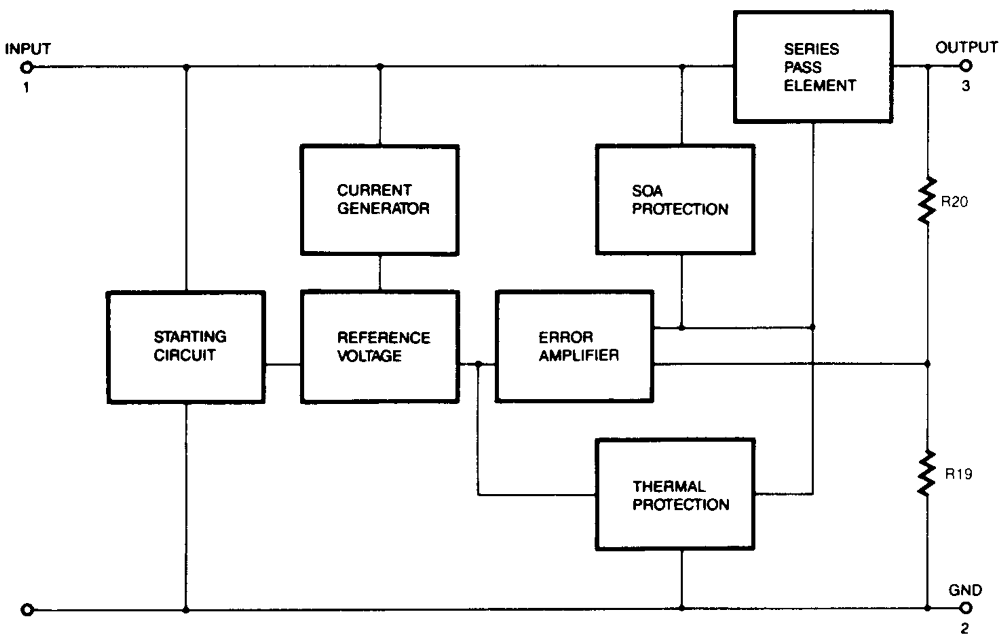
FEATURES

- Output Current up to 0.5A
- Output Voltages of 5; 6; 8; 10; 12; 15; 18; 20; 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection
- Industrial and commercial temperature range

ORDERING INFORMATION

Device	Package	Operating Temperature
LM78MXXT	TO-220	0 ~ + 125°C
LM78MXXIT	TO-220	- 40 ~ +125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V)	V_I	35	V
(for V_O = 24V)	V_I	40	V
Thermal Resistance Junction-Cases	R_{EJC}	5	°C /W
Thermal Resistance Junction-Air	R_{EJA}	65	°C /W
Operating Temperature Range KA78XXI	T_{OPR}	-40~ + 125	°C
KA78XX		0~ + 125	°C
Storage Temperature Range	T_{STG}	-65~ + 150	°C

LM78M05/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=10V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		4.8	5	5.2	V
		I_O = 5 to 350mA V_I= 7 to 20V		4.75	5	5.25	
Line Regulation	ΔV_O	I_O = 200mA	V_I= 7 to 25V			100	mV
		T_J = 25°C	V_I = 8 to 25V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				100	mV
		I_O = 5mA to 200mA, T_J = 25°C				50	
Quiescent Current	I_Q	T_J= 25°C			4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 8 to 25V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C			- 0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			40		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 8 to 18V		62			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

* T_{MIN} T_J T_{MAX}
LM78MXXI:T_{MIN}=-40°C, T_{MAX} = +125°C
LM78MXX: T_{MIN}=0°C, T_{MAX} = +125°C

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M06/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=11V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		5.75	6	6.25	V
		I_O = 5 to 350mA V_I= 8 to 21V		5.7	6	6.3	
Line Regulation	ΔV_O	I_O = 200mA	V_I= 8 to 25V			100	mV
		T_J = 25°C	V_I = 9 to 25V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				120	mV
		I_O = 5mA to 200mA, T_J = 25°C				60	
Quiescent Current	I_Q	T_J= 25°C			4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 9 to 25V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C			- 0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			45		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 9 to 19V		59			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}
LM78MXXI:T_{MIN}=-40°C
LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M08/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=14V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		7.7	8	8.3	V
		I_O = 5 to 350mA V_I= 10.5 to 23V		7.6	8	8.4	
Line Regulation	ΔV_O	I_O = 200mA T_J = 25°C	V_I= 10.5 to 25V			100	mV
			V_I = 11 to 25V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				160	mV
		I_O = 5mA to 200mA, T_J = 25°C				80	
Quiescent Current	I_Q	T_J= 25°C			4.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 10.5 to 25V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C			- 0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			52		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 9 to 19V		56			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}
LM78MXXI:T_{MIN}=-40°C
LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M10/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=17V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		9.6	10	10.4	V
		I_O = 5 to 350mA V_I= 12.5 to 25V		9.5	10	10.5	
Line Regulation	ΔV_O	I_O = 200mA	V_I= 12.5 to 25V			100	mV
		T_J = 25°C	V_I = 13 to 25V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				200	mV
		I_O = 5mA to 200mA, T_J = 25°C				100	
Quiescent Current	I_Q	T_J= 25°C			4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 12.5 to 25V				0.8	
Output Voltage Drift	$\Delta V_O / \Delta T$	I_O = 5mA T_J = 0 to 125°C			- 0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			65		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 13 to 23V		55			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}
LM78MXXI:T_{MIN}=-40°C
LM78MXX:T_{MIN}=0°C
* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M12/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=19V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		11.5	12	12.5	V
		I_O = 5 to 350mA, V_I= 14.5 to 27V		11.5	12	12.6	
Lines Regulation	ΔV_O	I_O = 200mA, T_J = 25°C	V_I= 14.5 to 30V			100	mV
			V_I = 16 to 30V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				240	mV
		I_O = 5mA to 200mA, T_J = 25°C				120	
Quiescent Current	I_Q	T_J= 25°C			4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA, V_I = 14.5 to 30V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA, T_J = 0 to 125°C			- 0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			75		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA, V_I = 15 to 25V		55			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}

LM78MXXI:T_{MIN}=-40°C

LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M15/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=23V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C	14.4	15	15.6	V
		I_O = 5 to 350mA V_I= 17.5 to 30V	14.25	15	15.75	
Line Regulation	ΔV_O	I_O = 200mA, T_J = 25°C, V_I= 17.5 to 30V			100	mV
		I_O = 200mA, T_J = 25°C, V_I = 20 to 30V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C			300	mV
		I_O = 5mA to 200mA, T_J = 25°C			150	
Quiescent Current	I_Q	T_J= 25°C		4.1	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA			0.5	mA
		I_O = 200mA V_I = 17.5 to 30V			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C		- 1		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz		100		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 18.5 to 28.5V	54			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA		2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V		300		mA
Peak Current	I_{PK}	T_J = 25°C		700		mA

*T_{MIN}

LM78MXXI:T_{MIN}=-40°C

LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M18/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=26V, unless otherwise specified, C_I = 0.33μF, C_O=0.1μF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		17.3	18	18.7	V
		I_O = 5 to 350mA V_I= 20.5 to 33V		17.1	18	18.9	
Line Regulation	ΔV_O	I_O = 200mA	V_I= 21 to 33V			100	mV
		T_J = 25°C	V_I = 24 to 33V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				360	mV
		I_O = 5mA to 200mA, T_J = 25°C				180	
Quiescent Current	I_Q	T_J= 25°C			4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 21 to 33V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C			- 1.1		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			100		μV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 22 to 32V		53			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}
LM78MXXI:T_{MIN}=-40°C
LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M20/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=29V, unless otherwise specified, C_I = 0.33μF, C_O=0.1μF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		19.2	20	20.8	V
		I_O = 5 to 350mA, V_I= 23 to 35V		19	20	21	
Line Regulation	ΔV_O	I_O = 200mA, T_J = 25°C	V_I= 23 to 35V			100	mV
			V_I = 24 to 35V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				400	mV
		I_O = 5mA to 200mA, T_J = 25°C				200	
Quiescent Current	I_Q	T_J= 25°C			4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA, V_I = 23 to 35V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA, T_J = 0 to 125°C			- 1.1		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			110		μV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA, V_I = 24 to 34V		53			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}
LM78MXXI:T_{MIN}=-40°C
LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM78M24/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T_{MIN} T_J 125°C, I_O=350mA, V_I=33V, unless otherwise specified, C_I = 0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= 25°C		23	24	25	V
		I_O = 5 to 350mA V_I= 27 to 38V		22.8	24	25.2	
Line Regulation	ΔV_O	I_O = 200mA T_J = 25°C	V_I= 27 to 38V			100	mV
			V_I = 28 to 38V			50	
Load Regulation	ΔV_O	I_O = 5mA to 0.5A, T_J = 25°C				480	mV
		I_O = 5mA to 200mA, T_J = 25°C				240	
Quiescent Current	I_Q	T_J= 25°C			4.2	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 350mA				0.5	mA
		I_O = 200mA V_I = 27 to 38V				0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	I_O = 5mA T_J = 0 to 125°C			- 1.2		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz			170		µV
Ripple Rejection	RR	f = 120Hz, I_O = 300mA V_I = 28 to 38V		50			dB
Dropout Voltage	V_D	T_J = 25°C, I_O = 500mA			2		V
Short Circuit Current	I_{SC}	T_J= 25°C, V_I= 35V			300		mA
Peak Current	I_{PK}	T_J = 25°C			700		mA

*T_{MIN}

LM78MXXI:T_{MIN}=-40°C

LM78MXX:T_{MIN}=0°C

* Load and line regulation are specified at constant, junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

APPLICATION CIRCUIT

Fig. 1 Fixed output regulator

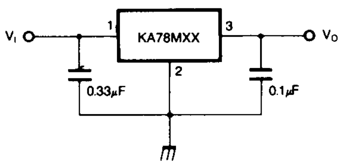
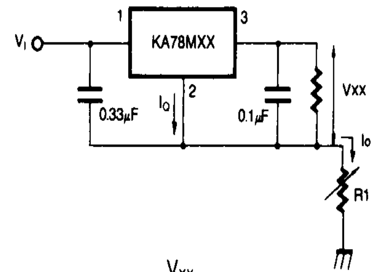


Fig. 2 Constant current regulator



$$I_O = \frac{V_{XX}}{R_1} + I_Q$$

Notes:

(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power Supply filter.

Fig. 3 Circuit for Increasing output voltage

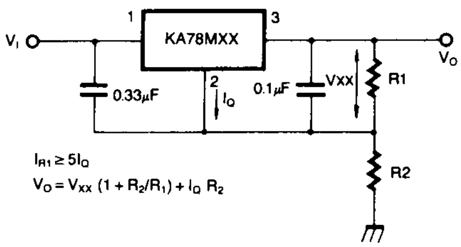


Fig. 4 Adjustable output regulator (7 to 30V)

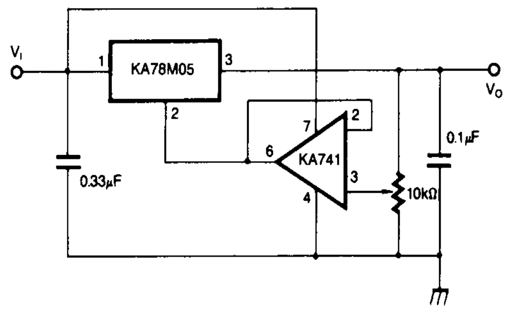
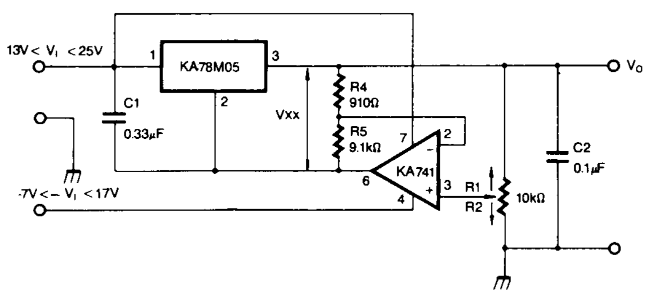


Fig. 5 0.5 to 10V Regulator



$$V_O = V_{XX} \frac{R_4}{R_1}$$

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ISOPLANAR™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

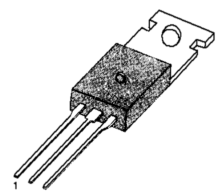
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

3-TERMINAL 1A NEGATIVE VOLTAGE REGULATORS

The LM79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.

TO-220



1: GND 2: Input 3: Output

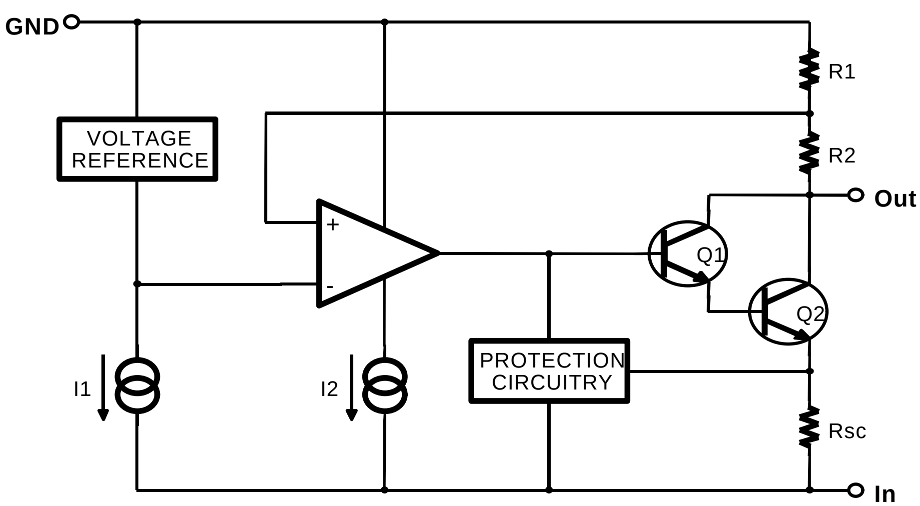
FEATURES

- Output Current in Excess of 1A
- Output Voltages of -5, -6, -8, -12, -15, -18, -24V
- Internal Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe-Area Compensation

ORDERING INFORMATION

Device	Output Voltage Tolerance	Package	Operating Temperature
LM79XXCT	± 4%	TO-220	0 ~ +125 °C
LM79XXAT	± 2%		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A=+25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage	V_I	-35	V
Thermal Resistance Junction-Cases Junction-Air	$R_{\theta JC}$ $R_{\theta JA}$	5 65	°C / W °C /W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	- 65 ~ +150	°C

LM7905 ELECTRICAL CHARACTERISTICS

(V_I = 10V, I_O = 500mA, 0°C ≤T_J ≤ +125°C, C_I =2.2μF, C_O =1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25°C		- 4.8	- 5.0	- 5.2	V
		I_O = 5mA to 1A, P_O 15W V_I = -7 to -20V		- 4.75	-5.0	- 5.25	
Line Regulation	ΔV_O	T_J =25°C	V_I = -7 to -20V I_O=1A		5	50	mV
			V_I = -8 to -12V I_O=1A		2	25	
		V_I = -7.5 to -25V			7	50	
		V_I= -8 to -12V I_O=1A			7	50	
Load Regulation	ΔV_O	I_O = 5mA to 1.5A			10	100	mV
		T_J =+25°C I_O = 250 to 750mA			3	50	
Quiescent Current	I_Q	T_J =+25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.05	0.5	mA
		V_I = -8 to -25V			0.1	0.8	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			- 0.4		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25°C			40		μV
Ripple Rejection	RR	f = 120Hz, I_O = -35V ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J=+25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J =+25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J =+25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7906 ELECTRICAL CHARACTERISTICS

(V_I = 11V, I_O = 500mA, 0°C ≤T_J≤ +125°C, C_I =2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C	- 5.75	- 6	- 6.25	V
		I_O = 5mA to 1A, P_O 15W V_I = - 9 to - 21V	- 5.7	- 6	- 6.3	
Line Regulation	ΔV_O	T_J = 25°C, V_I = - 8 to - 25V		10	120	mV
		T_J = 25°C, V_I= - 9 to -12V		5	60	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A		10	120	mV
		T_J =+ 25°C I_O = 250 to 750mA		3	60	
Quiescent Current	I_Q	T_J =+ 25°C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.5	mA
		V_I = -9 to -25V			1.3	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA		-0.5		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C		130		μV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V	54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A		2		V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I = -35V		300		mA
Peak Current	I_{PK}	T_J= +25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7908 ELECTRICAL CHARACTERISTICS

(V_I = 14V, I_O = 500mA, 0°C ≤T_J ≤ +125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C		- 7.7	- 8	- 8.3	V
		I_O = 5mA to 1A, P_O 15W V_I = -1.5 to -23V		- 7.6	- 8	- 8.4	
Line Regulation	ΔV_O	T_J = 25°C	V_I = -10.5 to -25V		10	100	mV
			V_I= -11 to -17V		5	80	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A			12	160	mV
		T_J =+ 25°C I_O = 250 to 750mA			4	80	
Quiescent Current	I_Q	T_J =+ 25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.05	0.5	mA
		V_I = -11.5 to -25V			0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			-0.6		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C			175		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J=+ 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7909 ELECTRICAL CHARACTERISTICS

(V_I = 14V, I_O = 500mA, 0°C ≤T_J ≤+ 125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C	- 8.7	- 9.0	- 9.3	V
		I_O = 5mA to 1A, P_O 15W V_I = -1.5 to -23V	- 8.6	- 9.0	- 9.4	
Line Regulation	ΔV_O	T_J = 25°C, V_I = -10.5 to -25V		10	180	mV
		T_J = 25°C, V_I= -11 to -17V		5	90	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A		12	180	mV
		T_J =+ 25°C I_O = 250 to 750mA		4	90	
Quiescent Current	I_Q	T_J =+ 25°C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		0.05	0.5	mA
		V_I = -11.5 to -25V		0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA		-0.6		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C		175		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V	54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A		2		V
Short Circuit Current	I_{SC}	T_J= +25°C, V_I = -35V		300		mA
Peak Current	I_{PK}	T_J =+25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7912 ELECTRICAL CHARACTERISTICS

(V_I= 18V, I_O =500mA, 0°C ≤T_J≤ +125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		-11.5	-12	-12.5	V
		I_O = 5mA to 1A, P_O 15W V_I = -15.5 to -27V		-11.4	-12	-12.6	
Line Regulation	ΔV_O	T_J = 25°C	V_I = -14.5 to -30V		12	240	mV
			V_I= -16 to -22V		6	120	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A			12	240	mV
		T_J =+ 25°C I_O = 250 to 750mA			4	120	
Quiescent Current	I_Q	T_J =+ 25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.05	0.5	mA
		V_I = -15 to -30V			0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			-0.8		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C			200		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J= +25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J=+ 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7915 ELECTRICAL CHARACTERISTICS

(V_I = 23V, I_O = 500mA, 0°C ≤T_J +125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C		-14.4	-15	-15.6	V
		I_O = 5mA to 1A, P_O 15W V_I = -18 to -30V		-14.25	-15	-15.75	
Line Regulation	ΔV_O	T_J = 25°C	V_I = -17.5 to -30V		12	300	mV
			V_I= -20 to -26V		6	150	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A			12	300	mV
		T_J =+ 25°C I_O = 250 to 750mA			4	150	
Quiescent Current	I_Q	T_J =+ 25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A			0.05	0.5	mA
		V_I = -18.5 to -30V			0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			-0.9		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100Khz T_A =+ 25°C			250		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J=+25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J=+ 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7918 ELECTRICAL CHARACTERISTICS

(V_I = 27V, I_O = 500mA, 0°C ≤T_J ≤+125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C		-17.3	-18	-18.7	V
		I_O = 5mA to 1A, P_O 15W V_I = -22.5 to -33V		-17.1	-18	-18.9	
Line Regulation	ΔV_O	T_J = 25°C	V_I= -21 to -33V		15	360	mV
			V_I= -24 to -30V		8	180	
Load Regulation	ΔV_O	T_J =+ 25°C I_O = 5mA to 1.5A			15	360	mV
		T_J =+ 25°C I_O = 250 to 750mA			5	180	
Quiescent Current	I_Q	T_J =+ 25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A				0.5	mA
		V_I = -22 to -33V				1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			-1		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C			300		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J=+ 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7924 ELECTRICAL CHARACTERISTICS

(V_I = 33V, I_O = 500mA, 0°C ≤T_J ≤+125°C, C_I =2.2µF, C_O = 1µF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+25°C		- 23	- 24	- 25	V
		I_O = 5mA to 1A, P_O ≤15W V_I = -27 to -38V		- 22.8	- 24	- 25.2	
Line Regulation	ΔV_O	T_J = 25°C	V_I = - 27 to - 38V		15	480	mV
			V_I= - 30 to - 36V		8	180	
Load Regulation	ΔV_O	T_J = +25°C I_O = 5mA to 1.5A			15	480	mV
		T_J =+ 25°C I_O = 250 to 750mA			5	240	
Quiescent Current	I_Q	T_J =+ 25°C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A				0.5	mA
		V_I = -27 to -38V				1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA			-1		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C			400		µV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V		54	60		dB
Dropout Voltage	V_D	T_J= +25°C I_O = 1A			2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V			300		mA
Peak Current	I_{PK}	T_J=+25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7905A ELECTRICAL CHARACTERISTICS

(V_I = 10V, I_O = 500mA, 0°C ≤ T_J ≤ +125°C, C_I = 2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C	- 4.9	- 5.0	- 5.1	V
		I_O = 5mA to 1A, P_O 15W V_I = -7 to -20V	- 4.8	-5.0	- 5.2	
Line Regulation	ΔV_O	T_J =+25°C; V_I = -7 to -20V, I_O=1A		5	50	mV
		T_J =+25°C; V_I = -8 to -12V, I_O=1A		2	25	
		V_I = -7.5 to -25V		7	50	
		V_I= -8 to -12V I_O=1A		7	50	
Load Regulation	ΔV_O	I_O = 5mA to 1.5A		10	100	mV
		T_J =+ 25°C I_O = 250 to 750mA		3	50	
Quiescent Current	I_Q	T_J = +25°C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		0.05	0.5	mA
		V_I = -8 to -25V		0.1	0.8	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA		- 0.4		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+ 25°C		40		μV
Ripple Rejection	RR	f = 120Hz, I_O = -35V ΔV_I = 10V	54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A		2		V
Short Circuit Current	I_{SC}	T_J =+ 25°C, V_I = -35V		300		mA
Peak Current	I_{PK}	T_J =+ 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7912A ELECTRICAL CHARACTERISTICS

(V_I= 18V, I_O =500mA, 0°C ≤T_J≤ +125°C, C_I =2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J =+ 25°C	-11.75	-12	-12.25	V
		I_O = 5mA to 1A, P_O 15W V_I = -15.5 to -27V	-11.5	-12	-12.5	
Line Regulation	ΔV_O	T_J =+25°C, V_I = -14.5 to -30V		12	240	mV
		T_J =+25°C, V_I= -16 to -22V		6	120	
Load Regulation	ΔV_O	T_J = +25°C I_O = 5mA to 1.5A		12	240	mV
		T_J =+ 25°C I_O = 250 to 750mA		4	120	
Quiescent Current	I_Q	T_J =+ 25°C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		0.05	0.5	mA
		V_I = -15 to -30V		0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA		-0.8		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100Khz T_A =+ 25°C		200		μV
Ripple Rejection	RR	f = 120Hz ΔV_I = 10V	54	60		dB
Dropout Voltage	V_D	T_J=+ 25°C I_O = 1A		2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V		300		mA
Peak Current	I_{PK}	T_J=+ 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM7915A ELECTRICAL CHARACTERISTICS

(V_I = 23V, I_O = 500mA, 0°C ≤T_J≤ +125°C, C_I =2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C	-14.7	-15	-15.3	V
		I_O = 5mA to 1A, P_O 15W, V_I = -18 to -30V	-14.4	-15	-15.6	
Line Regulation	ΔV_O	T_J =+25°C, V_I = -17.5 to -30V		12	300	mV
		T_J =+25°C, V_I= -20 to -26V		6	150	
Load Regulation	ΔV_O	T_J =+ 25°C, I_O = 5mA to 1.5A		12	300	mV
		T_J =+ 25°C, I_O = 250 to 750mA		4	150	
Quiescent Current	I_Q	T_J =+ 25°C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		0.05	0.5	mA
		V_I = -18.5 to -30V		0.1	1	
Temperature Coefficient of V_D	$\Delta V_O/\Delta T$	I_O = 5mA		-0.9		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A =+25°C		250		μV
Ripple Rejection	RR	f = 120Hz, ΔV_I = 10V	54	60		dB
Dropout Voltage	V_D	T_J= +25°C, I_O = 1A		2		V
Short Circuit Current	I_{SC}	T_J=+ 25°C, V_I = -35V		300		mA
Peak Current	I_{PK}	T_J=+ 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Output Voltage

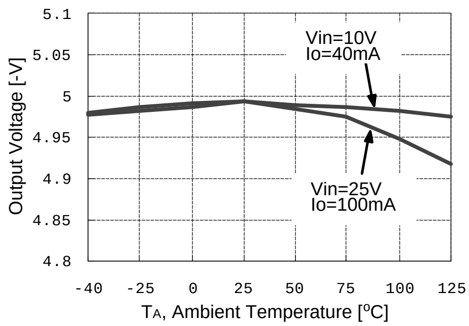


Fig. 2 Load Regulation

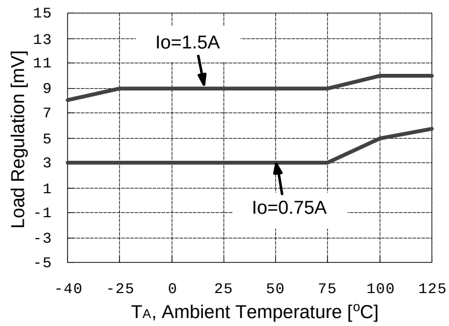


Fig.3 Quiescent Current

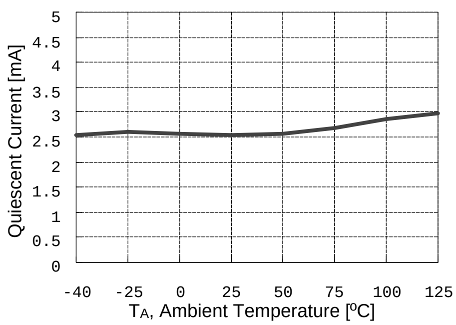


Fig. 4 Dropout Voltage

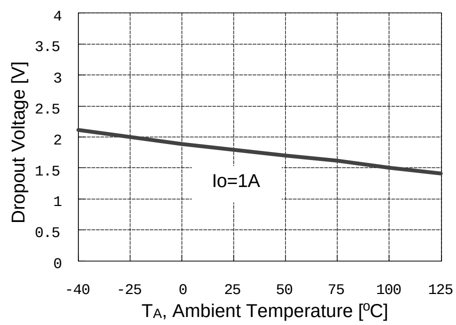
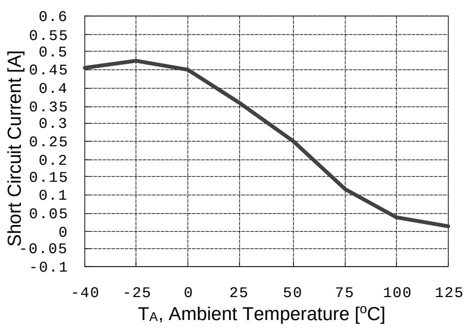
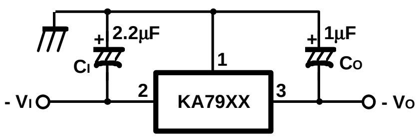


Fig.5 Short Circuit Current



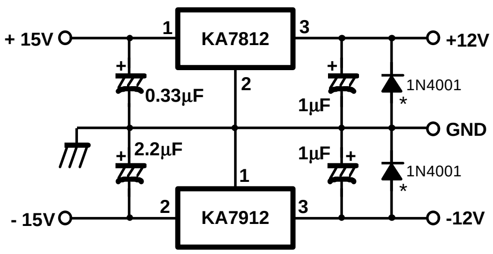
TYPICAL APPLICATIONS

Fig. 6 Negative Fixed output regulator



Notes:
(1) To specify an output voltage, substitute voltage value for “XX “
(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminum electronics are used, at least ten times value shown should be selected. C_I is required if regulator is located an appreciable distance from power supply filter.
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N400l or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 7 Split power supply (±12V/1A)



*****: Against potential latch-up problems.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

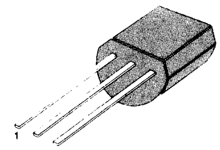
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

3-TERMINAL 0.1A NEGATIVE VOLTAGE REGULATORS

These regulators employ internal current limiting and thermal shutdown, making them essentially indestructible.

TO-92



1: GND 2: Input 3: Output

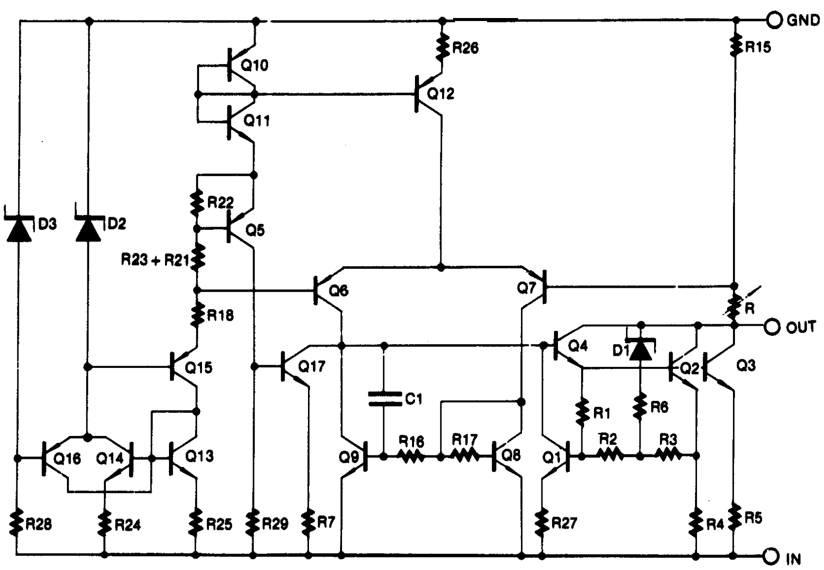
FEATURES

- Output current up to 100mA
- No external components
- Internal thermal over load protection
- Internal short circuit current limiting
- Output Voltage Offered in ± 5% Tolerance
- Output Voltage of -5V,-12V,-15V,-18V and -24V

ORDERING INFORMATION

Device	Package	Operating Temperature
MC79LXXACP (LM79LXXACZ) KA79LXXAZ	TO - 92	0 ~ + 125°C

SCHEMATIC DIAGRAM



FAIRCHILD SEMICONDUCTOR ™

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (-5V) (-12V to -18V) (-24V)	V_I	-30 -35 -40	V_{DC}
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

MC79L05A ELECTRICAL CHARACTERISTICS

(V_I = -10V, I_O = 40mA, C_I = 0.33µF, C_O = 0.1µF, 0°C ≤T_J ≤ +125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = +25°C		- 4.8	- 5.0	- 5.2	V
Line Regulation		ΔV_O	T_J =+25°C	-7.0V ≥ V_I ≥-20V		15	150	mV
				-8V ≥ V_I ≥-20V			100	
Load Regulation		ΔV_O	T_J =+25°C	1.0mA ≤ I_O ≤ 100mA		20	60	mV
				1.0mA ≤ I_O ≤ 40mA		10	30	
Output Voltage		V_O	-7.0V>V_I >-20V, 1.0mA≤ I_O ≤40mA		- 4.75		- 5.25	V
			V_I = -10V, 1.0mA≤ I_O ≤70mA		- 4.75		- 5.25	
Quiescent Current		I_Q	T_J = +25°C			2.0	6.0	mA
			T_J = +125°C				5.5	
Quiescent Current Change	With Line	ΔI_Q	-8V≥ V_I ≥-20V				1.5	mA
	With Load		1.0mA≤ I_O ≤40mA				0.1	
Output Noise Voltage		V_N	T_A = +25°C,10Hz≤f≤100KHz			30		µV
Ripple Rejection		RR	f = 120Hz, -8V≥V_I ≥-18V T_J = +25°C		41	60		dB
Dropout Voltage		V_D	T_J = +25°C			1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

MC79L12A ELECTRICAL CHARACTERISTICS

(V_I = -19V, I_O = 40mA, C_I = 0.33µF, C_O = 0.1µF, 0°C ≤T_J ≤ +125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = +25°C		-11.5	-12.0	-12.5	V
Line Regulation		ΔV_O	T_J =+25°C	-14.5V ≥V_I ≥-27V			250	mV
				-16V≥V_I ≥-27V			200	
Load Regulation		ΔV_O	T_J =+25°C	1.0mA≤ I_O ≤100mA			100	mV
				1.0mA≤ I_O ≤40mA			50	
Output Voltage		V_O	-14.5V>V_I >-27V, 1.0mA≤I_O≤40mA		-11.4		-12.6	V
			V_I = -19V, 1.0mA≤ I_O ≤70mA		-11.4		-12.6	
Quiescent Current		I_Q	T_J = +25°C				6.5	mA
			T_J = +125°C				6.0	
Quiescent Current Change	With Line	ΔI_Q	-16V≥V_I ≥-27V				1.5	mA
	With Load		1.0mA≤ I_O ≤40mA				0.1	
Output Noise Voltage		V_N	T_A = +25°C,10Hz f 100KHz			80		µV
Ripple Rejection		RR	f = 120Hz, -150V≥V_I ≥-25V T_J = +25°C		37	42		dB
Dropout Voltage		V_D	T_J = +25°C			1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

MC79L15A ELECTRICAL CHARACTERISTICS

(V_I = -23V, I_O = 40mA, C_I = 0.33µF, C_O = 0.1µF, 0°C ≤T_J ≤ +125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = +25°C		-14.4	-15.0	-15.6	V
Line Regulation		ΔV_O	T_J =+25°C	-17.5V≥V_I ≥-30V			300	mV
				-27V≥V_I ≥-30V			250	
Load Regulation		ΔV_O	T_J =+25°C	1.0mA≤ I_O ≤100mA			150	mV
				1.0mA≤ I_O ≤40mA			75	
Output Voltage		V_O	-17.5V>V_I >-30V, 1.0mA≤ I_O ≤40mA		-14.25		-15.75	V
			V_I = -23V, 1.0mA≤ I_O ≤70mA		-14.25		-15.75	
Quiescent Current		I_Q	T_J = +25°C				6.5	mA
			T_J = +125°C				6.0	
Quiescent Current Change	With Line	ΔI_Q	-20V≥V_I ≥-30V				1.5	mA
	With Load		1.0mA≤ I_O ≤40mA				0.1	
Output Noise Voltage		V_N	T_A = 25°C,10Hz≤f≤100KHz			90		µV
Ripple Rejection		RR	f = 120Hz, -18.5V≥ V_I ≥-28.5V T_J = +25°C		34	39		dB
Dropout Voltage		V_D	T_J = +25°C			1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

MC79L18A ELECTRICAL CHARACTERISTICS

(V_I = -27V, I_O = 40mA, C_I = 0.33µF, C_O = 0.1µF, 0°C ≤T_J≤ +125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J =+25°C		-17.3	-18.0	-18.7	V
Line Regulation		ΔV_O	T_J =+25°C	-20.7V≥ V_I ≥-33V			325	mV
				-21V≥ V_I ≥-33V			275	
Load Regulation		ΔV_O	T_J =+25°C	1.0mA≤ I_O ≤100mA			170	mV
				1.0mA≤ I_O ≤40mA			85	
Output Voltage		V_O	-20.7V>V_I >-33V, 1.0mA≤ I_O ≤40mA		-17.1		-18.9	V
			V_I = -1.0V, 1.0mA≤ I_O ≤70mA		-17.1		-18.9	
Quiescent Current		I_Q	T_J = +25°C				6.5	mA
			T_J = +125°C				6.0	
Quiescent Current Change	With Line	ΔI_Q	-21V≥V_I ≥-33V				1.5	mA
	With Load		1.0mA≤ I_O ≤40mA				0.1	
Output Noise Voltage		V_N	T_A =+25°C,10Hz≤f≤100KHz			150		µV
Ripple Rejection		RR	f = 120Hz, -23V≥V_I ≥-33V T_J = +25°C		33	48		dB
Dropout Voltage		V_D	T_J = +25°C			1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

MC79L24A ELECTRICAL CHARACTERISTICS

(V_I = -33V, I_O = 40mA, C_I = 0.33µF, C_O = 0.1µF, 0°C ≤T_J≤+ 125°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_J = +25°C		-23	-24	-25	V
Line Regulation		ΔV_O	T_J =+25°C	-27V≥ V_I ≥-38V			350	mV
				-28V≥ V_I ≥-38V			300	
Load Regulation		ΔV_O	T_J =+25°C	1.0mA≤ I_O ≤100mA			200	mV
				1.0mA≤ I_O ≤40mA			100	
Output Voltage		V_O	-27V>V_I >-38V, 1.0mA≤ I_O≤40mA		-22.8		-25.2	V
			V_I = -33V, 1.0mA≤ I_O ≤70mA		-22.8		-25.2	
Quiescent Current		I_Q	T_J = +25°C				6.5	mA
			T_J = +125°C				6.0	
Quiescent Current Change	With Line	ΔI_Q	-28V≥V_I ≥-38V				1.5	mA
	With Load		1.0mA≤ I_O ≤40mA				0.1	
Output Noise Voltage		V_N	T_A = +25°C,10Hz≤f≤100KHz			200		µV
Ripple Rejection		RR	f = 120Hz, -29V≥V_I ≥-35V T_J = +25°C		31	47		dB
Dropout Voltage		V_D	T_J = +25°C			1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL APPLICATIONS

Design Considerations

The MC79LXXA Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high - frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Fig. 1 Positive And Negative Regulator

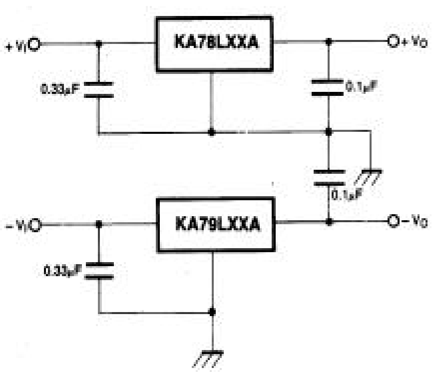
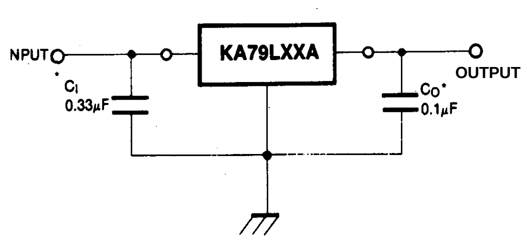


Fig. 2 Typical Application

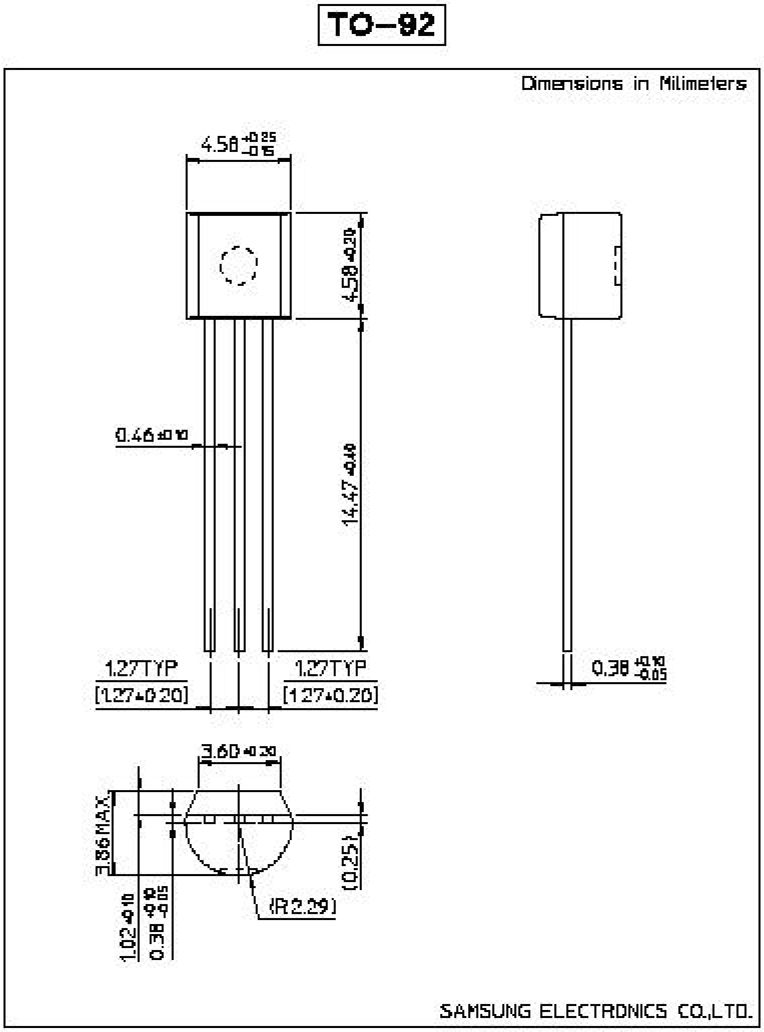


A common ground is required between the Input and the output voltages. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

= C_1 is required if regulator is located an appreciable distance from power supply filter.

* * = C_O improves stability and transient response.

PACKAGE DIMENSION



PRODUCT STATUS DEFINITIONS

Definition of Terms

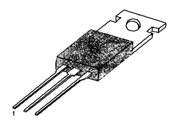
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

LM79MXX FIXED VOLTAGE REGULATOR(NEGATIVE)

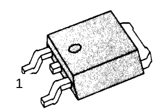
3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATORS

The LM79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially in destructible.

TO- 220



D-PAK



1: GND 2: Input 3: Output

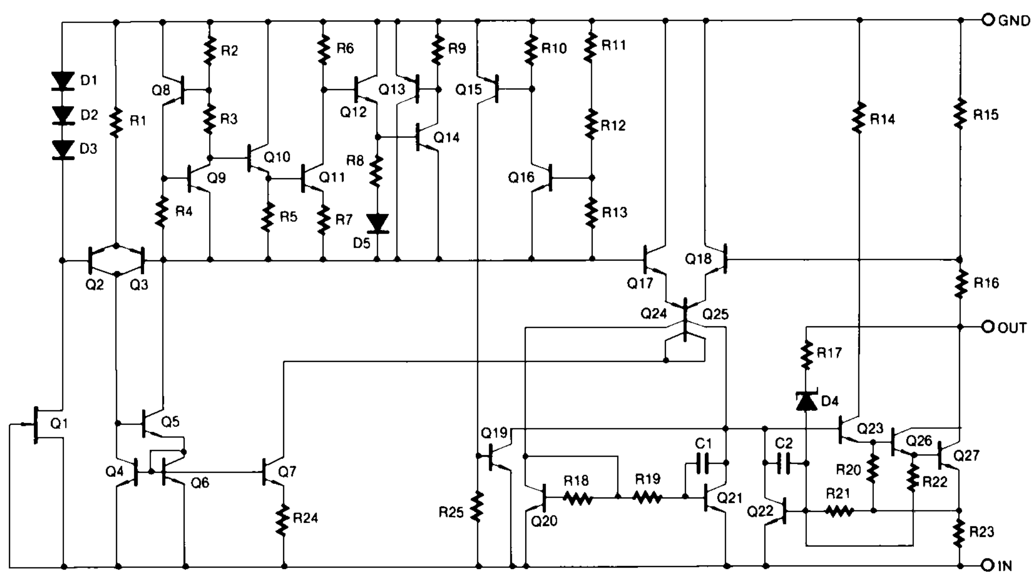
FEATURES

- No external components required
- Output current in excess of 0.5A
- Internal thermal-overload
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Output Voltages of -5V, -6V,-8V,-12V,-15V,-18V and -24V

ORDERING INFORMATION

Device	Package	Operating Temperature
LM79MXX	TO-220	0 ~ +125 °C
LM79MXXR	D-PAK	0 ~ +125 °C

SCHEMATHIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage(for V_O = -5V to -18V) (for V_O = -24V)	V_I V_I	-35 -40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C /W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C /W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	65 ~ +125	°C

LM79MO5/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J ≤ +125 °C, I_O =350mA, V_I =10V,unless otherwise specified, C_I =0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test condition		MIN	TYP	MAX	Unit
Output Voltage	V_O	T_J= +25 °C		-4.8	-5	-5.2	V
		I_O = 5 to 350mA V_I = -7 to -25V		-4.75	-5	-5.25	
Line Regulation	ΔV_O	T_J= +25°C	V_I= -7 to -25V		7.0	50	mV
			V_I= -8 to -25V		2.0	30	
Load Regulation	ΔV_O	I_O = 5mA to 500mA T_J = 25 °C			30	100	mV
Quiescent Current	I_Q	T_J= 25 °C			3.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		I_O = 200mA V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.2		mV/ °C
Output Noise Voltage	V_N	f = 10Hz, 100Khz T_J = +25 °C			40		µV
Ripple Rejection	RR	f = 120Hz V_I = -8 to -18V		54	60		dB
Dropout Voltage	V_D	T_J =+25 °C, I_O = 500mA			1.1		V
Short Circuit Current	I_{SC}	T_J= +25 °C, V_I = -35V			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79MO6/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J≤ +125 °C, I_O =350mA, V_I = -11V,unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 5.75	- 6.0	- 6.25	V
		I_O = 5 to 350mA V_I = -8.0 to -25V		- 5.7	- 6.0	- 6.3	
Line Regulation	ΔV_O	T_J= +25 °C	V_I = -8 to -25V		7.0	60	mV
			V_I = -9 to -19V		2.0	40	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	120	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			0.4		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			50		µV
Ripple Rejection	RR	f = 120Hz,V_I = -9 to -19V		54	60		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79MO8/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J≤ +125 °C, I_O =350mA, V_I = -14V,unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 7.7	- 8.0	- 8.3	V
		I_O = 5 to 350mA V_I = -10.5 to -25V		- 7.6	- 8.0	- 8.4	
Line Regulation	ΔV_O	T_J= +25 °C	V_I = -10.5 to -25V		7.0	80	mV
			V_I = -11 to -21V		2.0	50	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	160	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.6		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			60		µV
Ripple Rejection	RR	f = 120Hz,V_I = -9 to -19V		54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J = +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M12/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = - 19V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C	-11.5	-12	-12.5	V
		I_O = 5 to 350mA, V_I = -14.5 to -30V	-11.4	-1.2	-12.6	
Line Regulation	ΔV_O	T_J = +25 °C, V_I = -14.5 to -30V		8.0	80	mV
		T_J = +25 °C, V_I = -15 to -25V		3.0	50	
Load Regulation	ΔV_O	T_J= +25°C, I_O = 5.0mA to 500mA		30	240	mV
Quiescent Current	I_Q	T_J= +25 °C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA			0.4	mA
		V_I = -14.5V to -30V			0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A =+25 °C		75		µV
Ripple Rejection	RR	f = 120Hz,V_I = -15 to -25V	54	60		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C		1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C		140		mA
Peak Current	I_{PK}	T_J= +25 °C		650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M15/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = - 23V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C	- 14.4	- 15	- 15.6	V
		I_O = 5 to 350mA, V_I = -17.5 to -30V	- 14.25	- 15	- 15.75	
Line Regulation	ΔV_O	T_J = +25 °C, V_I = -17.5 to -30V		9.0	80	mV
		T_J = +25 °C, V_I = -18 to -28V		5.0	50	
Load Regulation	ΔV_O	T_J= +25°C, I_O = 5.0mA to 500mA		30	240	mV
Quiescent Current	I_Q	T_J= +25 °C		3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA			0.4	mA
		V_I = -17.5V to -28V			0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA		-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C		90		µV
Ripple Rejection	RR	f = 120Hz,V_I = -18.5 to -28.5V	54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C		1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C		140		mA
Peak Current	I_{PK}	T_J= +25 °C		650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M18/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = - 27V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 17.3	- 18	- 18.7	V
		I_O = 5 to 350mA V_I = -21 to -33V		- 17.1	- 18	- 18.9	
Line Regulation	ΔV_O	T_J =+ 25 °C	V_I = -21 to -33V		9.0	80	mV
			V_I = -24 to -30V		5.0	80	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	360	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -21V to -33V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			110		µV
Ripple Rejection	RR	f = 120Hz,V_I = -22 to -32V		54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M24/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = - 33V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 23	- 24	- 25	V
		I_O = 5 to 350mA V_I = -27 to -38V		- 22.8	- 24	- 25.2	
Line Regulation	ΔV_O	T_J = +25 °C	V_I = -27 to -38V		9.0	80	mV
			V_I = -30 to -36V		5.0	70	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	300	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -27V to -38V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			180		µV
Ripple Rejection	RR	f = 120Hz,V_I = -28 to -38V		54	58		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL APPLICATIONS

Bypass capacitors are recommended for stable operation of the KA79MXX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.
The bypass capacitors, (2µF on the input, 1µF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electronics are used, their values should be 10µF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fig. 1 Fixed Output Regulator

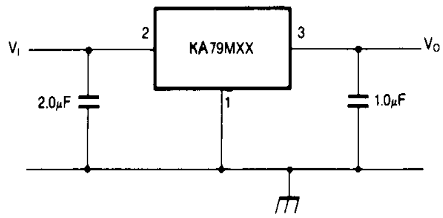
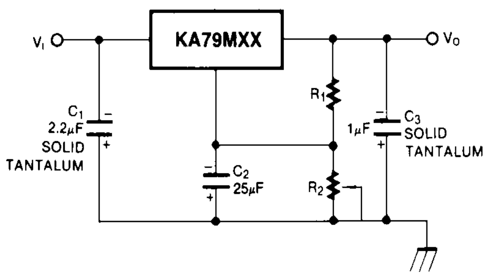


Fig. 2 Variable Output



Note

1. Required for stability. For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted.
2. C_2 improves transient response and ripple rejection. Do not increase beyond 50µF.

$$V_{OUT} = V_{SET}\left(\frac{R_1 + R_2}{R_1}\right)$$

Select R_2 as follows

KA79M 05: 300Ω, KA79M12: 750Ω, KA79M15: 11Ω

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

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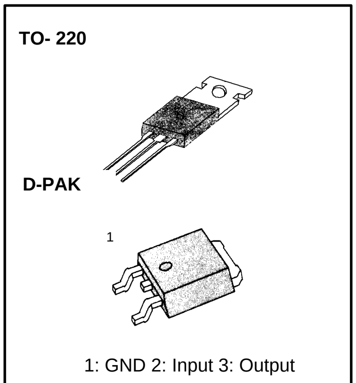
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATORS

The KA79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially in destructible.



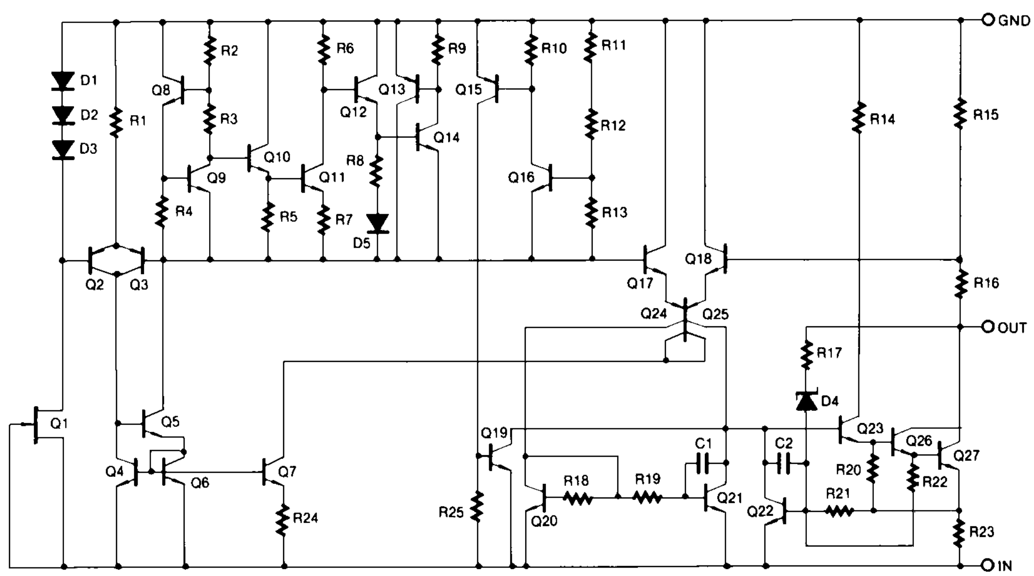
FEATURES

- No external components required
- Output current in excess of 0.5A
- Internal thermal-overload
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Output Voltages of -5V, -6V,-8V,-12V,-15V,-18V and -24V

ORDERING INFORMATION

Device	Package	Operating Temperature
KA79MXX	TO-220	0 ~ +125 °C
KA79MXXR	D-PAK	0 ~ +125 °C

SCHEMATHIC DIAGRAM



Rev. C

FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage(for V_O = -5V to -18V) (for V_O = -24V)	V_I V_I	-35 -40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C /W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C /W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	65 ~ +125	°C

LM79MO5/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J ≤ +125 °C, I_O =350mA, V_I =10V,unless otherwise specified, C_I =0.33µF, C_O=0.1µF)

Characteristic	Symbol	Test condition		MIN	TYP	MAX	Unit
Output Voltage	V_O	T_J= +25 °C		-4.8	-5	-5.2	V
		I_O = 5 to 350mA V_I = -7 to -25V		-4.75	-5	-5.25	
Line Regulation	ΔV_O	T_J= +25°C	V_I= -7 to -25V		7.0	50	mV
			V_I= -8 to -25V		2.0	30	
Load Regulation	ΔV_O	I_O = 5mA to 500mA T_J = 25 °C			30	100	mV
Quiescent Current	I_Q	T_J= 25 °C			3.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		I_O = 200mA V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.2		mV/ °C
Output Noise Voltage	V_N	f = 10Hz, 100Khz T_J = +25 °C			40		µV
Ripple Rejection	RR	f = 120Hz V_I = -8 to -18V		54	60		dB
Dropout Voltage	V_D	T_J =+25 °C, I_O = 500mA			1.1		V
Short Circuit Current	I_{SC}	T_J= +25 °C, V_I = -35V			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79MO6/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = -11V,unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 5.75	- 6.0	- 6.25	V
		I_O = 5 to 350mA V_I = -8.0 to -25V		- 5.7	- 6.0	- 6.3	
Line Regulation	ΔV_O	T_J= +25 °C	V_I = -8 to -25V		7.0	60	mV
			V_I = -9 to -19V		2.0	40	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	120	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			0.4		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			50		µV
Ripple Rejection	RR	f = 120Hz,V_I = -9 to -19V		54	60		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79MO8/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤ T_J ≤ +125 °C, I_O =350mA, V_I = -14V,unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 7.7	- 8.0	- 8.3	V
		I_O = 5 to 350mA V_I = -10.5 to -25V		- 7.6	- 8.0	- 8.4	
Line Regulation	ΔV_O	T_J= +25 °C	V_I = -10.5 to -25V		7.0	80	mV
			V_I = -11 to -21V		2.0	50	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	160	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -8V to -25V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.6		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			60		µV
Ripple Rejection	RR	f = 120Hz,V_I = -9 to -19V		54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J = +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M12/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J≤ +125 °C, I_O =350mA, V_I = - 19V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		-11.5	-12	-12.5	V
		I_O = 5 to 350mA V_I = -14.5 to -30V		-11.4	-1.2	-12.6	
Line Regulation	ΔV_O	T_J = +25 °C	V_I = -14.5 to -30V		8.0	80	mV
			V_I = -15 to -25V		3.0	50	
Load Regulation	ΔV_O	T_J= +25°C	I_O = 5.0mA to 500mA		30	240	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -14.5V to -30V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-0.8		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A =+25 °C			75		µV
Ripple Rejection	RR	f = 120Hz,V_I = -15 to -25V		54	60		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M15/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J≤ +125 °C, I_O =350mA, V_I = - 23V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 14.4	- 15	- 15.6	V
		I_O = 5 to 350mA V_I = -17.5 to -30V		- 14.25	- 15	- 15.75	
Line Regulation	ΔV_O	T_J = +25 °C	V_I = -17.5 to -30V		9.0	80	mV
			V_I = -18 to -28V		5.0	50	
Load Regulation	ΔV_O	T_J= +25°C	I_O = 5.0mA to 500mA		30	240	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -17.5V to -28V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			90		µV
Ripple Rejection	RR	f = 120Hz,V_I = -18.5 to -28.5V		54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M18/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J ≤ +125 °C, I_O =350mA, V_I = - 27V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 17.3	- 18	- 18.7	V
		I_O = 5 to 350mA, V_I = -21 to -33V		- 17.1	- 18	- 18.9	
Line Regulation	ΔV_O	T_J =+ 25 °C	V_I = -21 to -33V		9.0	80	mV
			V_I = -24 to -30V		5.0	80	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	360	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -21V to -33V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			110		μV
Ripple Rejection	RR	f = 120Hz,V_I = -22 to -32V		54	59		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

LM79M24/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T_J ≤ +125 °C, I_O =350mA, V_I = - 33V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Typ	Max	Unit
Output Voltage	V_O	T_J= +25 °C		- 23	- 24	- 25	V
		I_O = 5 to 350mA, V_I = -27 to -38V		- 22.8	- 24	- 25.2	
Line Regulation	ΔV_O	T_J = +25 °C	V_I = -27 to -38V		9.0	80	mV
			V_I = -30 to -36V		5.0	70	
Load Regulation	ΔV_O	T_J= +25 °C	I_O = 5.0mA to 500mA		30	300	mV
Quiescent Current	I_Q	T_J= +25 °C			3	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5 to 350mA				0.4	mA
		V_I = -27V to -38V				0.4	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O = 5mA			-1.0		mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz,T_A = +25 °C			180		μV
Ripple Rejection	RR	f = 120Hz,V_I = -28 to -38V		54	58		dB
Dropout Voltage	V_D	I_O = 500mA, T_J = +25 °C			1.1		V
Short Circuit Current	I_{SC}	V_I = -35V, T_J = +25 °C			140		mA
Peak Current	I_{PK}	T_J= +25 °C			650		mA

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL APPLICATIONS

Bypass capacitors are recommended for stable operation of the KA79MXX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.
The bypass capacitors, (2µF on the input, 1µF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electronics are used, their values should be 10µF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fig. 1 Fixed Output Regulator

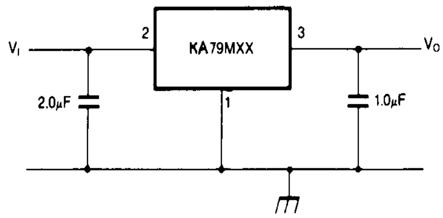
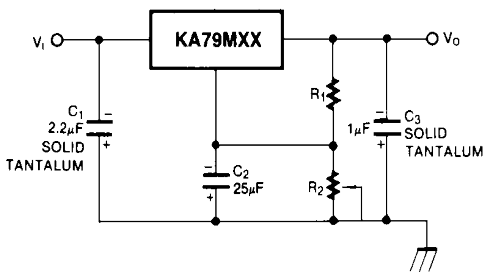


Fig. 2 Variable Output



Note
1. Required for stability. For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted.
2. C_2 improves transient response and ripple rejection. Do not increase beyond 50µF.

$$V_{OUT} = V_{SET}\left(\frac{R_1 + R_2}{R_1}\right)$$

Select R_2 as follows

KA79M 05: 300Ω, KA79M12: 750Ω, KA79M15: 11Ω

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