NEC

PRELIMINARY DATA SHEET

MOS INTEGRATED CIRCUIT

μPD4516421,4516821,4516161

16M bit Synchronous DRAM

Description

The uPD4516421, uPD4516821, uPD 4516161 are high-speed 16 777 216-bit synchronous dynamic random-access memories, each organized as 2 097 152-word x 4-bit x 2 banks,1 048 576-word x 8-bit x 2 banks and 524 288-word x16-bit x 2 banks.

The synchronous DRAMs acheive high-speed data transfer using the pipeline architecture.

All inputs and outputs are syncronized with the positive edge of clock.

The synchronous DRAMs conpatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are available in 400-mil ,44-pin TSOP II (x4,x8) and 400-mil, 50-pin TSOP II(x16).

Features

- Fully Synchronous Dynamic RAM,with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual Internal Banks controlled by A11 (Bank Select)
- Programmable burst-length (1,2,4,8 Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable $\overline{CAS}$ latency (1, 2, 3)
- Automatic precharge and controlled Precharge
- CBR(Auto) refresh and self refresh
- x4, x8, x16 organization
- Single +3.3 ± 0.3V power supply
- LVTTL compatible
- Byte control (x16) by LDQM and UDQM
- 2048 refresh cycles / 32ms
- Burst termination by Burst Stop command and Precharge command

The information in this document is subject to change without notice. Ver.4.0

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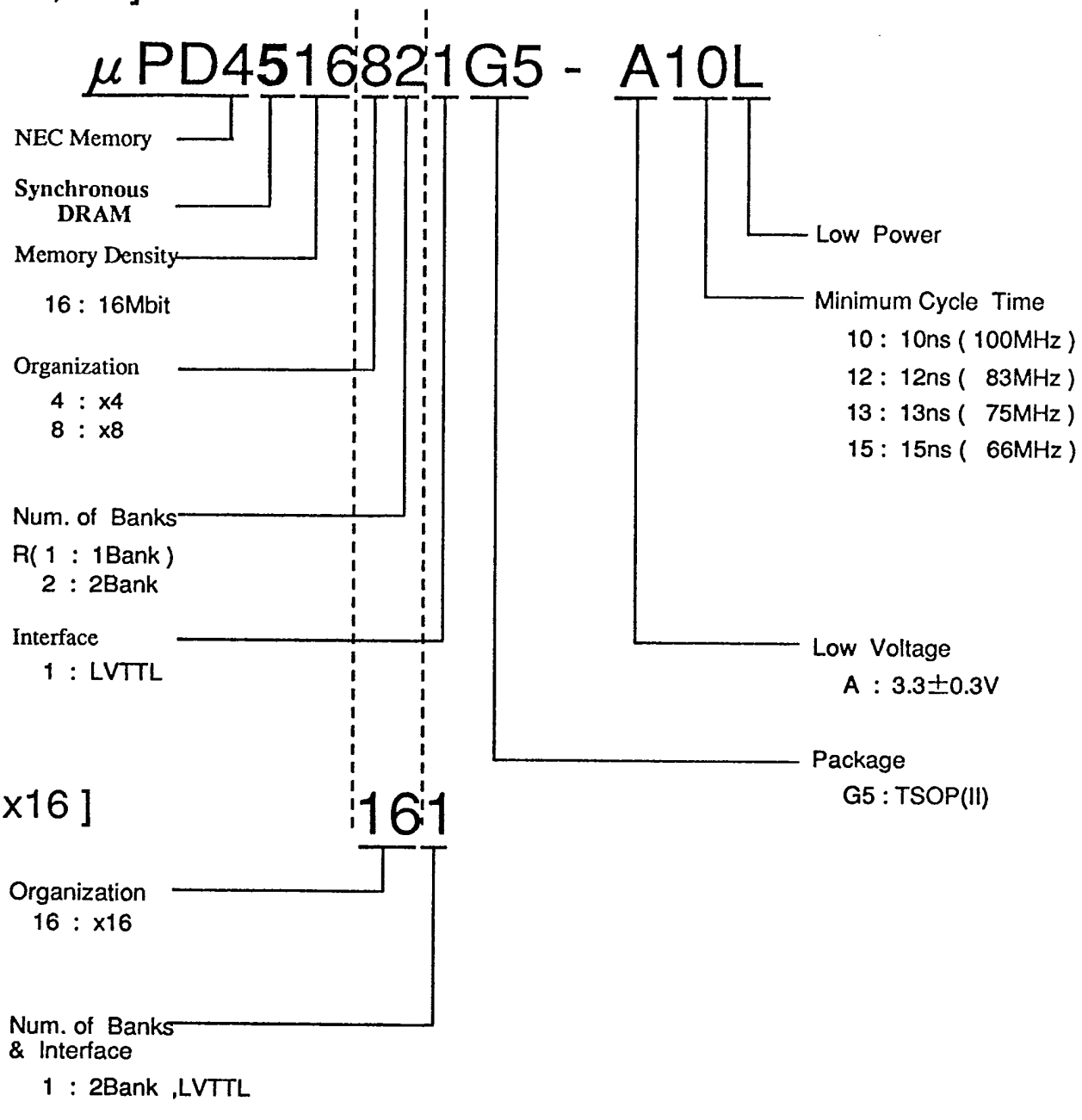
Ordering information

Part number	Organization (word x bit x bank)	MAX. Clock Frequency	Package
uPD4516421G5-A10-7JF	2M x 4 x 2	100MHz	44-pin Plastic TSOP(II) (400mil)
uPD4516421G5-A12-7JF		83MHz	
uPD4516421G5-A13-7JF		75MHz	
uPD4516421G5-A15-7JF		66MHz	
uPD4516821G5-A10-7JF	1M x 8 x 2	100MHz	44-pin Plastic TSOP(II) (400mil)
uPD4516821G5-A12-7JF		83MHz	
uPD4516821G5-A13-7JF		75MHz	
uPD4516821G5-A15-7JF		66MHz	
uPD4516161G5-A10-7JF	512K x 16 x 2	100MHz	50-pin Plastic TSOP(II) (400mil)
uPD4516161G5-A12-7JF		83MHz	
uPD4516161G5-A13-7JF		75MHz	
uPD4516161G5-A15-7JF		66MHz	

Part Numbers

[x4, x8]



[x16]

R:Reserved

Symbol	Function
CLK(input pin)	CLK is the master clock input . Other inputs signals are referenced to the CLK rising edge .
$\overline{CS}$(input pin)	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$(input pins)	$\overline{RAS}$ $\overline{CAS}$ and $\overline{WE}$ have the same symbols on conventional DRAMs but different functions. For details, refer to the command table.
A0 - A11(input pins)	Row Address is determined by A0 - A10 at the CLK(clock) rising edge in the activate command cycle. And it does not depend on the bit organization. Column Address is determined by A0 - A9 at the CLK rising edge in the read or write command cycle. It depend on the bit organi- zation. A0 - A9 for X4 device, A0 - A8 for X8 devices and A0 - A7 for X16 devices. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precherged ; when A10 is low, only the bank selected by A11 is precharged. When A10 high in read or write command cycle, the precharge start automatically after the burst access.
A11(input pin)	A11 is the bank select signal(BS). In command cycle, A11 low selects bank A and A11 High selects bank B.
CKE(input pin)	CKE determine validity of the next CLK(clock). If CKE is high ,the next CLK rising edge is valid ; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the µPD4516XXX suspends operation. When the µPD4516XXX is not in burst mode and CKE is negated, the device enter power-down made,during power down mode CKE must remain low.
DQM , DQMU , DQML (input pin)	DQM controls I/O buffers .In X16 products ,DQMU and DQML control upper byte and lower byte I/O buffers,respectively. In read mode, DQM control the output buffers the same as a conventional $\overline{OE}$ pin. Respectively , DQM high and DQM low turn the output buffers off and on. The DQM latency for the read is two clocks. In write mode,DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
I/O0 - I/O15 (input/output pins)	I/O pins have the same function as I/O pins on a conventional DRAM.
Vcc, Vss, VccQ, VssQ (power supply)	Vcc and Vss are power supply pins for internal circuits.VccQ and VssQ are power supply pins for the output buffers.

PIN OUT (4Mx4)

LVTTL

Vcc	1	44	Vss
NC	2	43	NC
VssQ	3	42	VssQ
DQ0	4	41	DQ3
VccQ	5	40	VccQ
NC	6	39	NC
VssQ	7	38	VssQ
DQ1	8	37	DQ2
VccQ	9	36	VccQ
NC	10	35	NC
NC	11	34	NC
$\overline{WE}$	12	33	DQM
$\overline{CAS}$	13	32	CLK
$\overline{RAS}$	14	31	CKE
$\overline{CS}$	15	30	NC
A11	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

400mil 44Pin 0.8mmTSOP(II)

Pin Identification

Name	Function
A0 to A11	Address Inputs
(A0 to A11	Row Address Inputs)
(A0 to A9, A11	Column Address Inputs)
DQ0 to DQ3	Data Inputs/Outputs
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col Address Strobe

Name	Function
$\overline{WE}$	Write Enable
DQM	DQ Mask Enable
Vcc	Supply Voltage
Vss	Ground
VccQ	Supply Voltage for DQ
VssQ	Ground for DQ
NC	No connection

PIN OUT (2Mx8)

LVTTL

Vcc	1	44	Vss
DQ0	2	43	DQ7
VssQ	3	42	VssQ
DQ1	4	41	DQ6
VccQ	5	40	VccQ
DQ2	6	39	DQ5
VssQ	7	38	VssQ
DQ3	8	37	DQ4
VccQ	9	36	VccQ
NC	10	35	NC
NC	11	34	NC
$\overline{WE}$	12	33	DQM
$\overline{CAS}$	13	32	CLK
$\overline{RAS}$	14	31	CKE
$\overline{CS}$	15	30	NC
A11	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

400mil 44Pin 0.8mmTSOP(II)

Pin Identification

Name	Function
A0 to A11	Address Inputs
(A0 to A11	Row Address Inputs)
(A0 to A8, A11	Column Address Inputs)
DQ0 to DQ7	Data Inputs/Outputs
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col Address Strobe

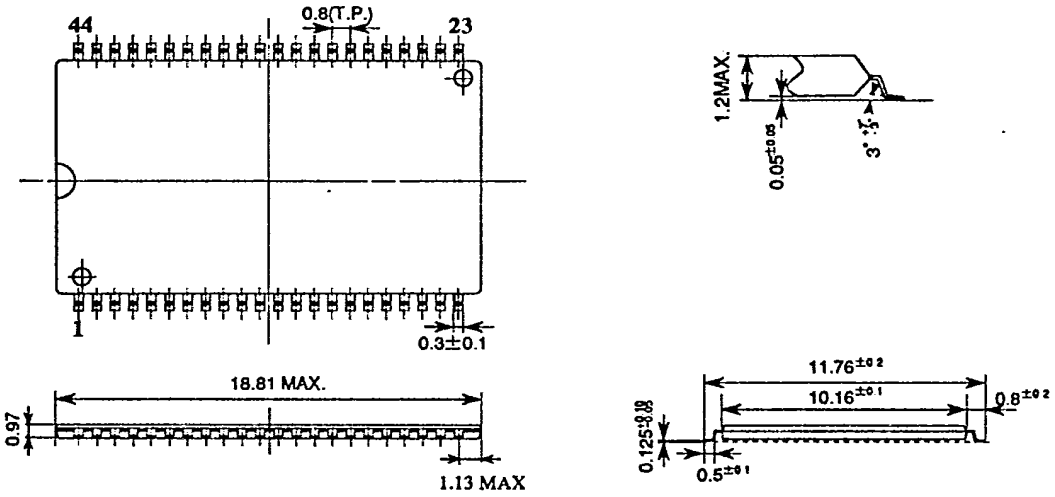
Name	Function
$\overline{WE}$	Write Enable
DQM	DQ Mask Enable
Vcc	Supply Voltage
Vss	Ground
VccQ	Supply Voltage for DQ
VssQ	Ground for DQ
NC	No connection

PIN CONFIGURATION

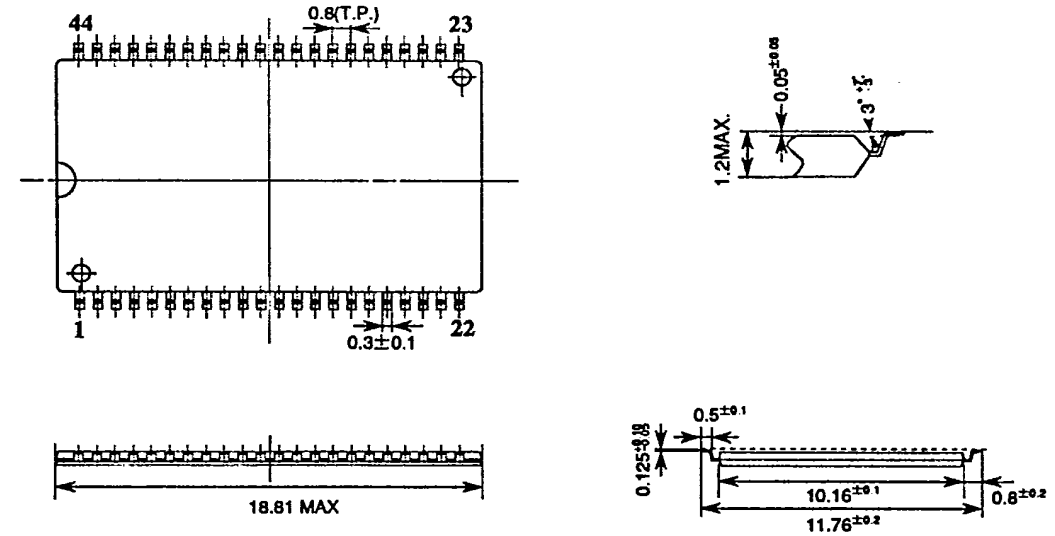
X4/X8/X9/

44pin 400mil TSOP (TypeII) (unit : mm)

Normal Bend



Reverse Bend



PIN OUT (1Mx16)

LVTTL

Vcc	1	50	Vss
DQ0	2	49	DQ15
DQ1	3	48	DQ14
VssQ	4	47	VssQ
DQ2	5	46	DQ13
DQ3	6	45	DQ12
VccQ	7	44	VccQ
DQ4	8	43	DQ11
DQ5	9	42	DQ10
VssQ	10	41	VssQ
DQ6	11	40	DQ9
DQ7	12	39	DQ8
VccQ	13	38	VccQ
LDQM	14	37	NC
$\overline{WE}$	15	36	UDQM
$\overline{CAS}$	16	35	CLK
$\overline{RAS}$	17	34	CKE
$\overline{CS}$	18	33	NC
A11	19	32	A9
A10	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	Vss

400mil 50Pin 0.8mmTSOP(II)

Pin Identification

Name	Function
A0 to A11	Address Inputs
(A0 to A11	Row Address Inputs)
(A0 to A7, A11	Column Address Inputs)
DQ0 to DQ15	Data Inputs/Outputs
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col Address Strobe

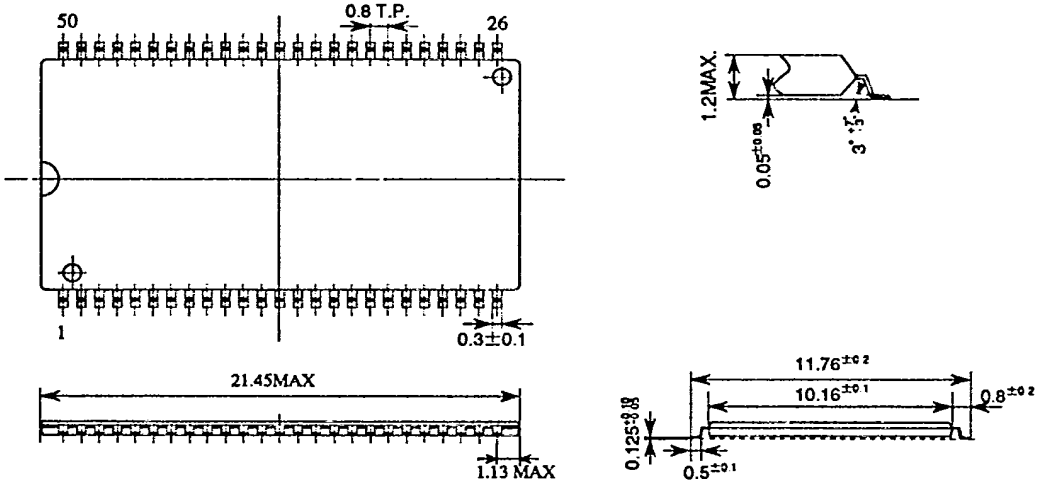
Name	Function
$\overline{WE}$	Write Enable
LDQM, UDQM	DQ Mask Enable
Vcc	Supply Voltage
Vss	Ground
VccQ	Supply Voltage for DQ
VssQ	Ground for DQ
NC	No connection

PIN CONFIGURATION

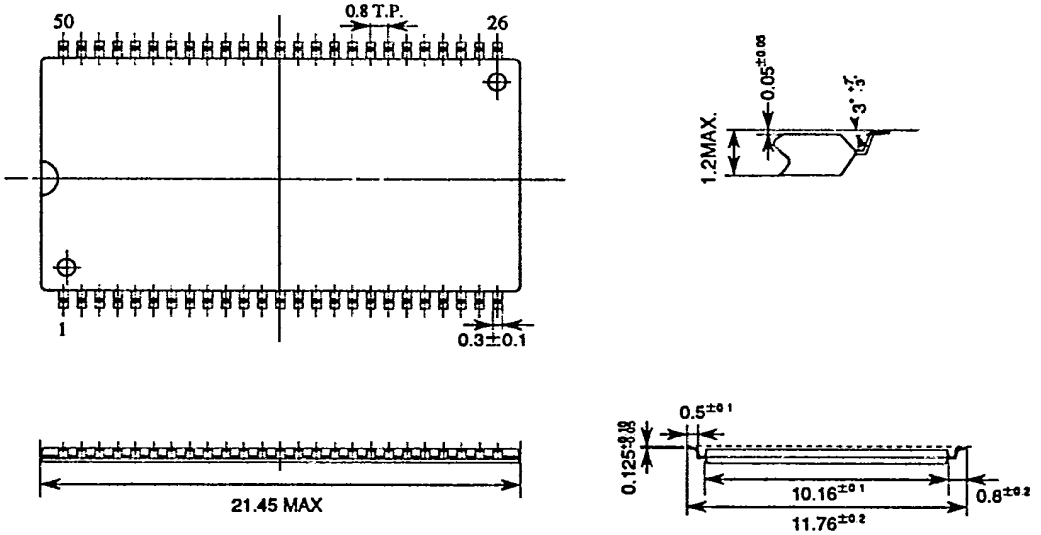
X16/X18

50pin 400mil TSOP (TypeII) (unit : mm)

Normal Bend



Reverse Bend



Commands

Mode register set command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low)

µPD4516XXX has a mode register that define how the device operates. In this command,A0 - A11 are the data input pins. After power-on,the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During the two cycles following this command, µPD4516XXX cannot accept any other commands.

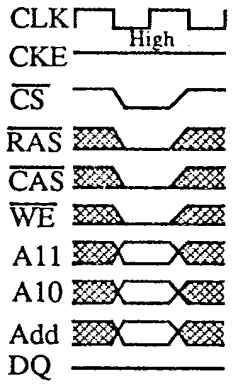


Fig.1 Mode register set command

Row activate command

($\overline{CS}$, $\overline{RAS}$ = Low, $\overline{CAS}$, $\overline{WE}$ = High)

µPD4516XXX has two banks, each with 2048 rows .
This command activates the bank selected by A11(BS) and a row address selected by A0 - A10 .

The command corresponds to a conventional DRAM's falling $\overline{RAS}$ signal.

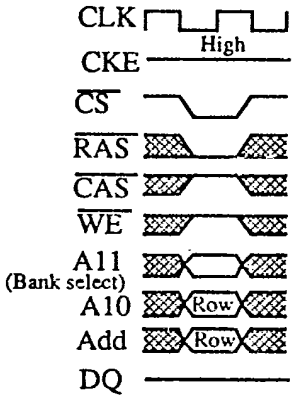


Fig.2 Row address strobe and bank active command

Precharge command

($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low, $\overline{CAS}$ = High)

This command begins precharge operation of the bank selected by A11(BS) and A10. When A10 is High , both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, µPD4516XXX can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period) .

The command corresponds to a conventional DRAM's rising $\overline{RAS}$ signal.

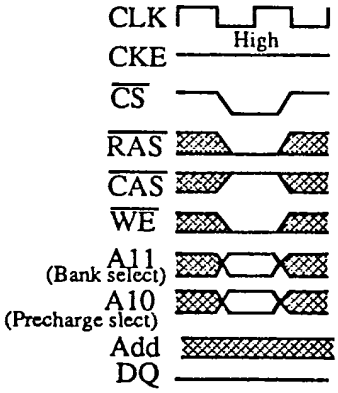


Fig.3 Precharge command

Column Address and Write command

($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low, $\overline{RAS}$ = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data must be input with this write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

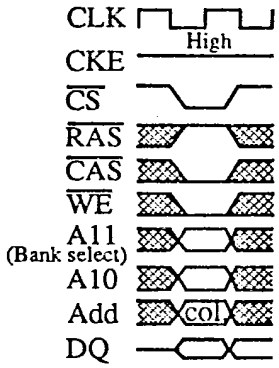


Fig.4 Column Address and Write command

Column address and Read command

($\overline{CS}$, $\overline{CAS}$ = Low, $\overline{RAS}$, $\overline{WE}$ = High)

This command sets the burst start address given by the column address.

Read data is available after $\overline{CAS}$ Latency requirements have been met .

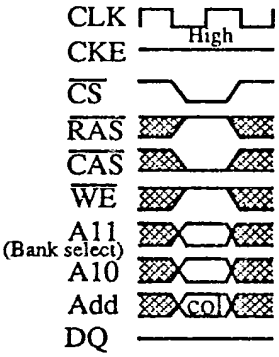


Fig.5 Column address and Read command

CBR (Auto) refresh command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low, $\overline{WE}$, CKE = High)

This command is a request to begin the CBR refresh operation. The refresh address and the bank select address are generated internally.

Before executing CBR refresh, both banks must be precharged.

After this cycle , both banks will be in the idle (precharge) state and ready for a row activate command.

During t_{RC} period (from refresh command to refresh or activate command) , μPD4516XXX cannot accept any other command.

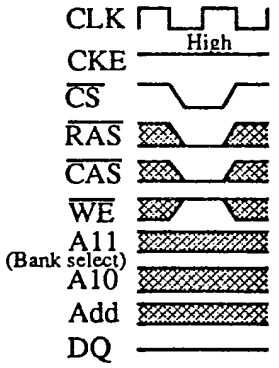


Fig.6 Auto refresh command

Self - refresh Entry command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$,CKE = Low, $\overline{WE}$ = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high , the μPD4516XXX exits the self-refresh mode.

During self- refresh mode , refresh interval and refresh operation are preformed internally, so there is no need for external control. Before executing self - refresh , both banks must be precharged.

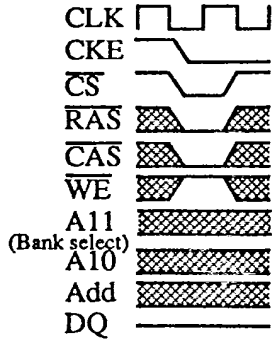


Fig.7 Self refresh Entry command

Burst stop command

($\overline{CS}$, $\overline{WE}$ = Low, $\overline{RAS}$, $\overline{CAS}$ = High)

This command terminates the current burst operation .

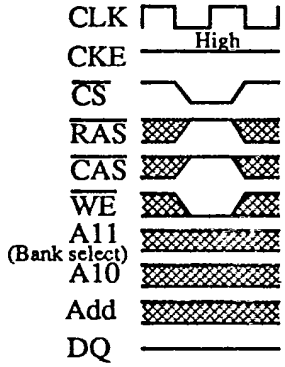


Fig.8 Burst stop command in Full Page mode

No Operation

($\overline{CS}$ = Low, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High)

This command is not a execution command. No operations begin or terminate by this command.

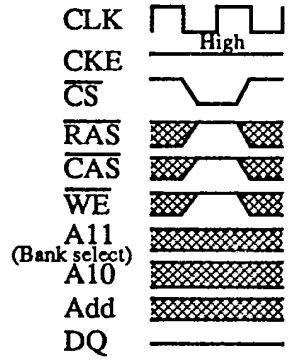
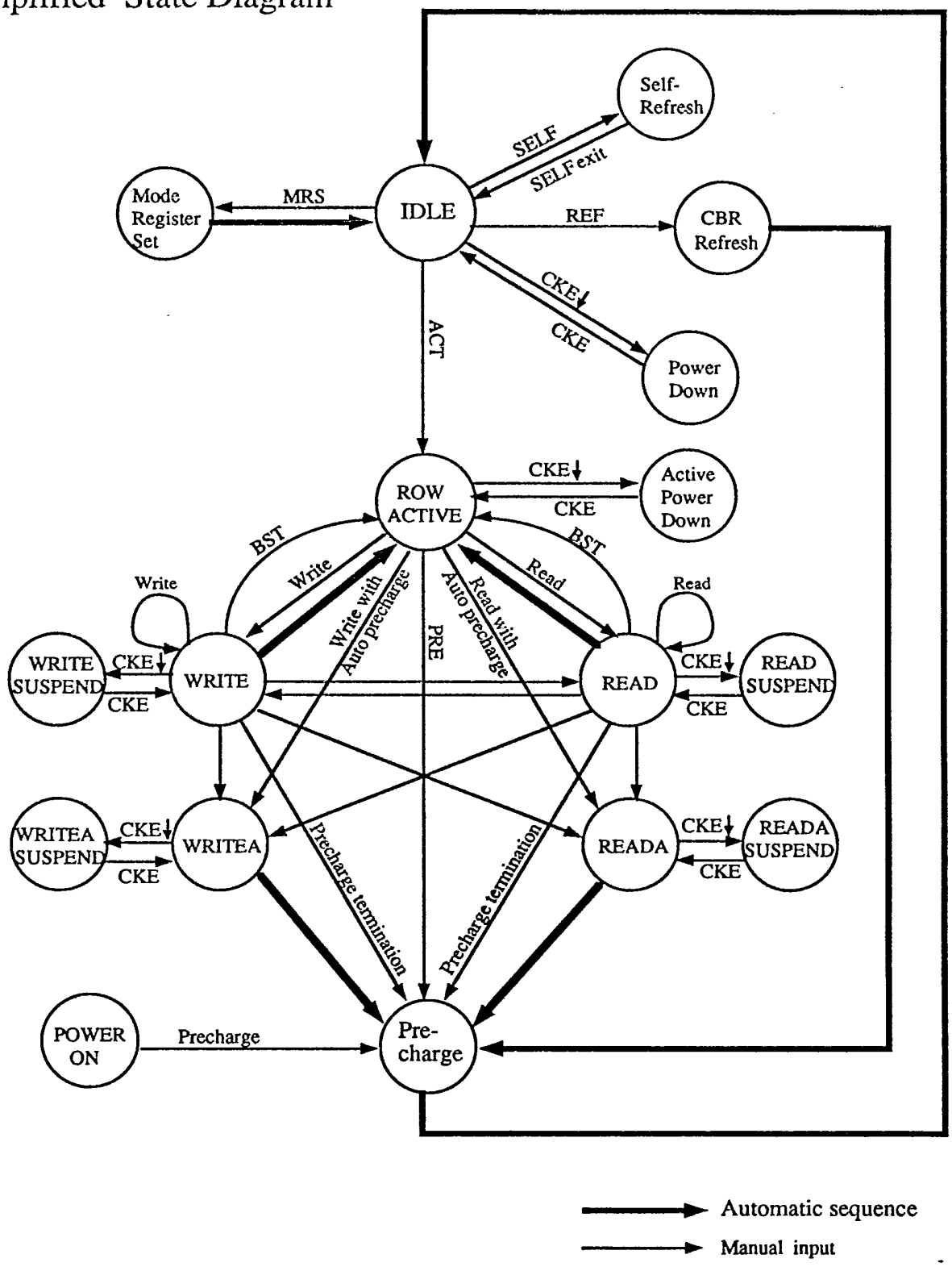


Fig.9 No Operation

Simplified State Diagram



Command truth table

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9 -0
		n-1	n							
Device Deselect	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Precharge	WRITA	H	X	L	H	L	L	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Precharge select Bank	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

DQM truth table

Function	Symbol	CKE		DQM	
		n-1	n	U	L
Data Write / Output Enable	ENB	H	X	L	
Data Mask / Output Disable	MASK	H	X	H	
Upper byte Write Enable / Output Enable	ENBU	H	X	L	X
Lower byte Write Enable / Output Enable	ENBL	H	X	X	L
Upper byte Write Inhibit / Output Disable	MASKU	H	X	H	X
Lower byte Write Inhibit / Output Disable	MASKL	H	X	X	H

CKE truth table

Current state	Function	Sym bol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add
			n-1	n					
Activating	Clock Suspend Mode Entry		H	L	X	X	X	X	X
Any	Clock Suspend		L	L	X	X	X	X	X
Clock suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

H : High level, L : Low level
X : High or Low level (Don't care) , V: Valid Data input

Operative command table 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Idle	H	X	X	X	X	DESL	Nop or Power Down	5
	L	H	H	X	X	NOP or BST	Nop or Power Down	5
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	Row Active	
	L	L	H	L	BA,A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self Refresh	6
	L	L	L	L	Op-Code	MRS	Mode Register Access	
Row Active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA,CA,A10	READ/READA	Begin Read:Determine AP	11
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Begin Write:Determine AP	11
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Precharge	8
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue Burst to End->Row Active	
	L	H	H	H	X	NOP	Continue Burst to End->Row Active	
	L	H	H	L	X	BST	Burst Stop ->Row Active	
	L	H	L	H	BA,CA,A10	READ/READA	Term Burst,New Read: Determine AP	9
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Term Burst,Start Write: Determine AP	4,9
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term Burst,Precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue Burst to End->Write Recovering	
	L	H	H	H	X	NOP	Continue Burst to End->Write Recovering	
	L	H	H	L	X	BST	Burst Stop ->Row Active	
	L	H	L	H	BA,CA,A10	READ/READA	Term Burst,Start Read: Determine AP	4,9
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Term Burst,New Write: Determine AP	9
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term Burst,Precharging	10
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Operative command table 1 (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Read with Auto Precharge	H	X	X	X	X	DESL	Continue Burst to End->Precharging	
	L	H	H	H	X	NOP	Continue Burst to End->Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	DESL	Continue Burst to End->Write Recovering with Auto Precharge	
	L	H	H	H	X	NOP	Continue Burst to End->Write Recovering with Auto Precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharg-ing	H	X	X	X	X	DESL	Nop->Enter Idle after tRP	
	L	H	H	H	X	NOP	Nop->Enter Idle after tRP	
	L	H	H	L	X	BST	Nop->Enter Idle after tRP	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Nop->Enter Idle after tRP	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row Activating	H	X	X	X	X	DESL	Nop->Enter Row Active after tRCD	
	L	H	H	H	X	NOP	Nop->Enter Row Active after tRCD	
	L	H	H	L	X	BST	Nop->Enter Row Active after tRCD	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	IILLEGAL	3,7
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Operative command table 1 (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Write Recover-ing	H	X	X	X	X	DESL	Nop->Enter Row Active after tDPL	
	L	H	H	H	X	NOP	Nop->Enter Row Active after tDPL	
	L	H	H	L	X	BST	Nop->Enter Row Active after tDPL	
	L	H	L	H	BA,CA,A10	READ/READA	Start Read, Determine AP	4
	L	H	L	L	BA,CA,A10	WRIT/WRITA	New Write, Detemine AP	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write Recover-ing with Auto Precharge	H	X	X	X	X	DESL	Nop->Enter Precharge after tDPL	
	L	H	H	H	X	NOP	Nop->Enter Precharge after tDPL	
	L	H	H	L	X	BST	Nop->Enter Precharge after tDPL	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3,4
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refresh-ing	H	X	X	X	X	DESL	Nop->Enter Idle after tRC	
	L	H	H	X	X	NOP/BST	Nop->Enter Idle after tRC	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	H	X	X	ACT/ PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/ MRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DESL	Nop->Enter Idle after 2Clocks	
	L	H	H	H	X	NOP	Nop->Enter Idle after 2Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/ PALL/ REF/ SELF/MRS	ILLEGAL	

Notes for "Operative command table 1,2,3"

1. H:High level, L:Low level,X:High or low level(Don't care),V:Valid data input
2. All entries assume that CKE was active(High level) during the preceding clock cycle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both banks are idle, and CKE is inactive(Low level), µPD4516XX will enter Power Down Mode. All input buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive(Low level), µPD4516XXX will enter Self-Refresh mode. All input buffers except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

Command truth table for CKE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action	Note
Self-Refresh (S.R.)	H	X	X	X	X	X	X	INVALID,CLK(n-1) would exit S.R	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain S.R.	
Self-Refresh Recovery	H	H	H	X	X	X	X	Idle after tRC	
	H	H	L	H	H	X	X	Idle after tRC	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin Clock Suspend next cycle	5
	H	L	L	H	H	X	X	Begin Clock Suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	2
	L	L	X	X	X	X	X	Maintain Clock Suspend	
Power Down (P.D.)	H	X	X	X	X	X		INVALID,CLK(n-1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D.->Idle	2
	L	L	X	X	X	X	X	Maintain Power Down Mode	
Both Banks Idle	H	H	H	X	X	X		Refer to Operations in Table 1	
	H	H	L	H	X	X		Refer to Operations in Table 1	
	H	H	L	L	H	X		Refer to Operations in Table 1	
	H	H	L	L	L	H	X	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to Operations in Table 1	
	H	L	H	X	X	X		Refer to Operations in Table 1	
	H	L	L	H	X	X		Refer to Operations in Table 1	
	H	L	L	L	H	X		Refer to Operations in Table 1	
	H	L	L	L	L	H	X	Self Refresh	3
	H	L	L	L	L	L	Op-Code	Refer to Operations in Table 1	
	L	X	X	X	X	X	X	Power-Down	3
Any State other than listed above.	H	H	X	X	X	X	X	Refer to Operations in Table 1.	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	4
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend.	

Notes for "Command truth table for CKE"

1. H:High level, L:Low level, X:High or low level(Don't care)
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously.A minimum setup time must be satisfied before any command other than EXIT.
3. Power-Down and Self-Refresh can be entered only from the Both Banks Idle State.
4. Must be legal command as defined in Operative command table 1.
5. Illegal if t_{SREX} is not satisfied.

Command truth table for 2-bank operation

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A9-0	Action	"FROM" State	"TO" State
H	X	X	X	X	X	X	NOP	Any	Any
L	H	H	H	X	X	X	NOP	Any	Any
L	H	H	L	X	X	X	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	X	H	X	Precharge	(R/W/A/I)0(I/A)1	I0I1
				X	H	X		(R/W/A/I)1(I/A)0	I1I0
				H	L	X		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	X		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	X		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	X		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	X	X	X	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes for "Command truth table for 2-bank operation"

1.Logic level abbreviations
H:High level, L:Low level, X:High or low level(Don't care)
Pin name abbreviation
BA:Bank address (A11)
2.State abbreviations
I = Idle
A = Row active
R = Read with No precharge (No precharge is posted)
W = Write with No precharge (No precharge is posted)
RP = Read with auto precharge (Precharge is posted)
WP = Write with auto precharge (Precharge is posted)
Any = Any State
X0Y1 = Y1X0 = Bank0 is in state "X",Bank1 is in state "Y"
(X/Y)0Z1 = Z1(X/Y)0 = Bank0 is in state "X"or"Y",Bank1 is in state "Z"
3.If the μPD4516XXX is in a state other than above listed in the "From State" column, the command is illegal.
4.The states listed under "To" might not be entered on the next clock cycle. Timing restrictions apply.

Initialization

Synchronous DRAM must be initialized in the power-on sequence, like conventional DRAMs. Once power has been applied, a 100 µs delay must precede any signals being toggled. During this delay, CKE and DQM must be held high. After the 100 µs delay, both banks must be precharged using the All Banks Precharge command. Once Precharge is completed and the minimum t_{RP} is satisfied, the Mode Register can be programmed.

Two clocks after the Mode Register Set command, two CBR Refresh command that satisfy the t_{RC} on on each CBR Refresh cycle must be performed.

Programming the mode Register

The mode register is programmed by the Mode Register Set command using address bits A11 - A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options	A11 - A7
CAS latency	A6 - A4
Wrap type	A3
Burst length	A2 - A0

After Mode Register programming, any command can not be asserted for at least two clocks.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ Latency is the most critical of the parameters being set. It tells the device how many clocks must elapse befor the data will be available. The NEC SDRAM is capable of reconfiguring its internal architecture based on the value of $\overline{\text{CAS}}$ Latency.
The valueis determined by the frequency of the clock and the speed grade of the device. Table of page 39 shows the relationship of $\overline{\text{CAS}}$ Latency to the clock period and the speed grade of the device.

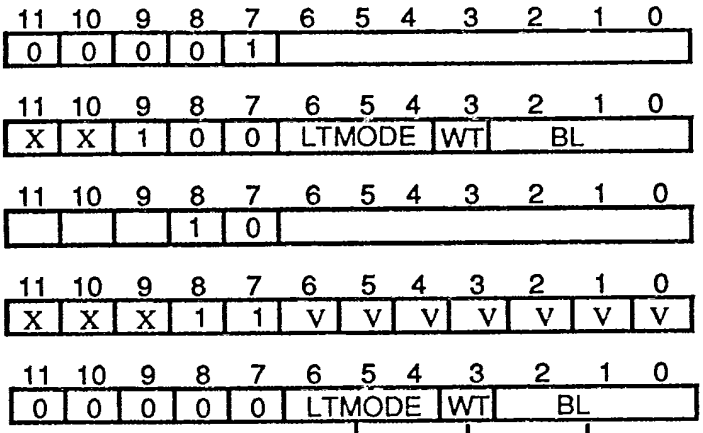
Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst has completed, the output bus will become high impedance.
The burst lengthis programmable as 1, 2, 4, 8 or full page.

Wrap Type(Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed . This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.
Some microprocessor cache system are optimized for sequential addressing and othrs for interleaved addressing. Table of the page 23 shows the addressing sequense for each burst length using them. Both sequences support burst of 1, 2, 4 and 8. Additionally ,sequential sequence supports the full page length.

Mode-Register

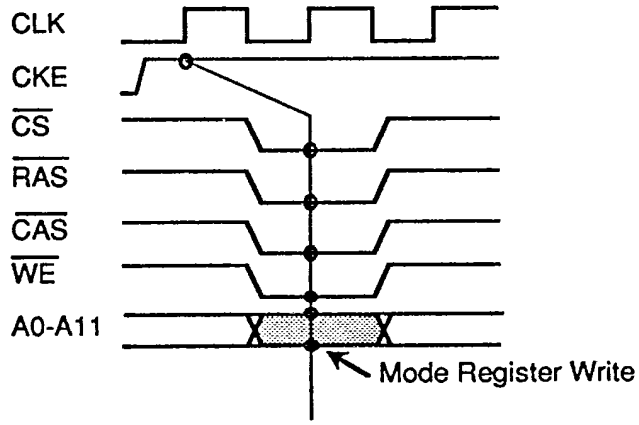


Burst Length	Bits2-0	WT=0	WT=1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R*	R*
	101	R*	R*
	110	R*	R*
	111	Full Page	R*

Wrap Type		
	0	Sequential
	1	Interleave

Latency MODE	Bits6-4	CAS Latency
	000	R*
	001	1
	010	2
	011	3
	100	R*
	101	R*
	110	R*
	111	R*

Mode-Register write timing



Burst Length and Sequence

Burst of Two

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1,0	1,0

Burst of Four

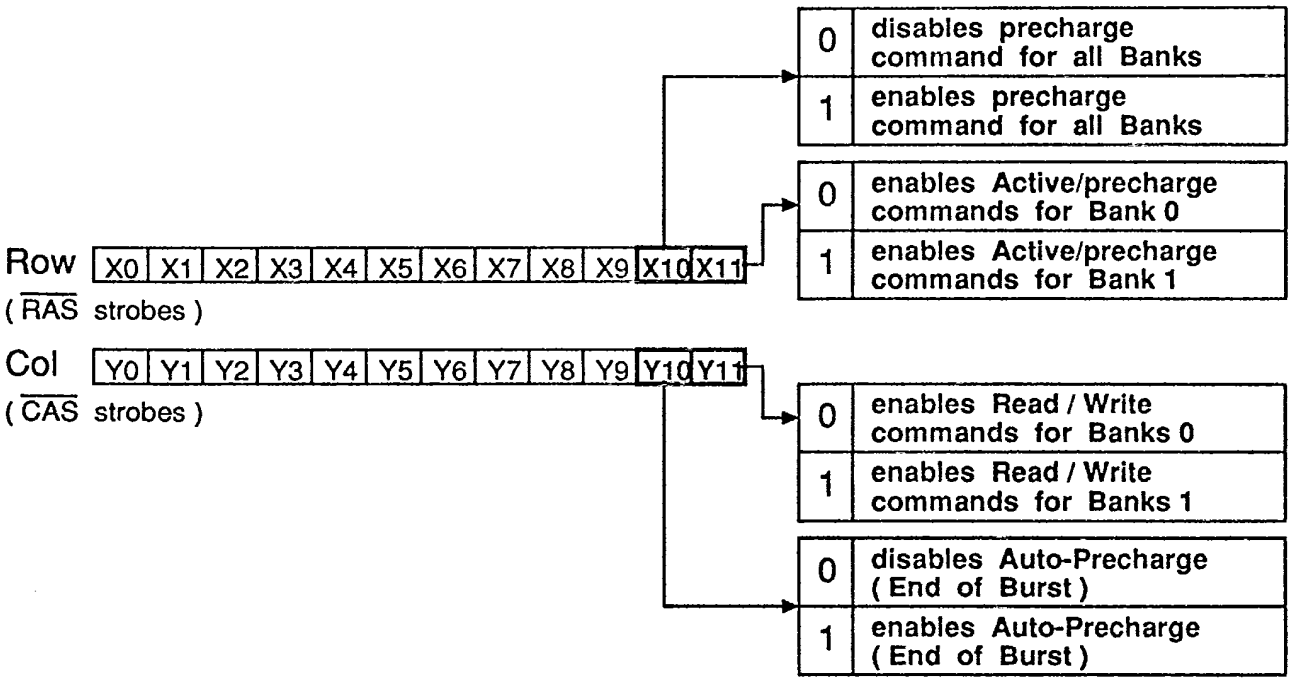
Starting Address (column address A1-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

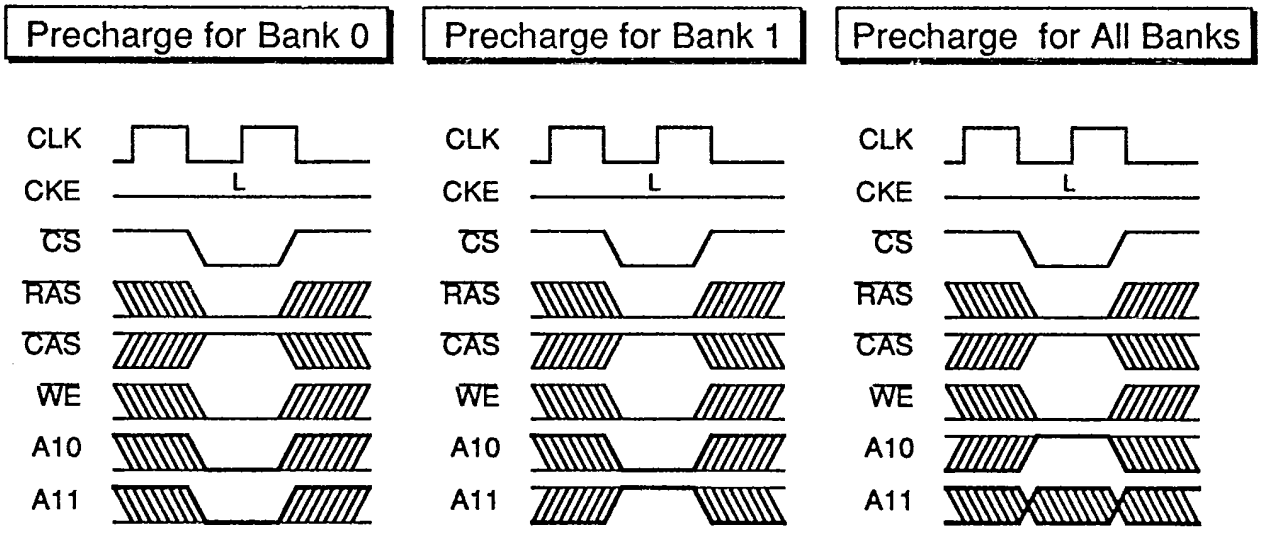
Burst of Eight

Starting Address (column address A2-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 (for 2M x8 / 9 devices), 1024 (for 4M x4 device) and 256(for 1Mx16/18 devices).

Address bits of Bank-Select and Precharge





Auto precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins after the burst access automatically.

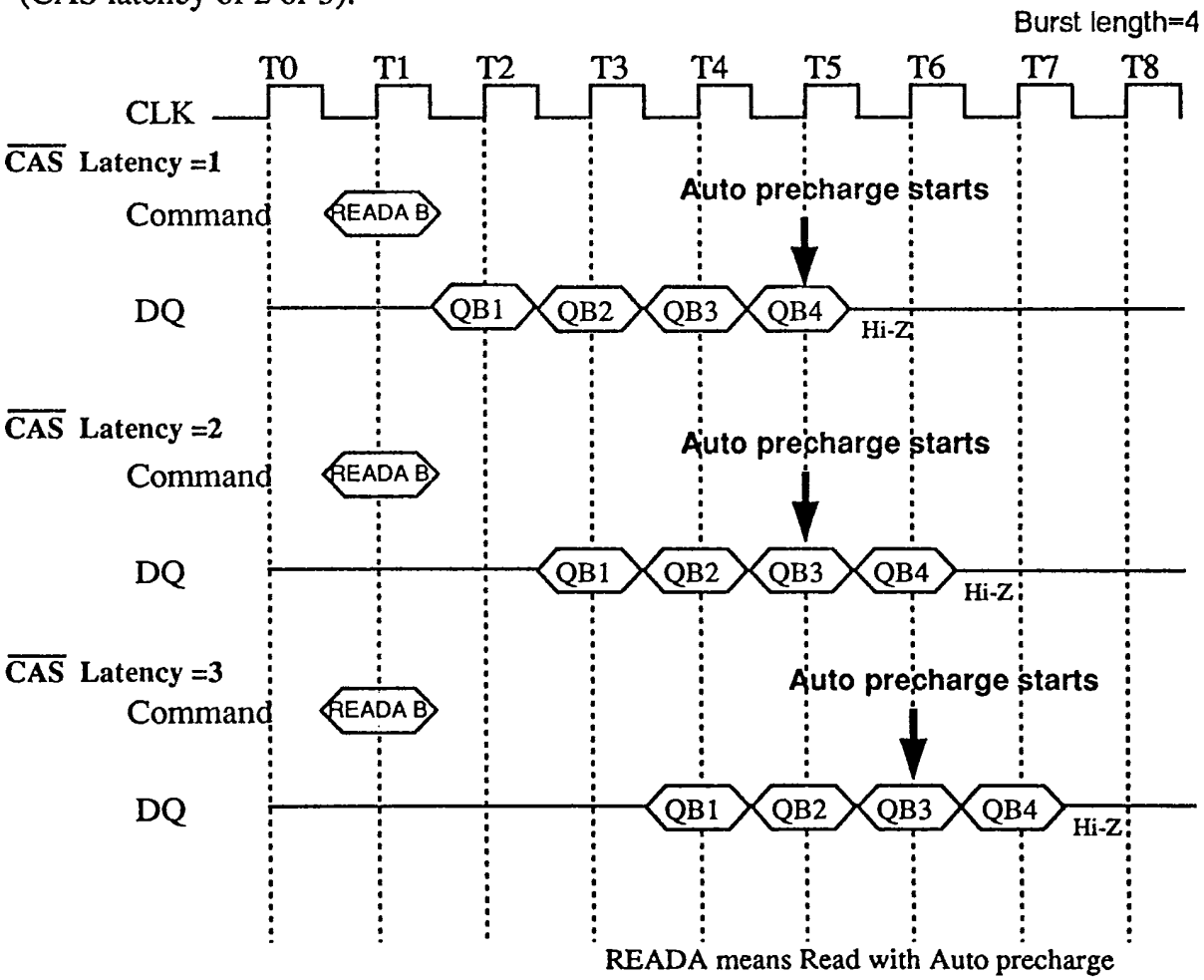
In write cycle , the t_{DAL} must be satisfied to assert the next activate command to the bank being precharged. And it is not necessary to know when the precharge starts.

When using auto precharge in read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharge can not be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

The clock that begins the auto precharge cycle is depend on both the $\overline{CAS}$ latency programmed into the mode register and whether READ or WRITE cycle.

Read with Auto precharge

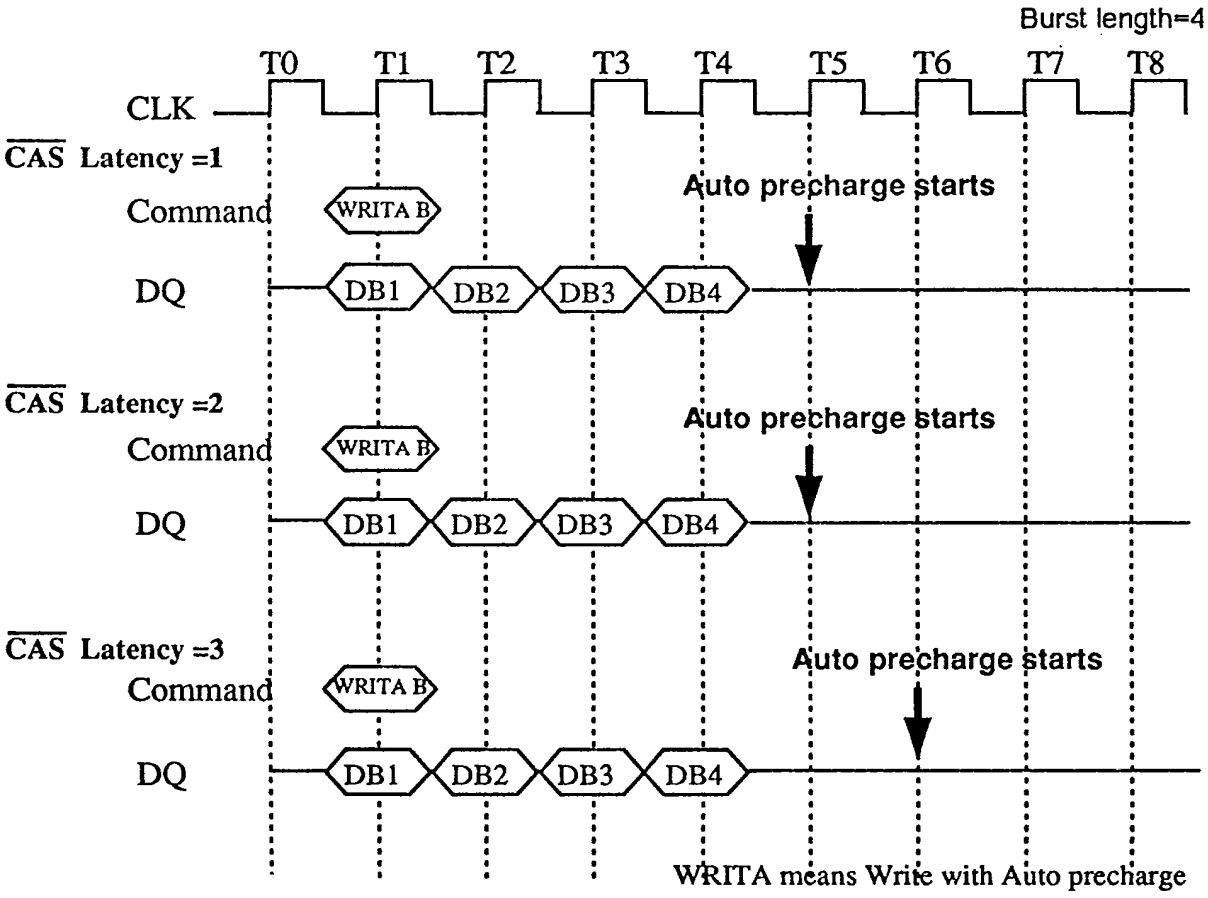
During READ cycle, the auto precharge begins on the clock that indicates the last data word output during the burst is valid ($\overline{CAS}$ latency of 1) or one clock earlier ($\overline{CAS}$ latency of 2 or 3).



READA means Read with Auto precharge

Write with Auto precharge

During WRITE cycle, the auto precharge begins one clock after the last data word input to the device ($\overline{CAS}$ latency of 1 or 2) or two clocks after ($\overline{CAS}$ latency of 3).



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

$\overline{CAS}$ latency	Read	Write
1	0	+1
2	-1	+1
3	-1	+2

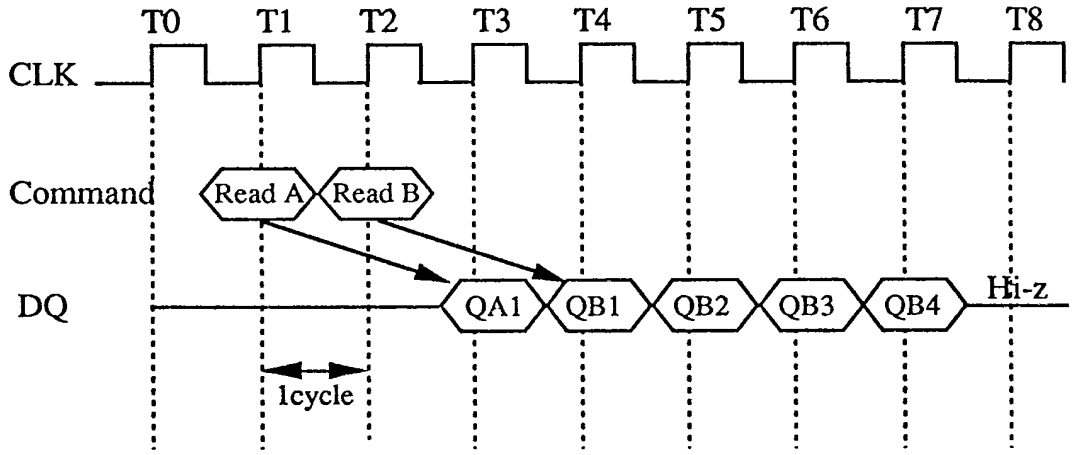
Read / Write Command Interval

Read to Read Command Interval

During READ cycle, when new Read command is asserted, it will be effective after $\overline{CAS}$ Latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

The interval between the commands is minimum 1 cycle. Each Read command can be asserted in every clock without any restriction.

Burst length=4,$\overline{CAS}$ Latency=2

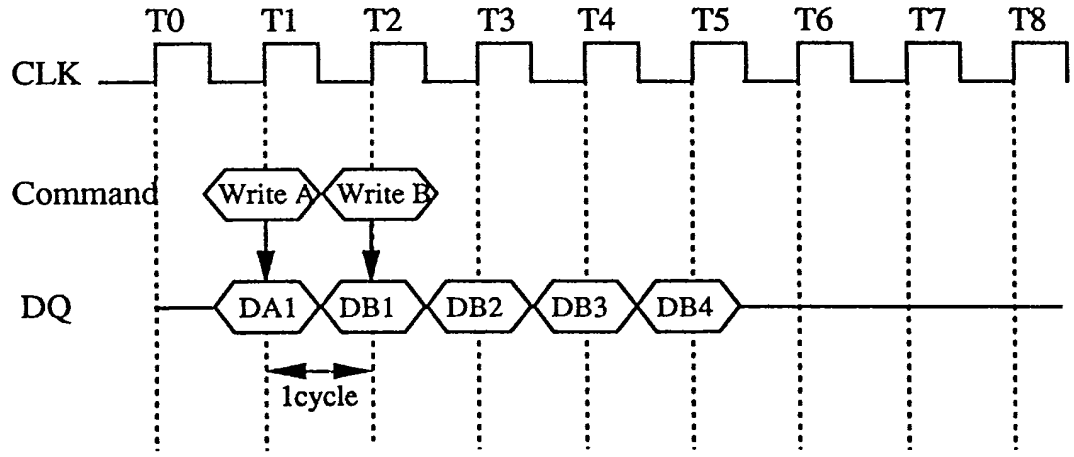


Write to Write Command Interval

During WRITE cycle, when new Write command is asserted, the previous burst will terminate and the new burst will begin with at new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be asserted in every clock without any restriction.

Burst length=4,$\overline{CAS}$ Latency=2

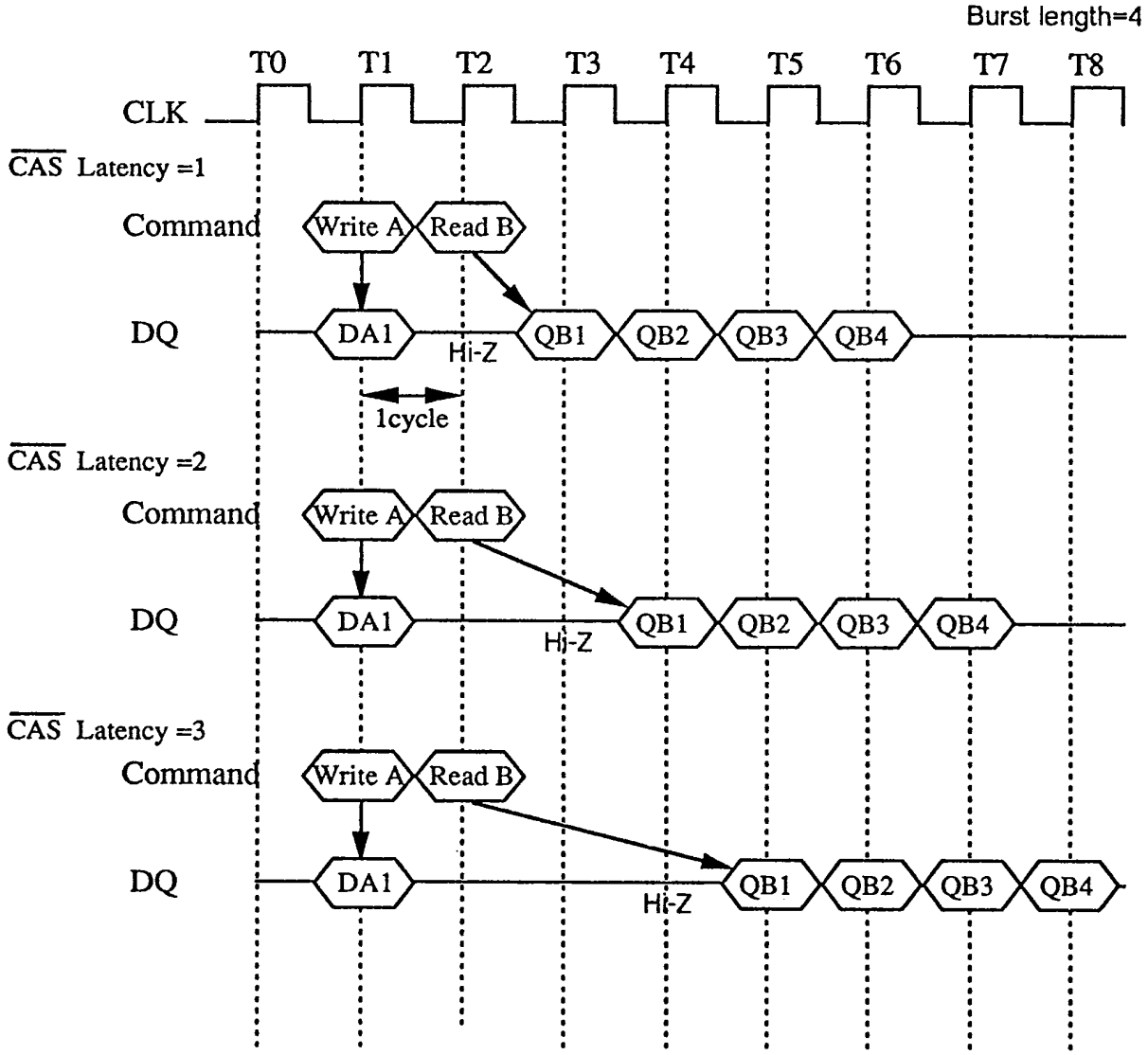


Write to Read command interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

The data bus must be Hi-Z at least one cycle prior to the first Dout.

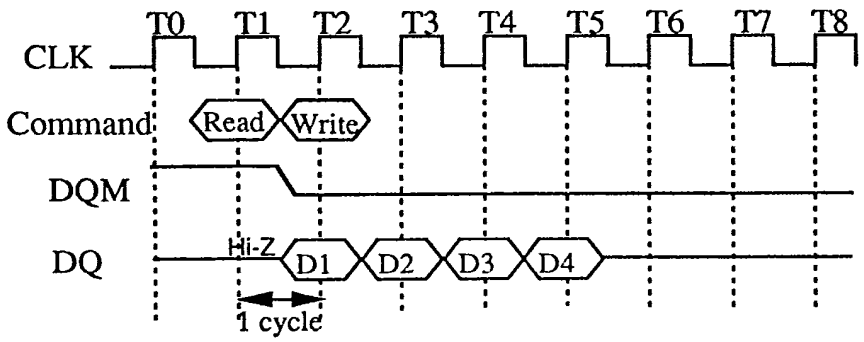


Read to Write Command Interval

During READ cycle, READ can be interrupted by WRITE. When the $\overline{CAS}$ Latency is 3 and then the burst length is Full page, the burst read can not be interrupted by WRITE. (A Burst Stop command(BST) or a Precharge command can interrupt).

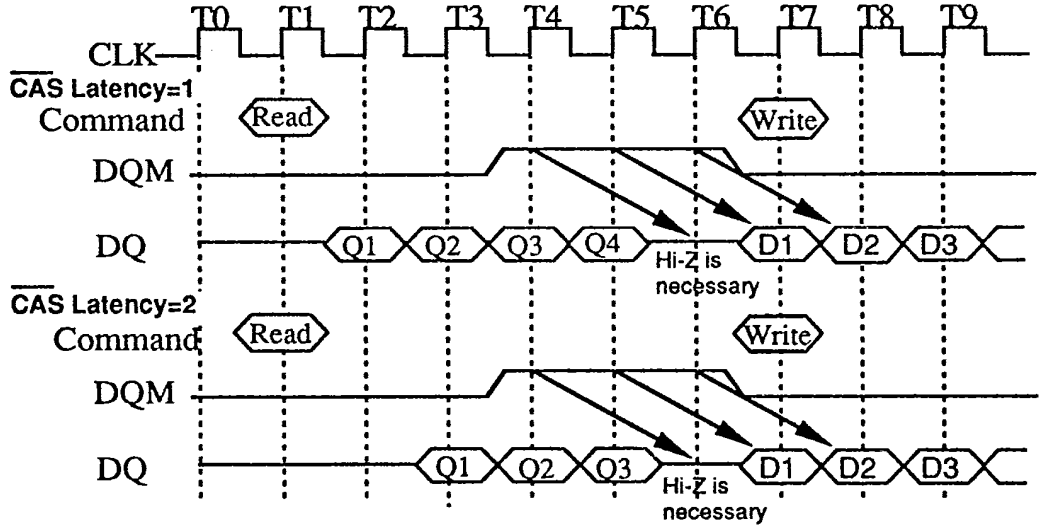
When the $\overline{CAS}$ latency is 1 or 2, the Read and Write command interval is minimum 1 cycle. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before e WRITE.

$\overline{CAS}$ Latency=1,2



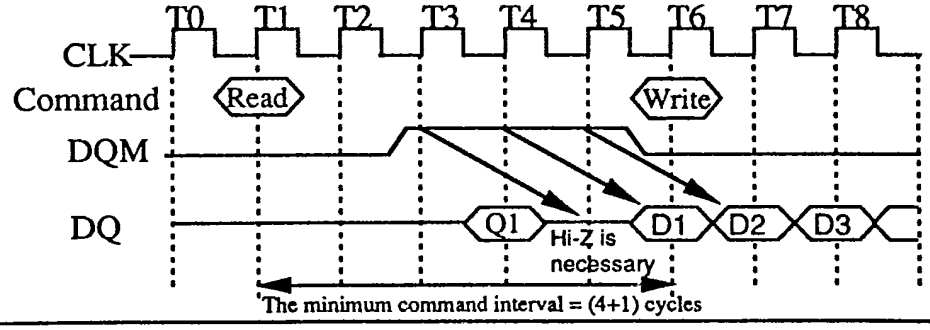
In case $\overline{CAS}$ latency is 1 or 2, READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.

Burst Length=8, $\overline{CAS}$ Latency=1, 2



In case $\overline{CAS}$ latency is 3 (burst length is not Full page), READ can be interrupted by WRITE. The minimum command interval is [burst length + 1] cycles. DQM must be High at least 3 clocks prior to the Write command.

ex.) $\overline{CAS}$ Latency=3 **Burst length=4**

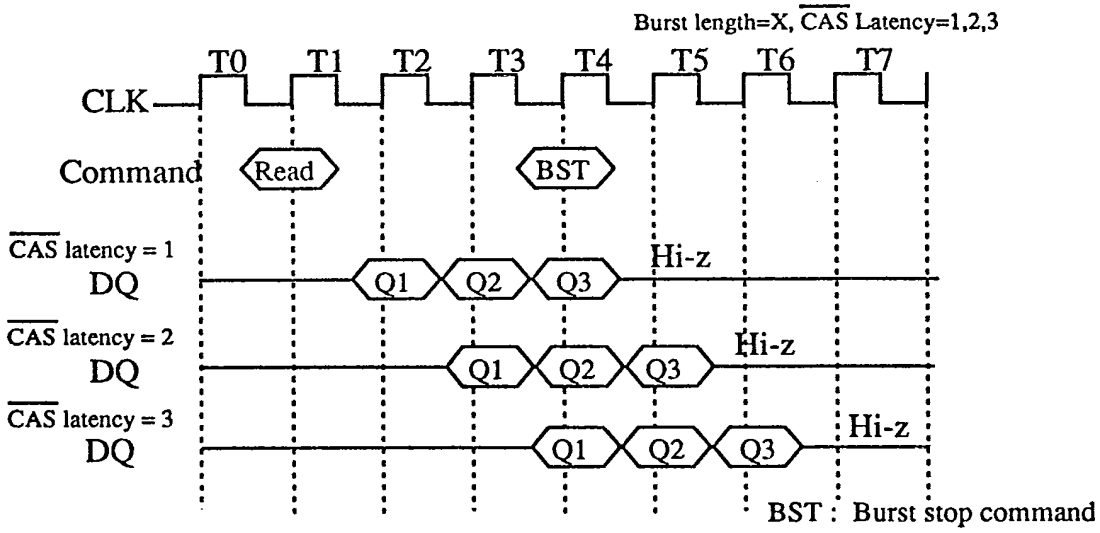


Burst termination

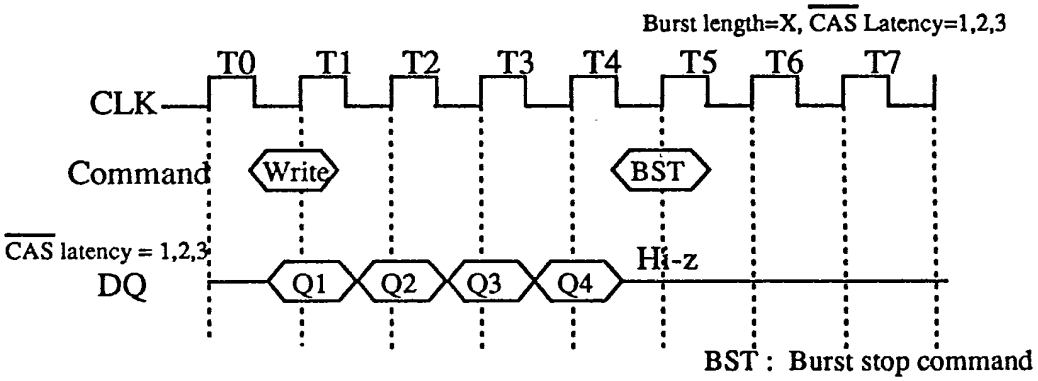
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

Burst stop command

During the READ cycle, when the burst stop command is asserted, the burst read data are terminated and the data-bus goes to High-Z after the $\overline{CAS}$ latency from the burst stop command.



During the WRITE cycle, when the burst stop command is asserted, the burst read data are terminated and data-bus go to High-Z at the same clock with the burst stop command.

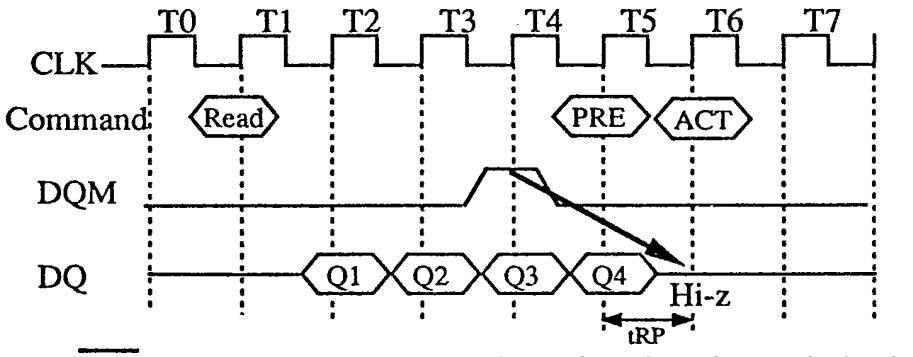


Precharge termination

During the READ cycle, the burst read operation is terminated by a precharge command.
When the precharge command is asserted,the burst read operation is terminated and precharge starts.
The same bank can be activated again after tRP from the precharge command.
The DQM must be high to mask the invalid data.

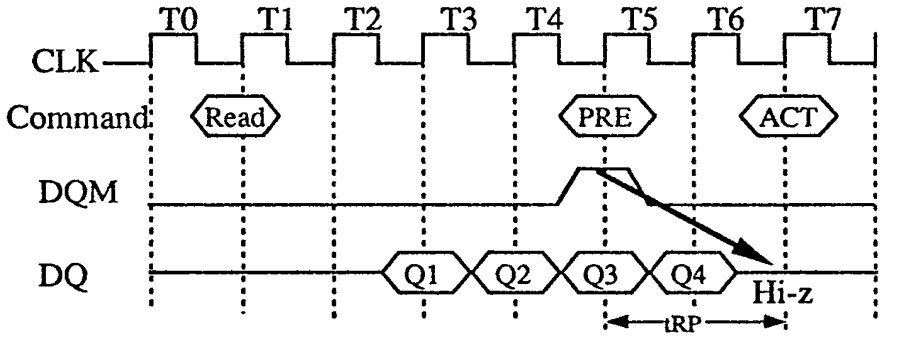
When $\overline{CAS}$ latency is 1, the read data will remain valid until the precharge command is asserted.
Invalid data may appear one clock after valid data out.
The DQM may be high to mask the invalid data.

Burst length=X, $\overline{CAS}$ Latency=1



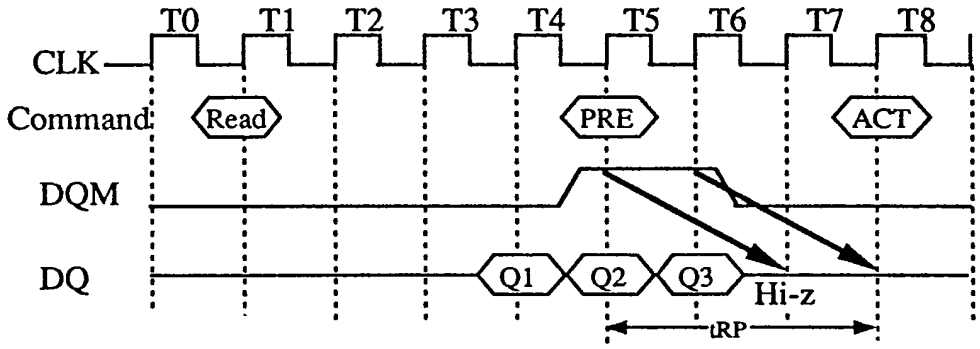
When $\overline{CAS}$ latency is 2, the read data will remain valid until one clock after the precharge command. Invalid data may appear one clock after valid data out.
The DQM may be high to mask the invalid data .

Burst length=X, $\overline{CAS}$ Latency=2



When $\overline{CAS}$ latency is 3, the read data will remain valid until one clock after the precharge command. Invalid data may appear one and two clocks after valid data out.
The DQM may be high to mask the invalid data.

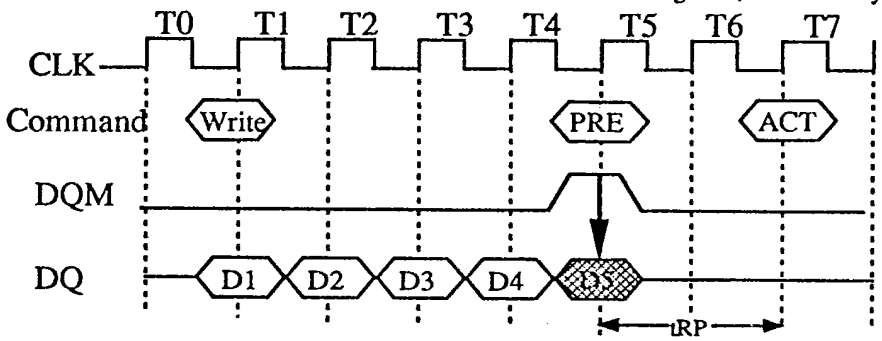
Burst length=X, $\overline{CAS}$ Latency=3



During the Write cycle, the burst write operation is terminated by a precharge command.
When the precharge command is asserted,the burst write operation is terminated and precharge starts.
The same bank can be activated again after tRP from the precharge command.
The DQM must be high to mask invalid data in.

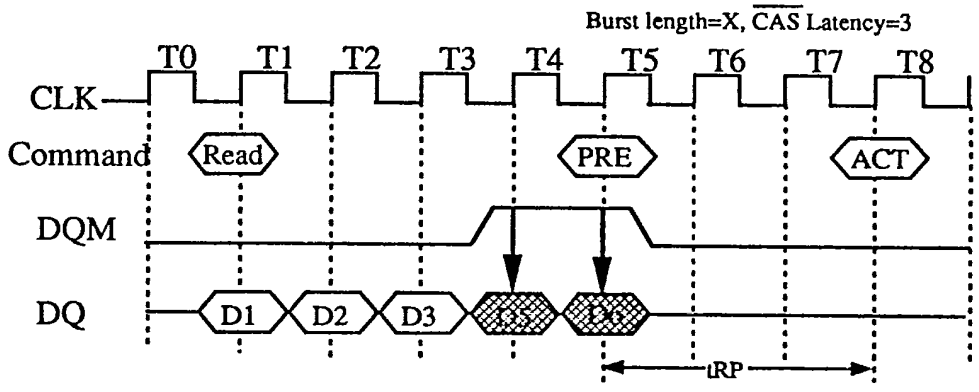
When $\overline{CAS}$ latency is 1 or 2, the write data written prior to the precharge command will be correctly stored.
However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

Burst length=X, $\overline{CAS}$ Latency=1, 2



When $\overline{CAS}$ latency is 3, the write data written more than one clock prior to the precharge command will be correctly stored.
However, invalid data may be written at one clock before and the same clock as the precharge command.
To prevent this from happening, DQM must be high from one clock prior to the precharge command until the precharge command. This will mask the invalid data.

Burst length=X, $\overline{CAS}$ Latency=3



Electrical Specifications

ABSOLUTE MAXIMUM RATINGS *

Voltage on Power Supply Pin Relative to GND	-1.0 to +4.6	V
Voltage on Input Pin Relative to GND	-1.0 to +4.6	V
Short Circuit Output Current	50	mA
Power Dissipation	1	W
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +125	°C

*COMMENT : Exposing the device to stress above those listed in absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	Vcc	3.0	3.3	3.6	V
High Level Input Voltage	VIH	2.0		4.6	V
Low Level Input Voltage	VIL	-0.3		0.8	V
Ambient Temperature	Ta	0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) 1/2

3.5 4.0

PARAMETER	SYMBOL	TEST CONDITION	CAS Latency	GRADE	MAXIMUM X4	MAXIMUM X8	MAXIMUM X16	UNIT	NOTE
Operating Current	Icc 1	Burst length = 1 tRC≥ tRC(MIN) Io = 0 mA	CL=1	-10	70	75	80	mA	3
				-12	65	70	75		
				-13	60	65	70		
				-15	60	65	70		
			CL=2	-10	75	80	85	mA	3
				-12	70	75	80		
				-13	65	70	75		
				-15	65	70	75		
			CL=3	-10	80	85	90	mA	3
				-12	75	80	85		
				-13	70	75	80		
				-15	65	70	75		
PrechargeStandby Current in Power-down mode	Icc 2P	CKE ≤ VIL (MAX) tCK= 15ns			3	3	3	mA	
	Icc 2PS	CKE ≤ VIL (MAX) tCK= ∞			2	2	2		
PrechargeStandby Current in Non power-down mode	Icc 2N	CKE ≥ VIH (MIN) tCK= 15ns CS ≥ VIH(MIN) Input signals are changed one time during 30ns.			20	20	20	mA	
	Icc 2NS	CKE ≥ VIH (MIN) tCK=∞ Input signals are Stable.			6	6	6		
Active Standby Current in Power-down mode	Icc 3P	CKE ≤ VIL (MAX) tCK= 15ns			3	3	3	mA	
	Icc 3PS	CKE ≤ VIL (MAX) tCK= ∞			2	2	2		
Active Standby Current in Non power-down mode	Icc 3N	CKE ≥ VIH (MIN) tCK= 15ns CS ≥ VIH(MIN) Input signals are changed one time during 30ns.			25	25	25	mA	
	Icc 3NS	CKE ≥ VIH (MIN) tCK= ∞ Input signals are Stable.			10	10	10		

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) 2/2

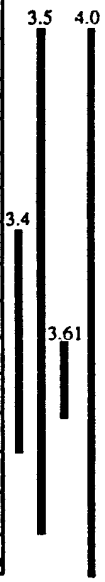
PARAMETER	SYMBOL	TEST CONDITION	CAS Latency	GRADE	MAXIMUM X4	MAXIMUM X8	MAXIMUM X16	UNIT	NOTE
Operating Current (Burst Mode)	Icc 4	tCK ≥ tCK (MIN) Io = 0 mA	CL= 1	-10	70	75	90	mA	3
				-12	60	65	80		
				-13	55	60	75		
				-15	55	60	75		
			CL= 2	-10	110	120	150		
				-12	90	100	125		
				-13	85	95	115		
				-15	85	95	115		
			CL= 3	-10	150	165	210		
				-12	130	145	180		
				-13	120	130	160		
				-15	100	110	140		
Refresh Current	Icc 5	tRC ≥ tRC (MIN)	CL= 1	-10	90	90	90	mA	
				-12	80	80	80		
				-13	75	75	75		
				-15	75	75	75		
			CL= 2	-10	95	95	95		
				-12	85	85	85		
				-13	80	80	80		
				-15	80	80	80		
			CL= 3	-10	100	100	100		
				-12	90	90	90		
				-13	85	85	85		
				-15	80	80	80		
Self Refresh Current	Icc 6	CKE ≤ 0.2V		-**	2	2	2	mA	
				-**L	100	100	100	µA	

SYNCHRONOUS CHARACTERISTIC (Recommended Operating unless otherwise note)

PARAMETER		SYMBOL	-10		-12		-13		-15		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock Cycle Time	CAS Latency = 3	tCK3	10	(100MHz)	12	(83MHz)	13	(75MHz)	15	(66MHz)	ns	
	CAS Latency = 2	tCK2	15	(66MHz)	18	(55MHz)	19.5	(50MHz)	19.5	(50MHz)	ns	
	CAS Latency = 1	tCK1	30	(33MHz)	36	(28MHz)	39	(25MHz)	39	(25MHz)	ns	
Access Time from CLK	CAS Latency = 3	tAC3		9		11		12		14	ns	50PF
	CAS Latency = 2	tAC2		12		15		16.5		16.5	ns	80PF
	CAS Latency = 1	tAC1		27		33		36		36	ns	80pf
CLK High Level Width		tCH	3.5		4		5		5		ns	
CLK Low Level Width		tCL	3.5		4		5		5		ns	
Data-out Hold Time		tOH	4		4		4		4		ns	
Data-out Low-Impedance Time		tLZ	0		0		0		0		ns	
Data-out High Impedance Time		tHZ	0	10	0	10	0	10	0	10	ns	
Data-in Set-up Time		tDS	3		3.5		3.5		3.5		ns	
Data-in Hold Time		tDH	1		1.5		1.5		1.5		ns	
Address Set-up Time		tAS	3		3.5		3.5		3.5		ns	
Address Hold Time		tAH	1		1.5		1.5		1.5		ns	
CKE Set-up time		tCKS	3		3.5		3.5		3.5		ns	
CKE Hold time		tCKH	1		1.5		1.5		1.5		ns	
Command($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) Set-up Time		tCMS	3		3.5		3.5		3.5		ns	
Command($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) Hold Time		tCMH	1		1.5		1.5		1.5		ns	

ASYNCHRONOUS CHARACTERISTIC (Recommended Operating unless otherwise note)

PARAMETER		SYMBOL	-10		-12		-13		-15		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF / ACTIV Command Period		tRC	100		120		130		130		ns	
ACTIVE to PRE Command Period		tRAS	70	120000	84	120000	91	120000	91	120000	ns	
PRE to ACTIVE Command Period		tRP	30		36		39		39		ns	
Delay Time ACTIVE to READ/WRITE Command		tRCD	30		36		39		39		ns	
ACTIVE(0) to ACTIVE(1) Command Period		tRRD	30		36		39		39		ns	
Data-in to PRE Command Period	CAS Latency=3	tDPL3	1CLK+10		1CLK+12		1CLK+13		1CLK+15		ns	
	CAS Latency=2	tDPL2	15		18		19.5		19.5		ns	
	CAS Latency=1	tDPL1	15		18		19.5		19.5		ns	
Data-in to ACTIVE(REF) Command Period (Auto Precharge)	CAS Latency=3	tDAL3	2CLK+30		2CLK+36		2CLK+39		2CLK+45		ns	
	CAS Latency=2	tDAL2	1CLK+30		1CLK+36		1CLK+39		1CLK+39		ns	
	CAS Latency=1	tDAL1	1CLK+30		1CLK+36		1CLK+39		1CLK+39		ns	
Self-Refresh EXit Time		tSREX	20		24		26		26		ns	
Transition Time		tT	1	30	1	30	1	30	1	30	ns	
Refresh Period		tREF		32		32		32		32	ms	2048 ROWs



DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	GRADE	MIN	TYP	MAX	UNIT	NOTE
Input Leakage Current	II (L)	VI=0 to 3.6V, all other pins noy under test =0V		-1.0		1.0	µA	
Output Leakage Current	Io(L)	Dout is disabled, Vo= 0 to 3.6V		-1.0		1.0	µA	
Output Hight Voltage	VOH	Io = -2mA		2.4			V	
Output Low Voltage	VOL	Io = +2mA				0.4	V	

CAPACITANCE(Ta=25°C, f=1MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	CI1	2		4	Pf	A0 TO A11
	CI2	2		4	Pf	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM
Data Input/Output Capacitance	CO	2		5	Pf	DQ0 TO DQ17

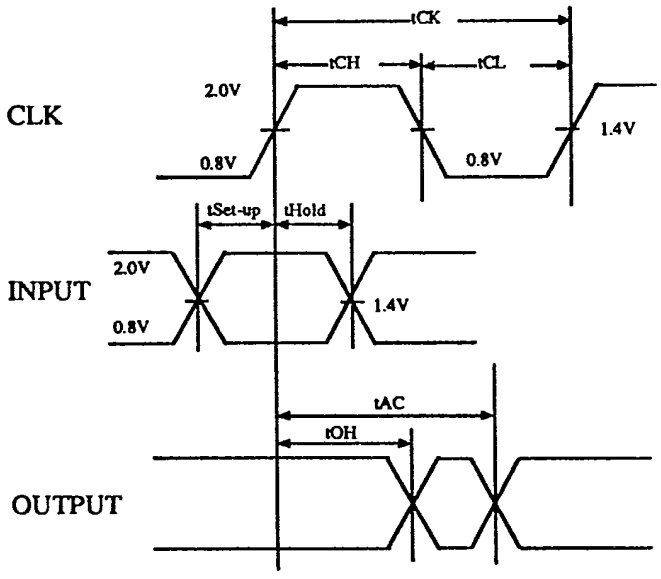
3.3

NOTES

(1) All voltages referenced Vss(Ground).
(2) An initial pause of 100µs is required after power-on followed by ***Power On Sequence & Auto Refresh*** before proper device operation is achieved.
(3) Icc1,Icc4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, Icc1,Icc4 and Icc5 are measured on condition that addresses are changed only one time during tCK(MIN).
(4) AC measurements assume tT=1ns.
(5) Reference level for measuring timing of input signals is 1.40V . Transition times are measured between VIH and VIL.
(6) An access time is measured at 1.40V
(7) If tT is longer than 1 ns,reference level for measuring timing of input signals is VIH (MIN) and VIL(MAX).

4.0

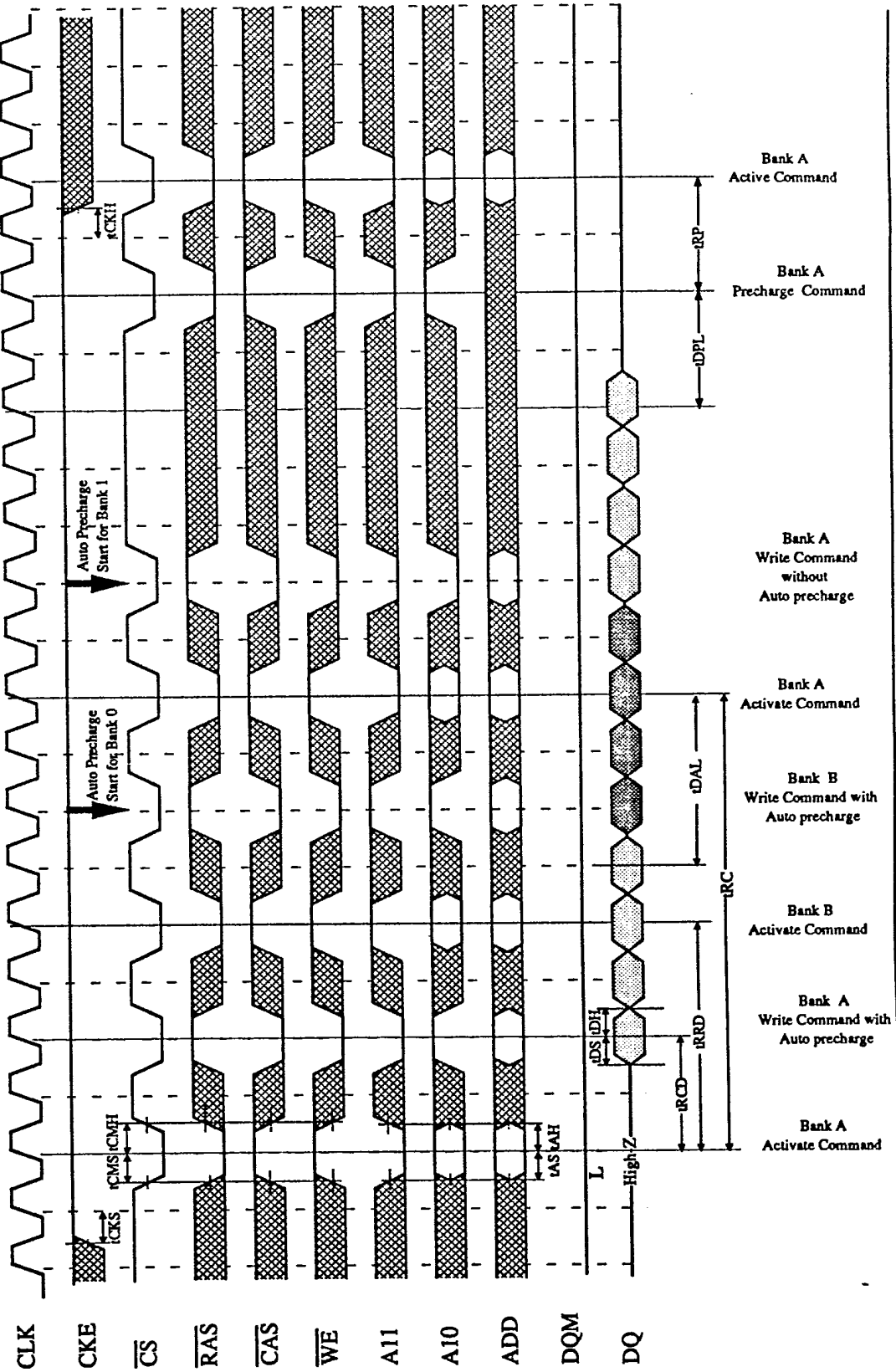
4.0



NEC

AC Parameters for Write Timing

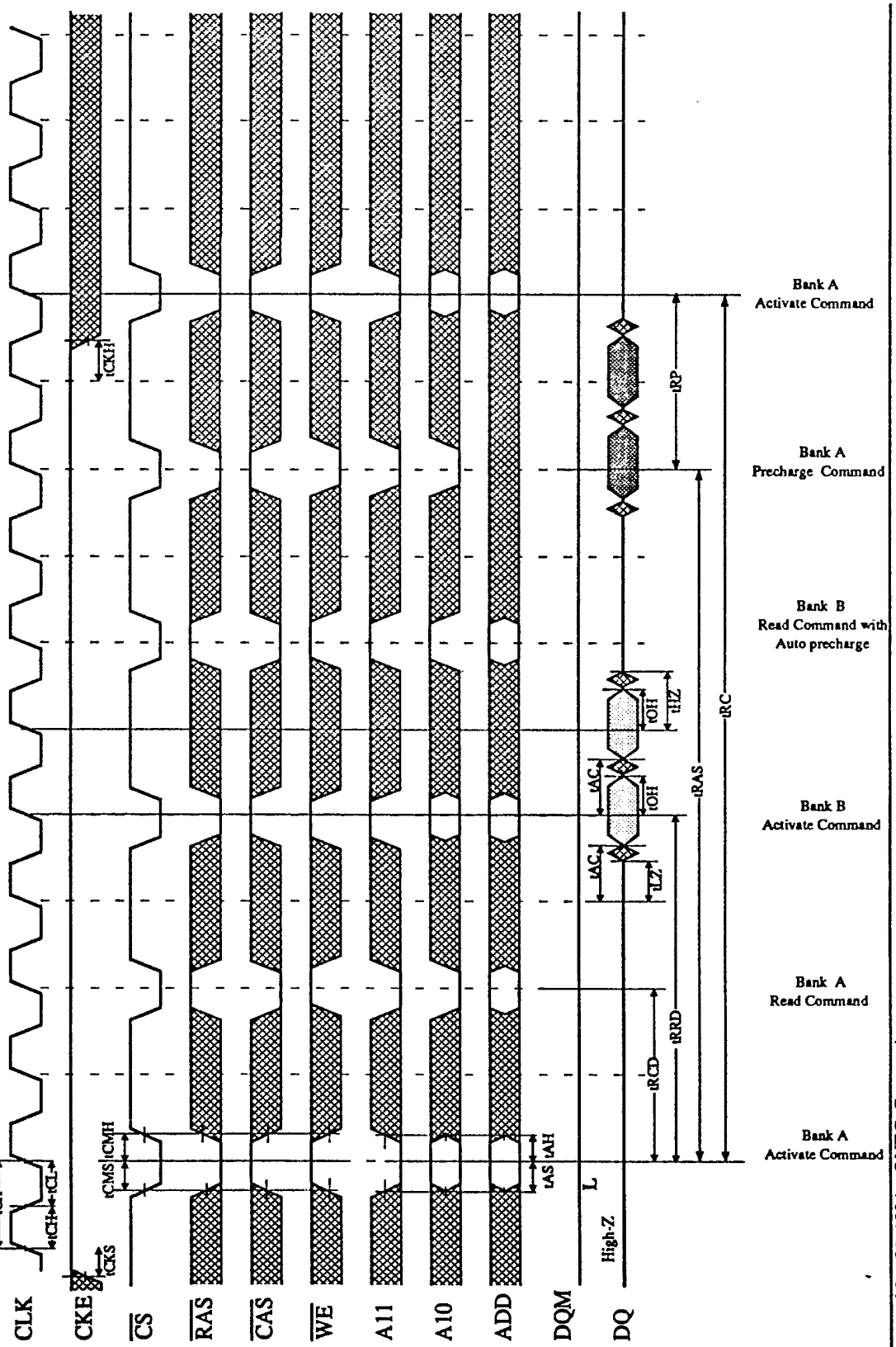
Burst Length = 4 CAS Latency = 2



NEC

AC Parameters for Read Timing

Burst Length = 2 CAS Latency = 2

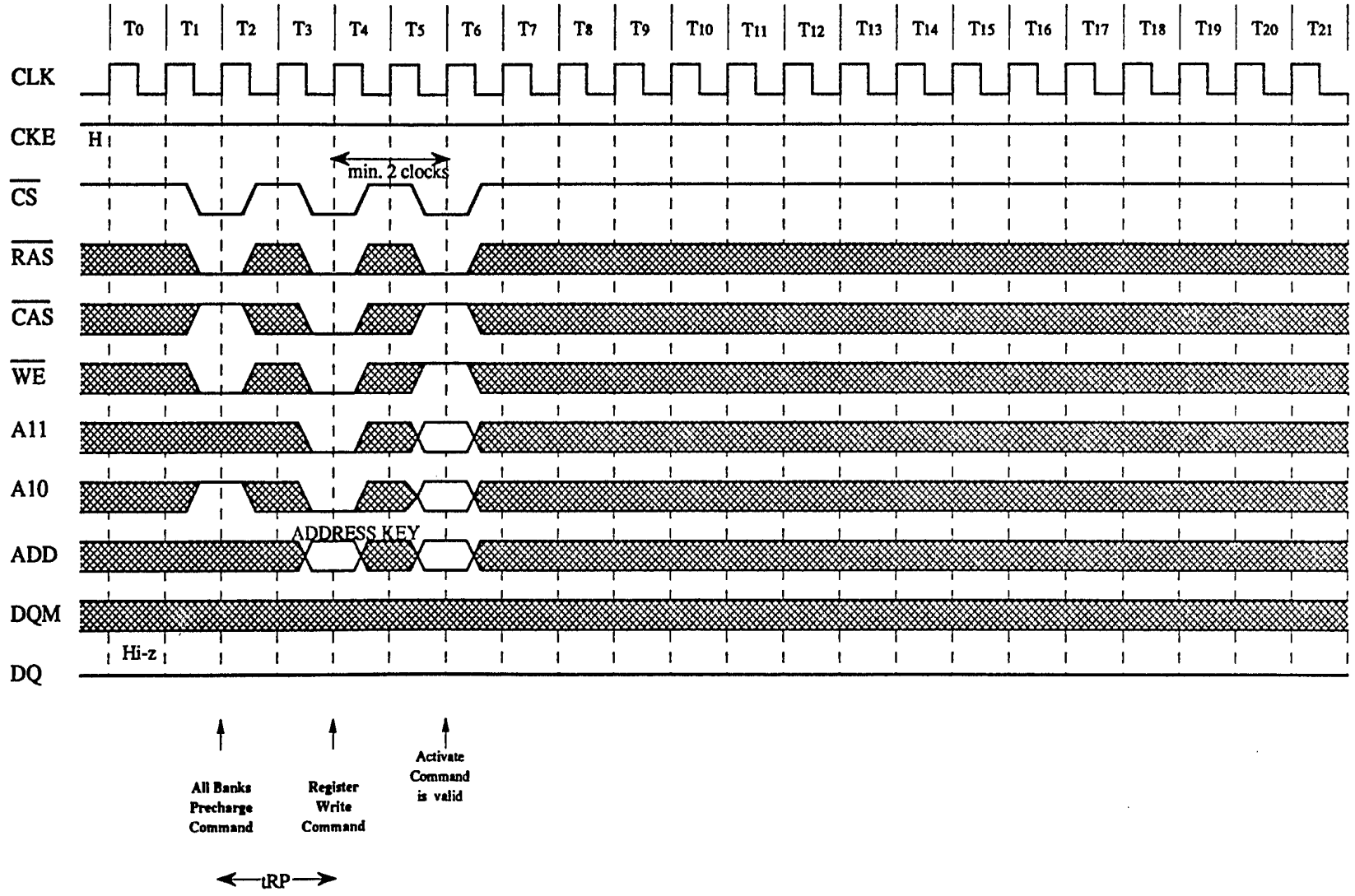


Relationship between Frequency and Latency

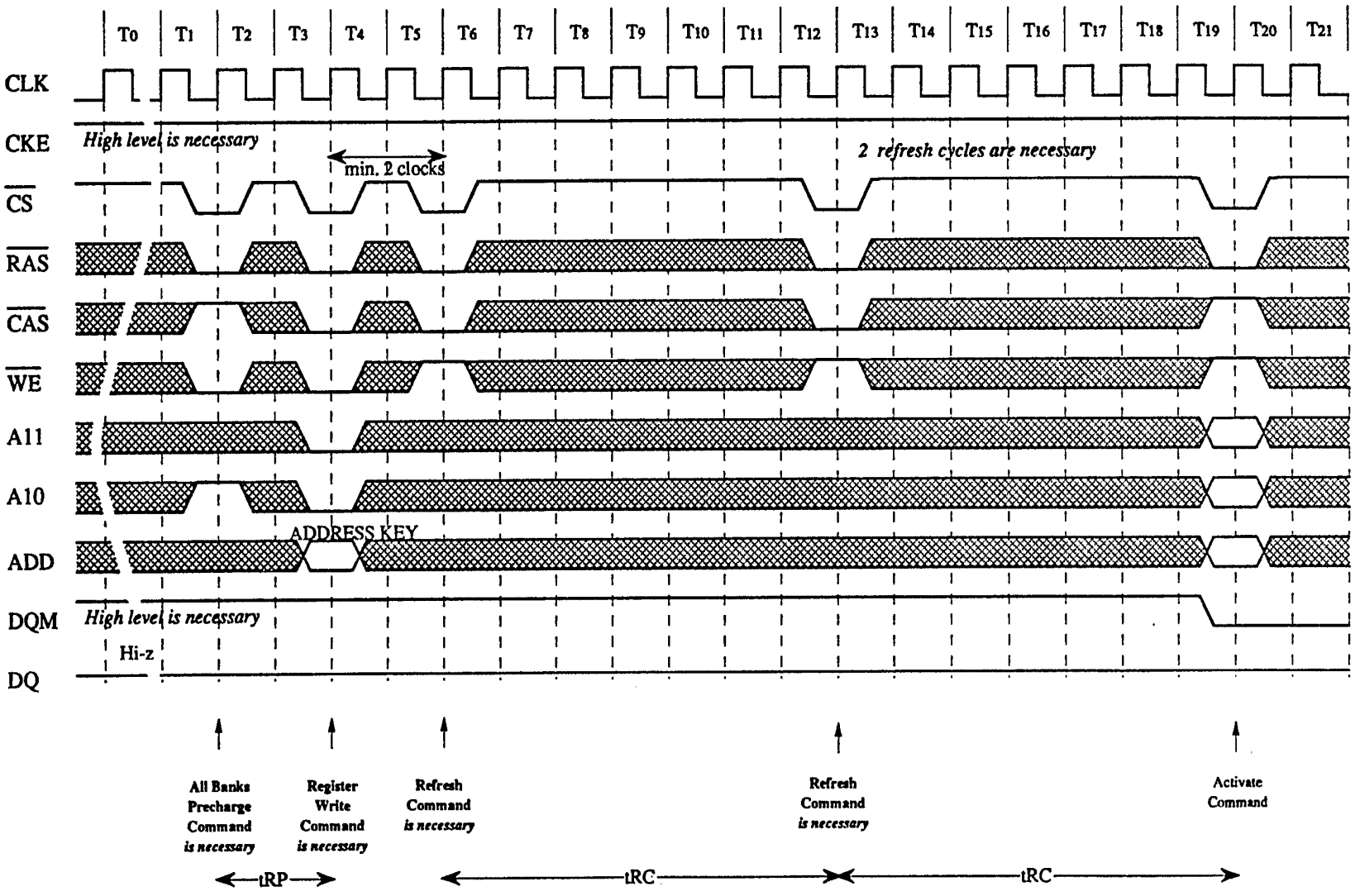
Speed Version	-10			-12			-13			-15		
Clock Cycle Time [ns]	10	15	30	12	18	36	13	19.5	39	15	19.5	39
Frequency [MHz]	100	66	33	83	55	27	75	50	25	66	50	25
CAS latency	3	2	1	3	2	1	3	2	1	3	2	1
[tRCD]	3	2	1	3	2	1	3	2	1	3	2	1
RAS latency (CAS latency +[tRCD])	6	4	2	6	4	2	6	4	2	6	4	2
[tRC]	10	7	4	10	7	4	10	7	4	10	7	4
[tRAS]	7	5	3	7	5	3	7	5	3	7	5	3
[tRRD]	3	2	1	3	2	1	3	2	1	3	2	1
[tRP]	3	2	1	3	2	1	3	2	1	3	2	1
[tDPL]	2	1	1	2	1	1	2	1	1	2	1	1
[tDAL]	5	3	2	5	3	2	5	3	2	5	3	2
[tSREX]	2	2	1	2	2	1	2	2	1	2	2	1

Mode Register Write

Burst Length = 4 CAS Latency = 2

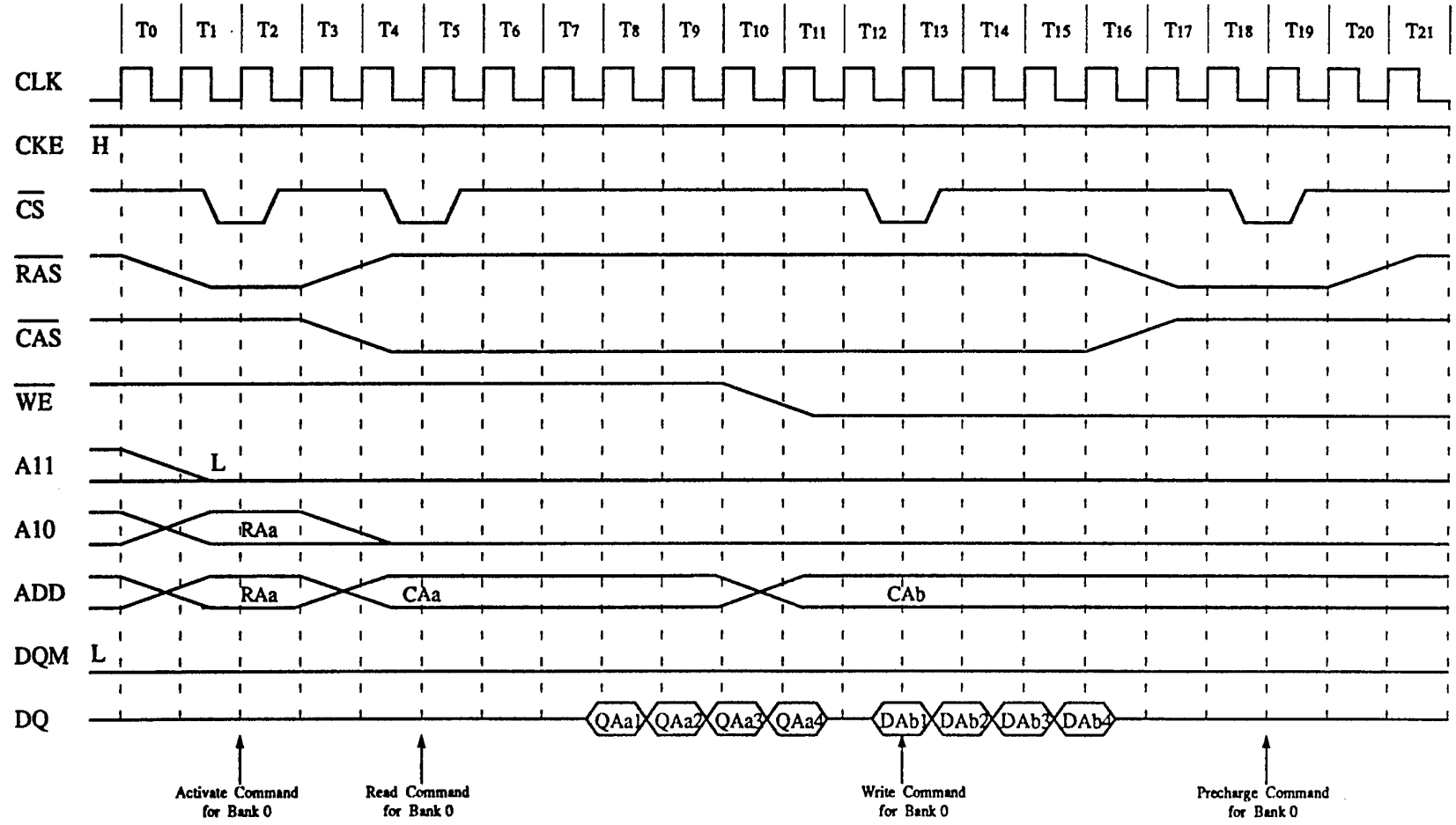


Power On Sequence & Auto Refresh



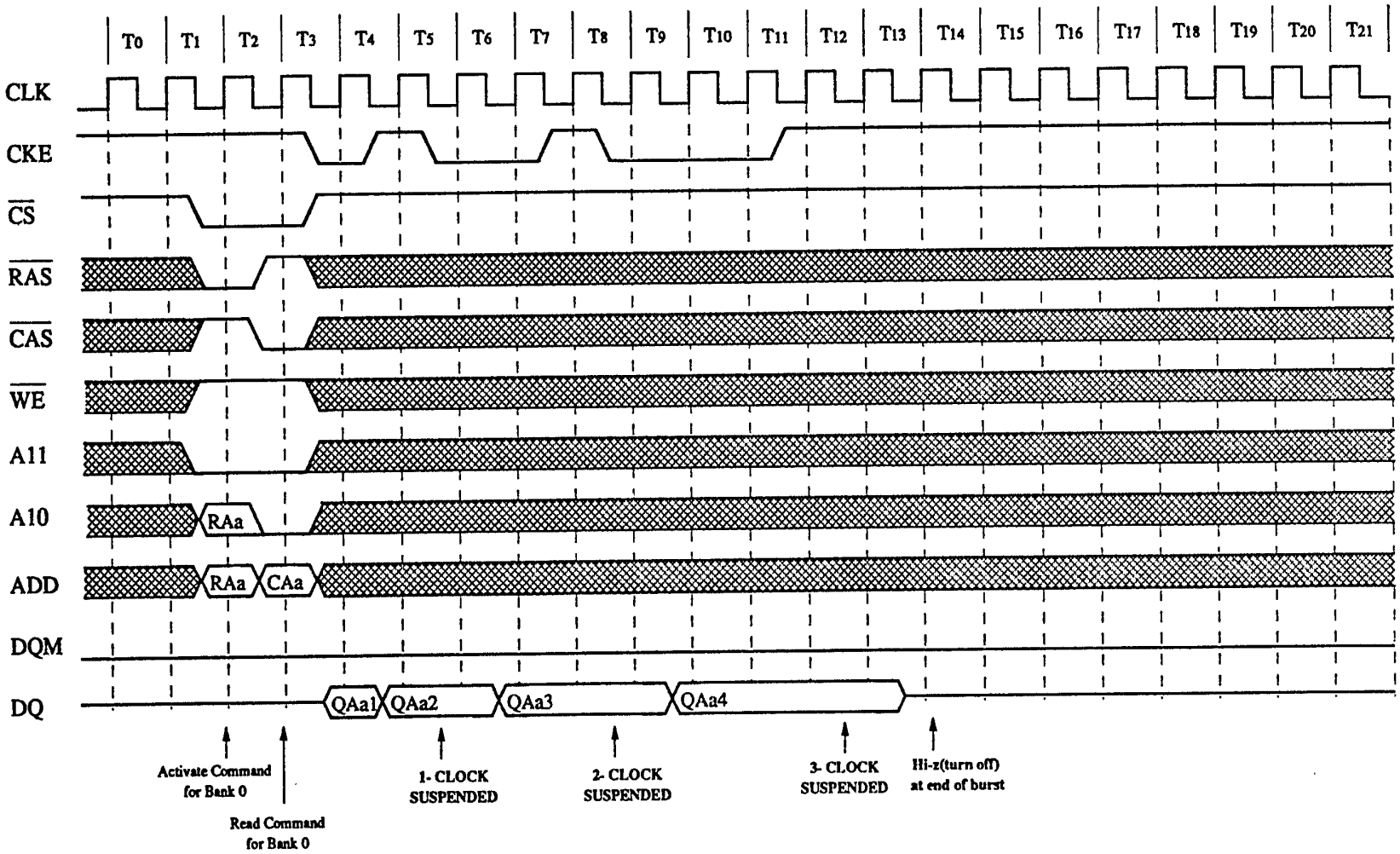
$\overline{CS}$ Function — Only $\overline{CS}$ signal needs to be asserted at minimum rate.

at 100MHz Burst Length = 4 CAS Latency = 3



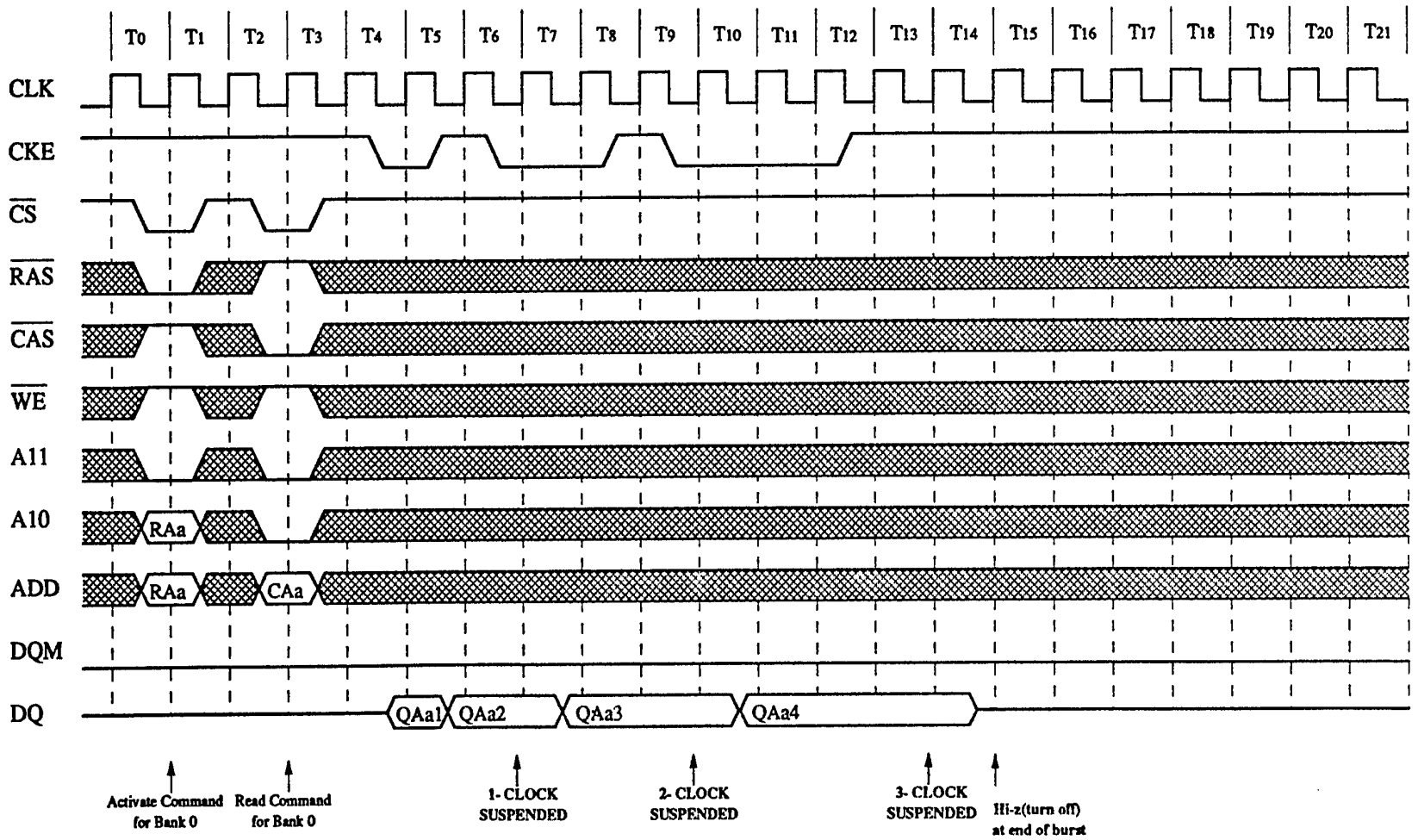
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 1



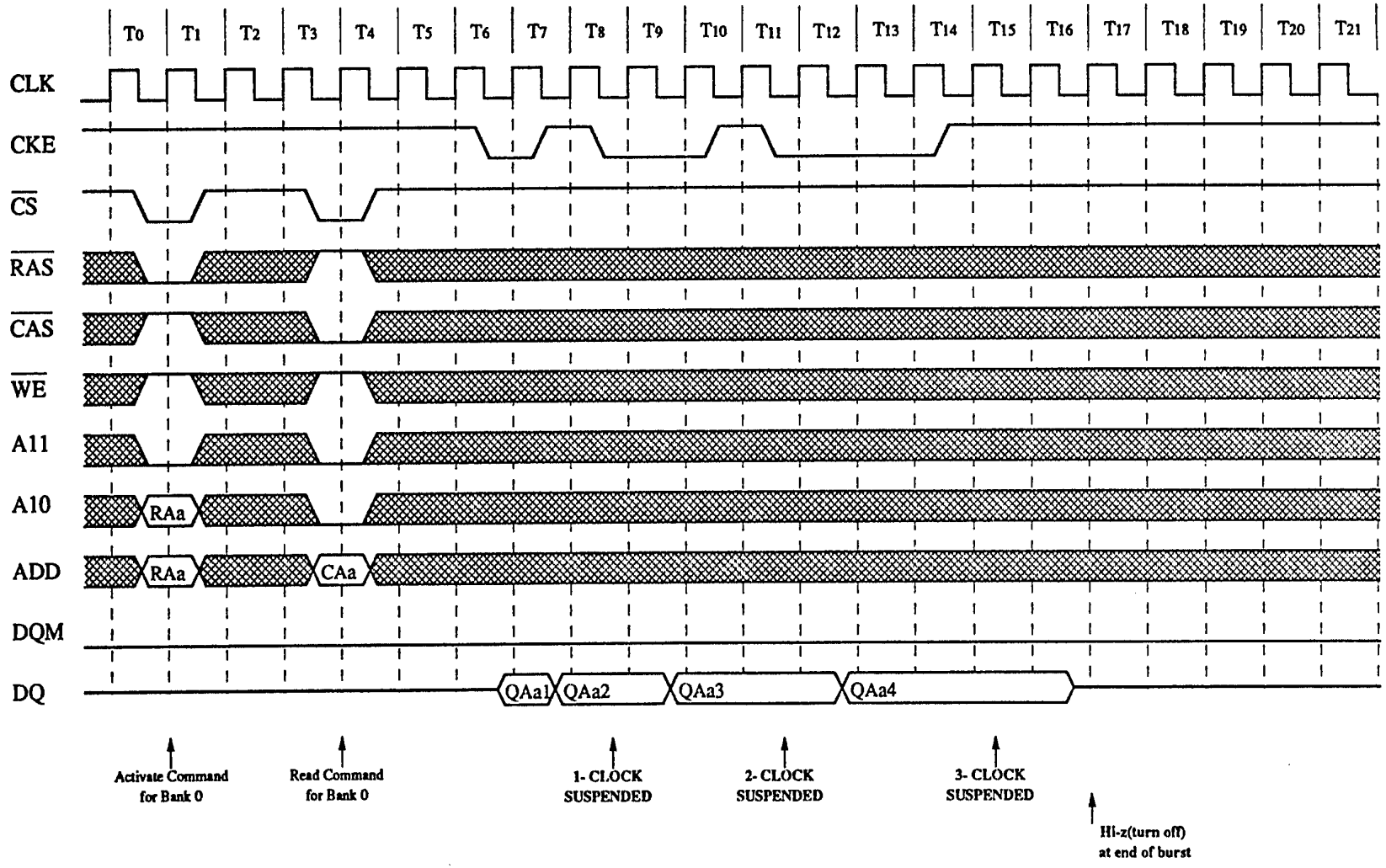
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 2



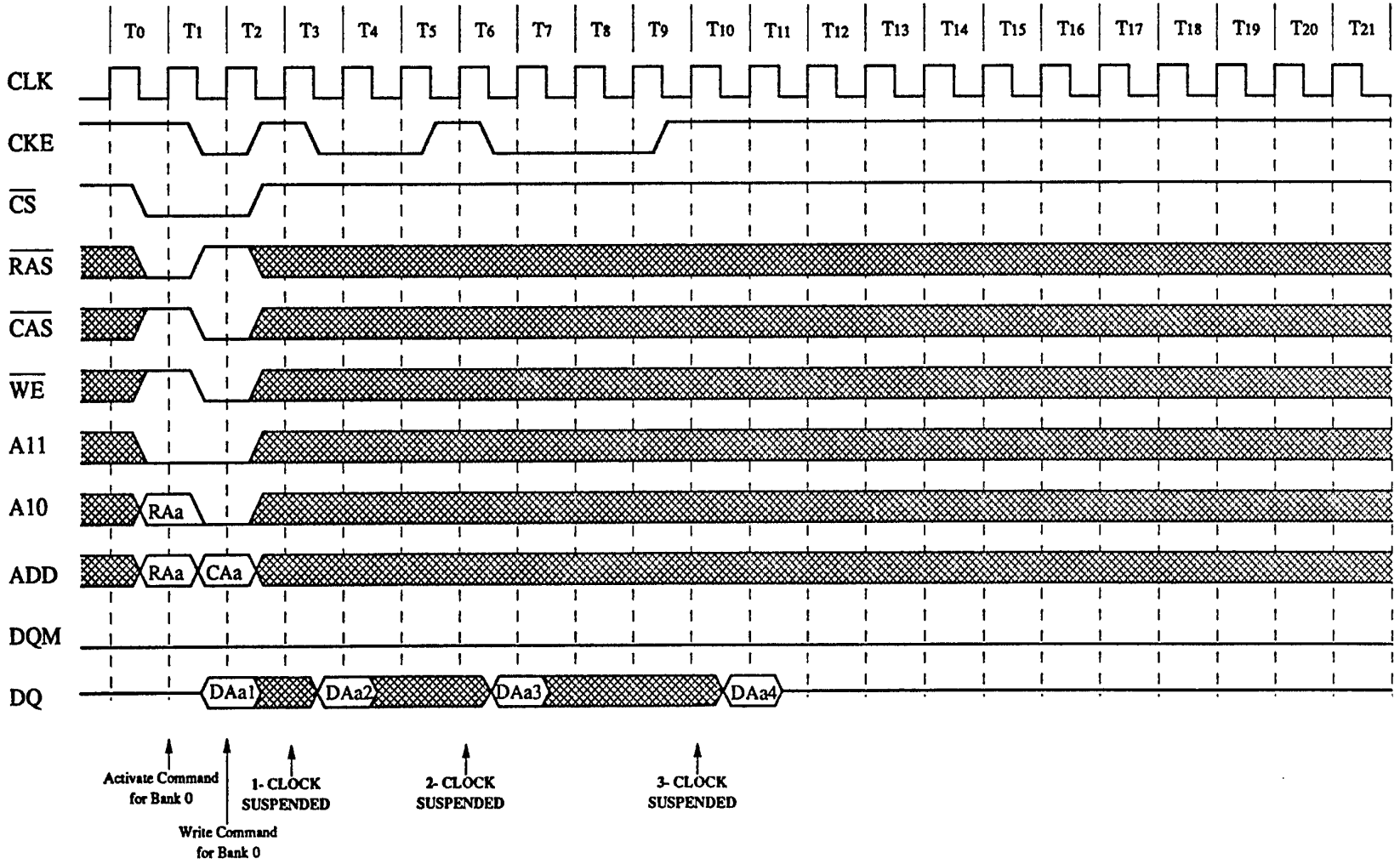
CLOCK SUSPENSION during BURST READ (using CKE Function)

Burst Length = 4 CAS Latency = 3



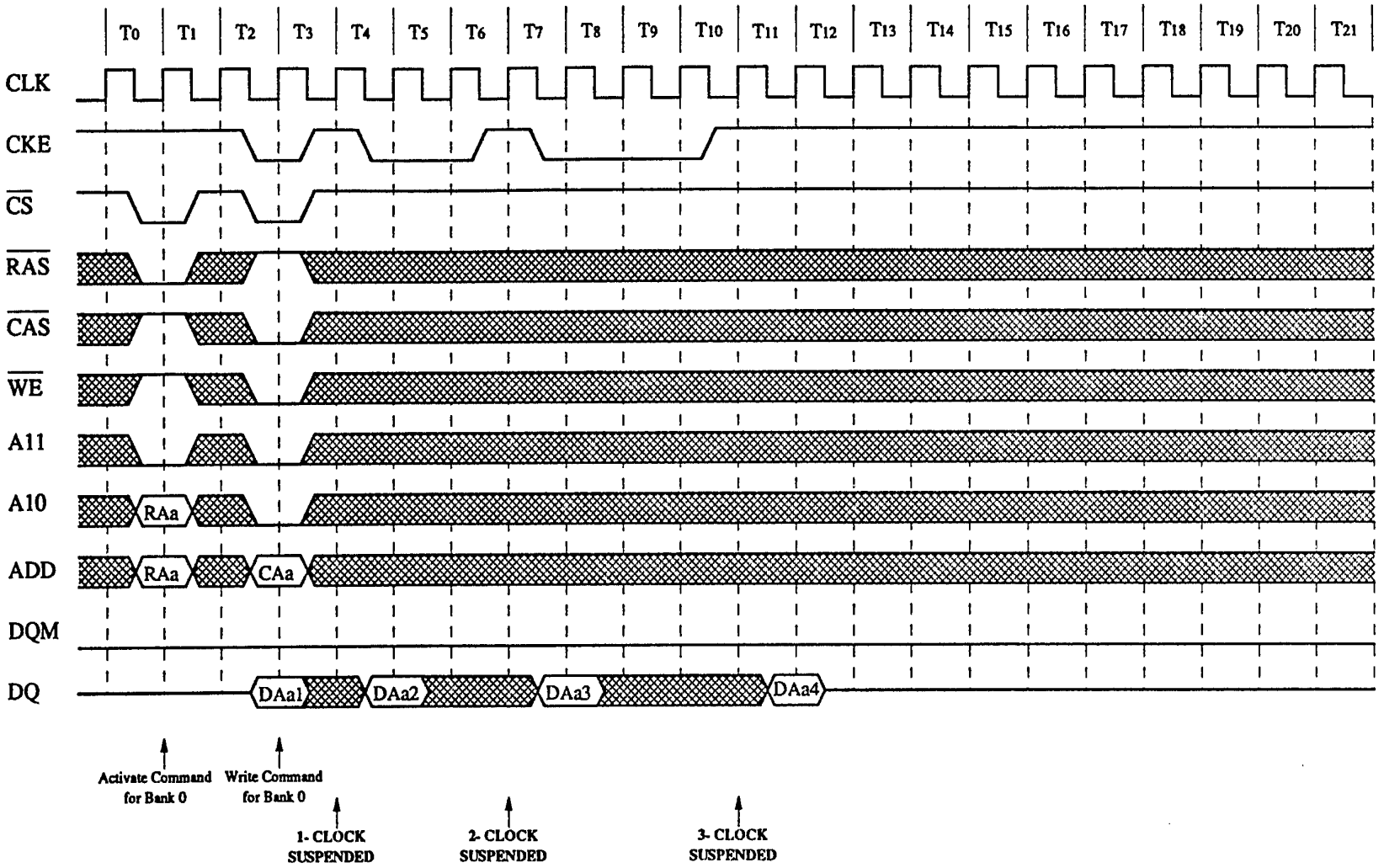
CLOCK SUSPENSION during BURST WRITE (using CKE Function)

Burst Length = 4 CAS Latency = 1



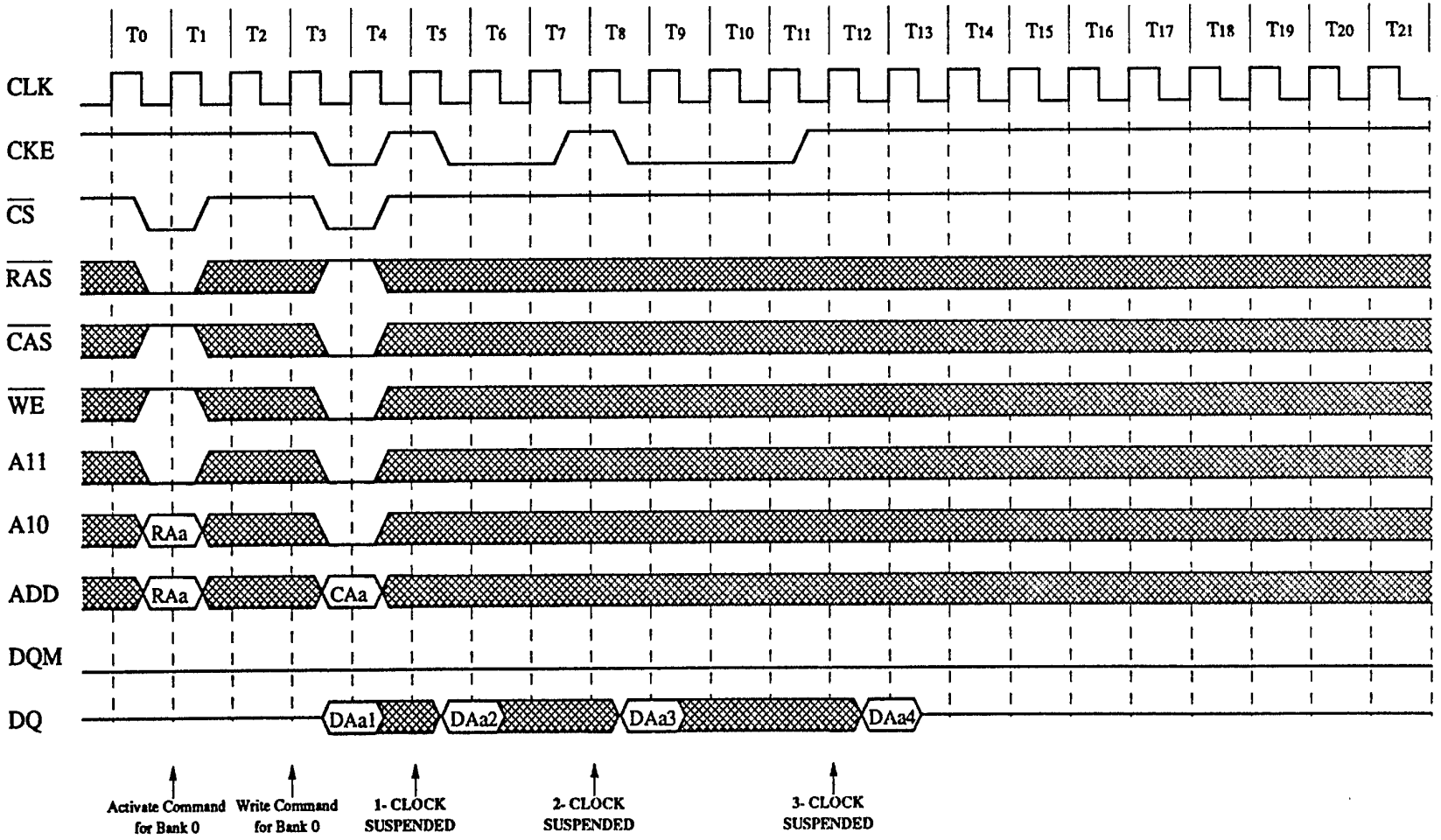
CLOCK SUSPENSION during BURST WRITE (using CKE Function)

Burst Length = 4 CAS Latency = 2



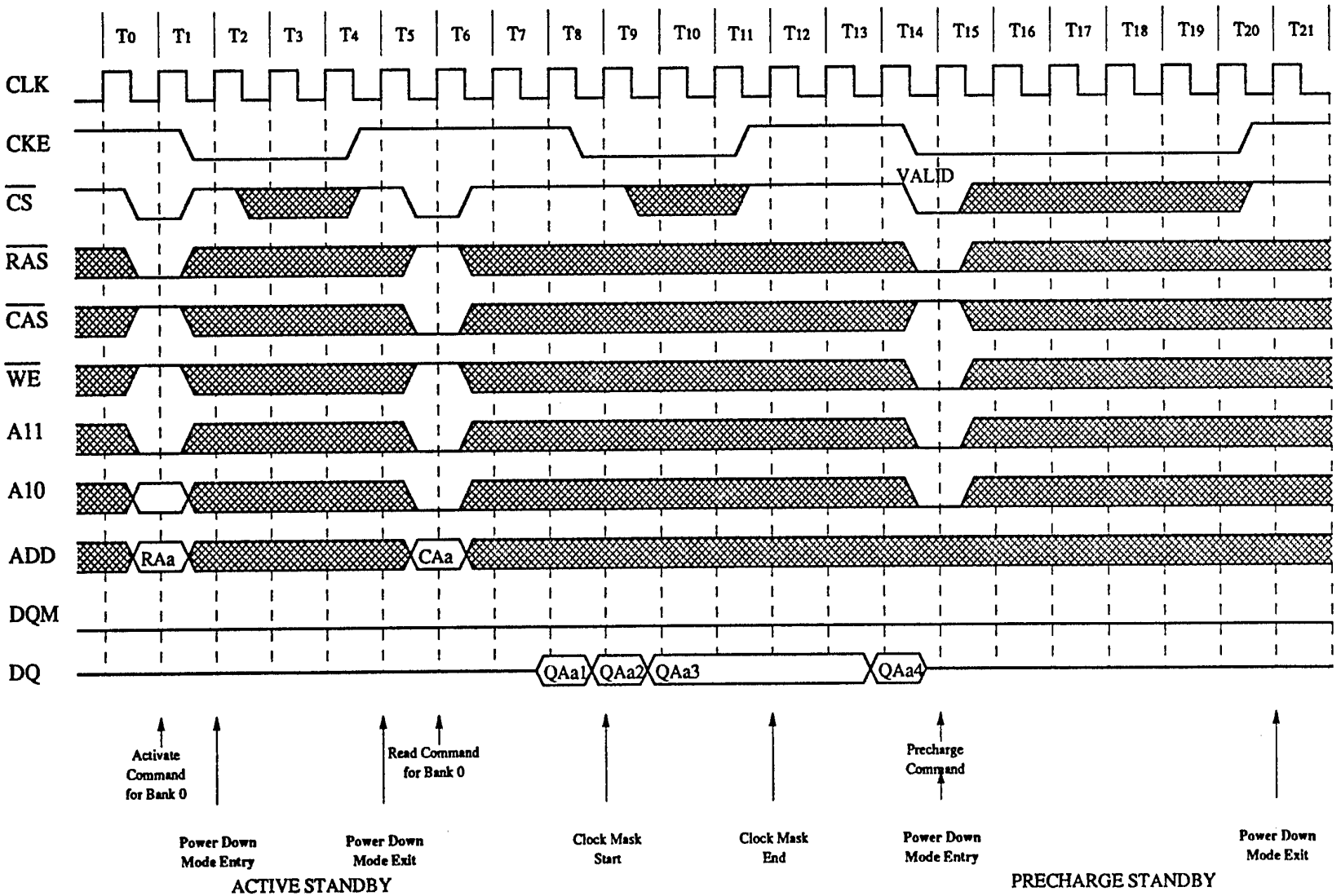
CLOCK SUSPENSION during BURST WRITE (using CKE Function)

Burst Length = 4 CAS Latency = 3

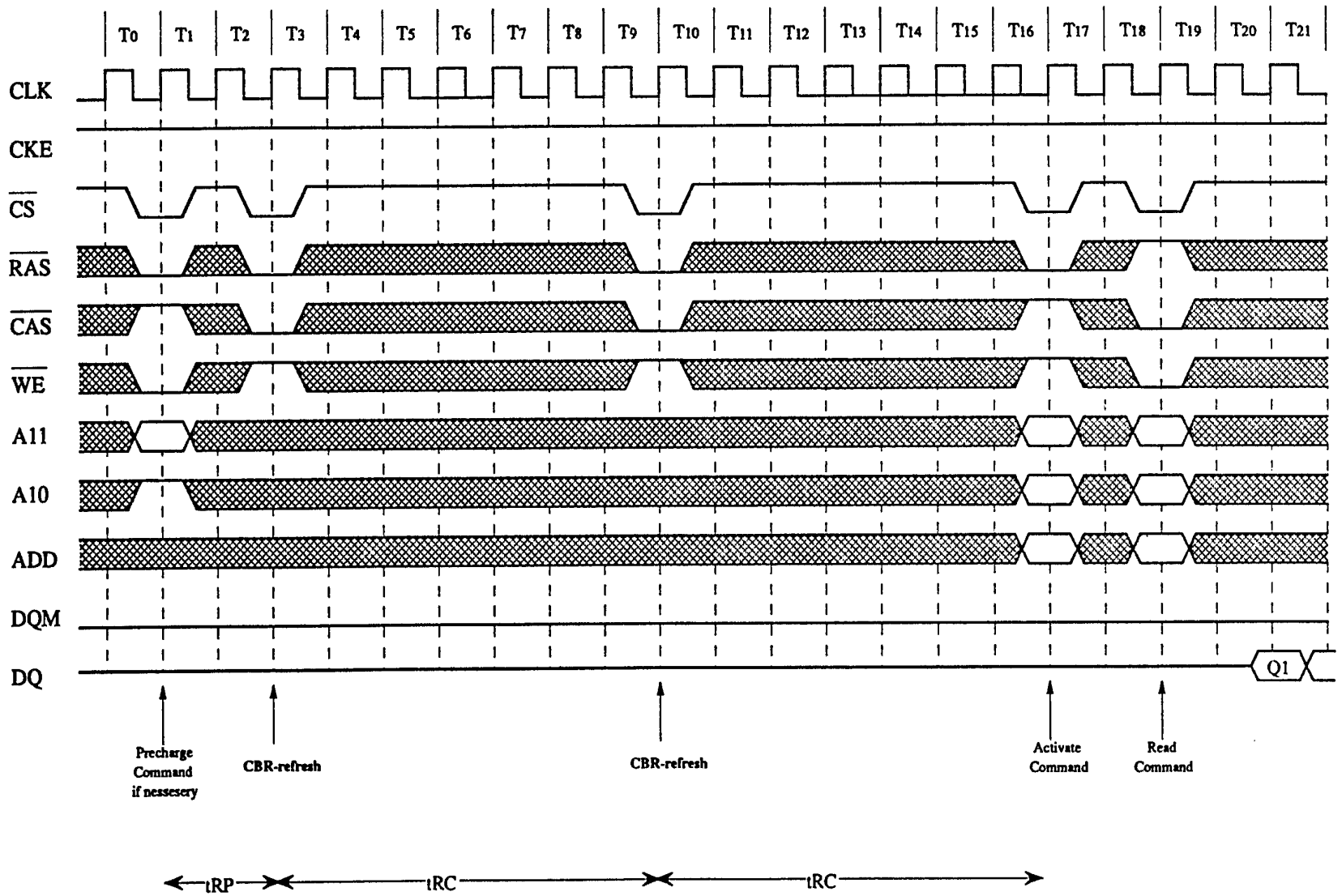


Power Down Mode and Clock Mask

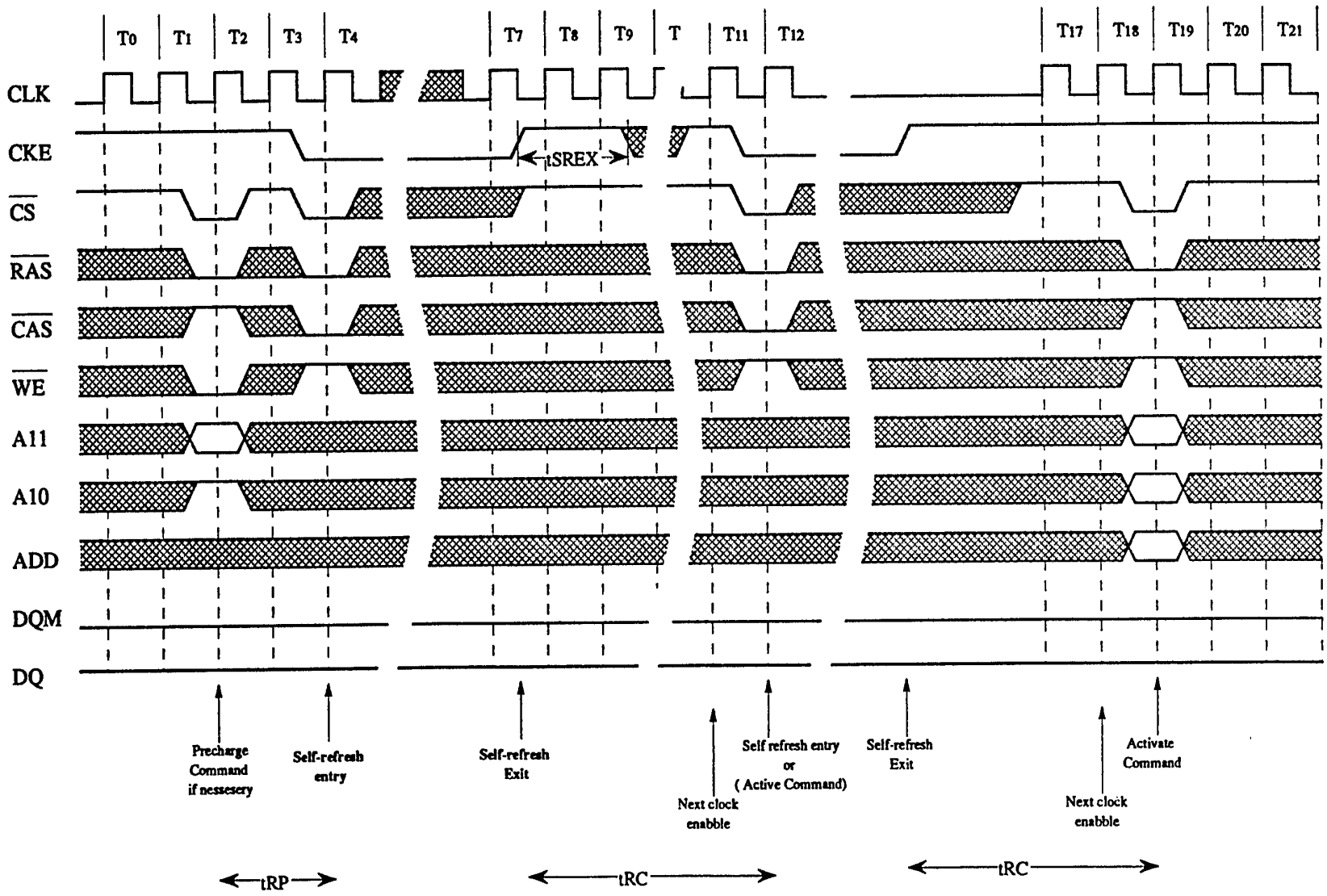
Burst Length = 4 CAS Latency = 2



CBR Refresh

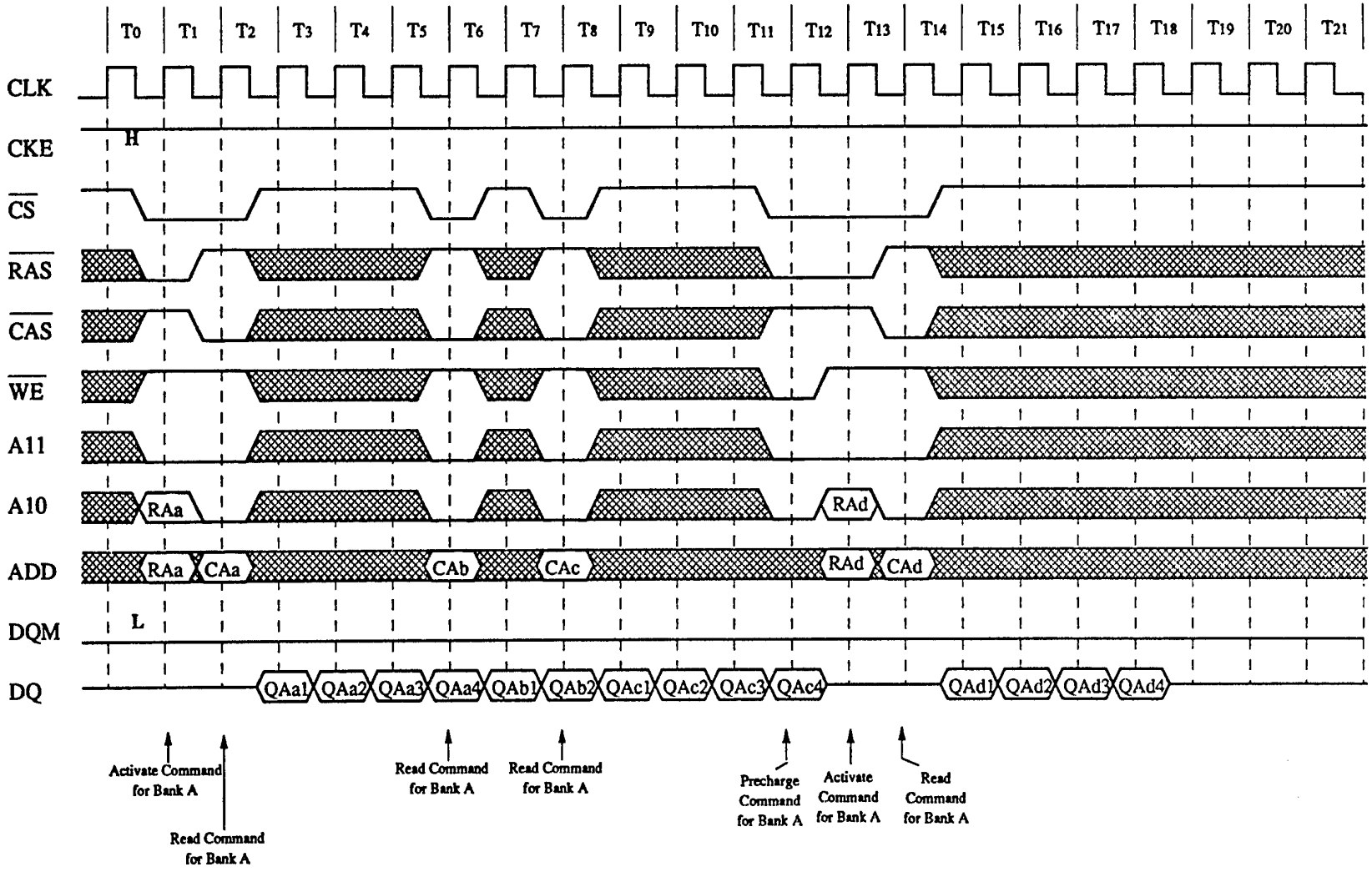


Self Refresh (entry&exit)



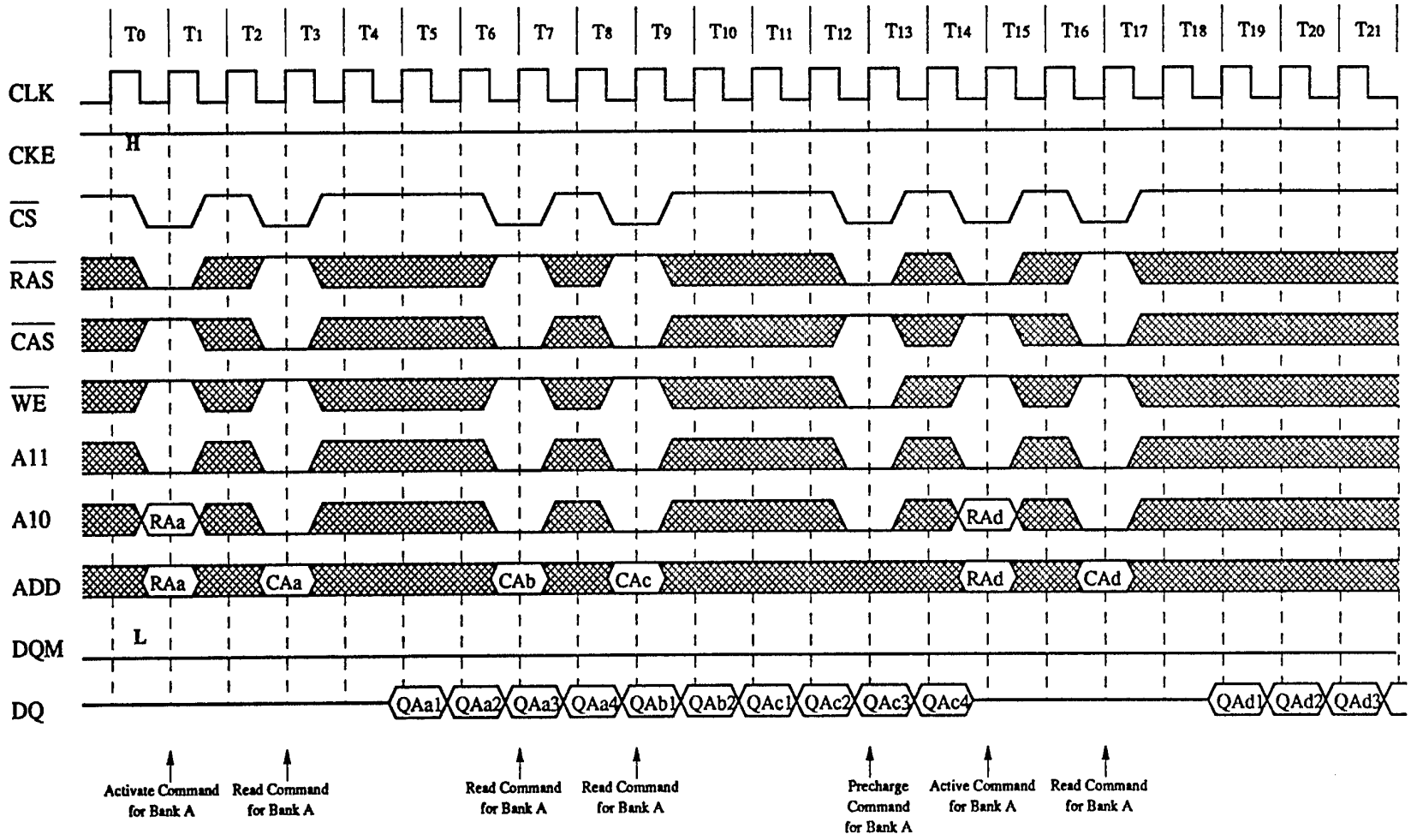
Random Column Read
(page with same bank)

Burst Length= 4 CAS Latency = 1



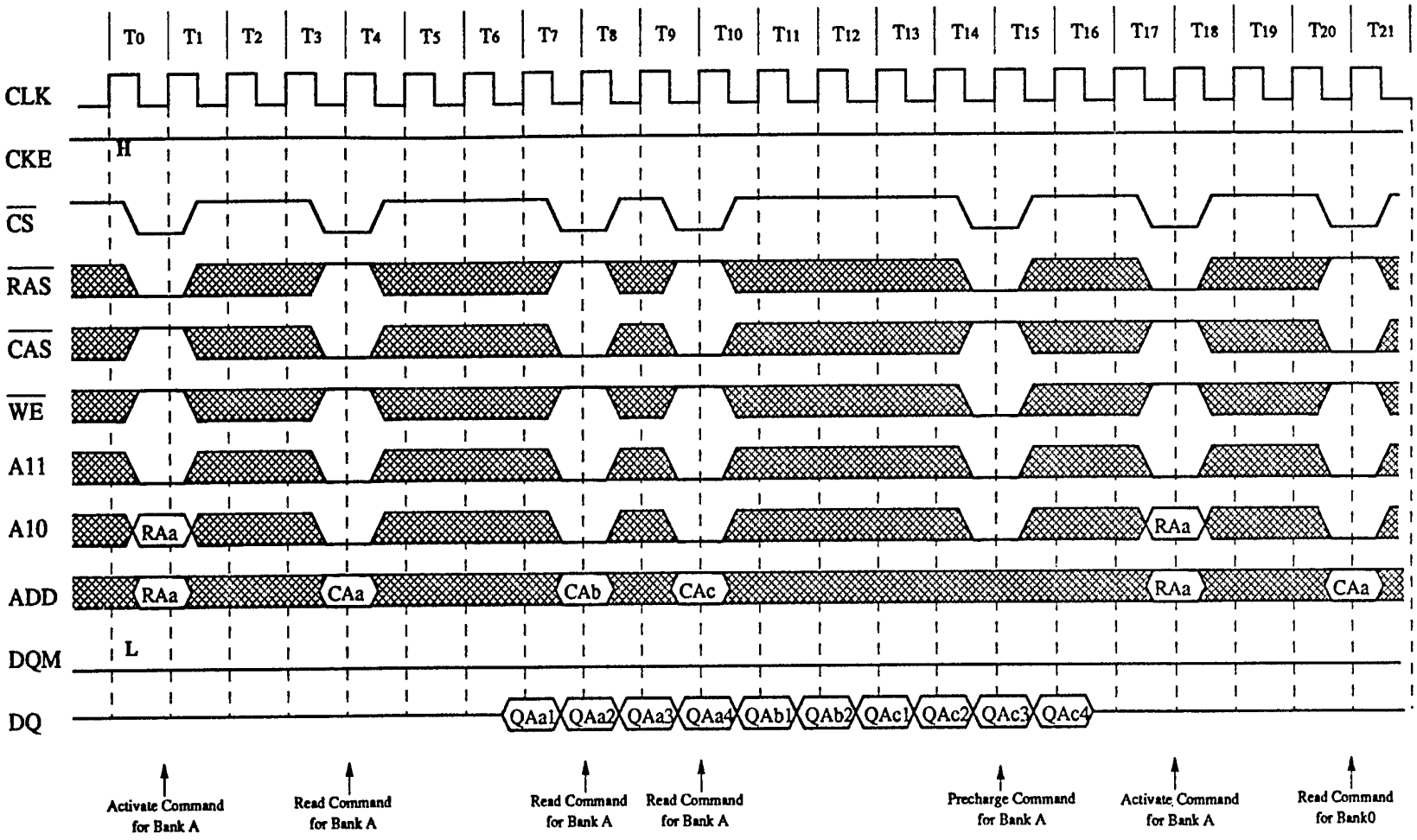
Random Column Read
(page with same bank)

Burst Length = 4 CAS Latency = 2



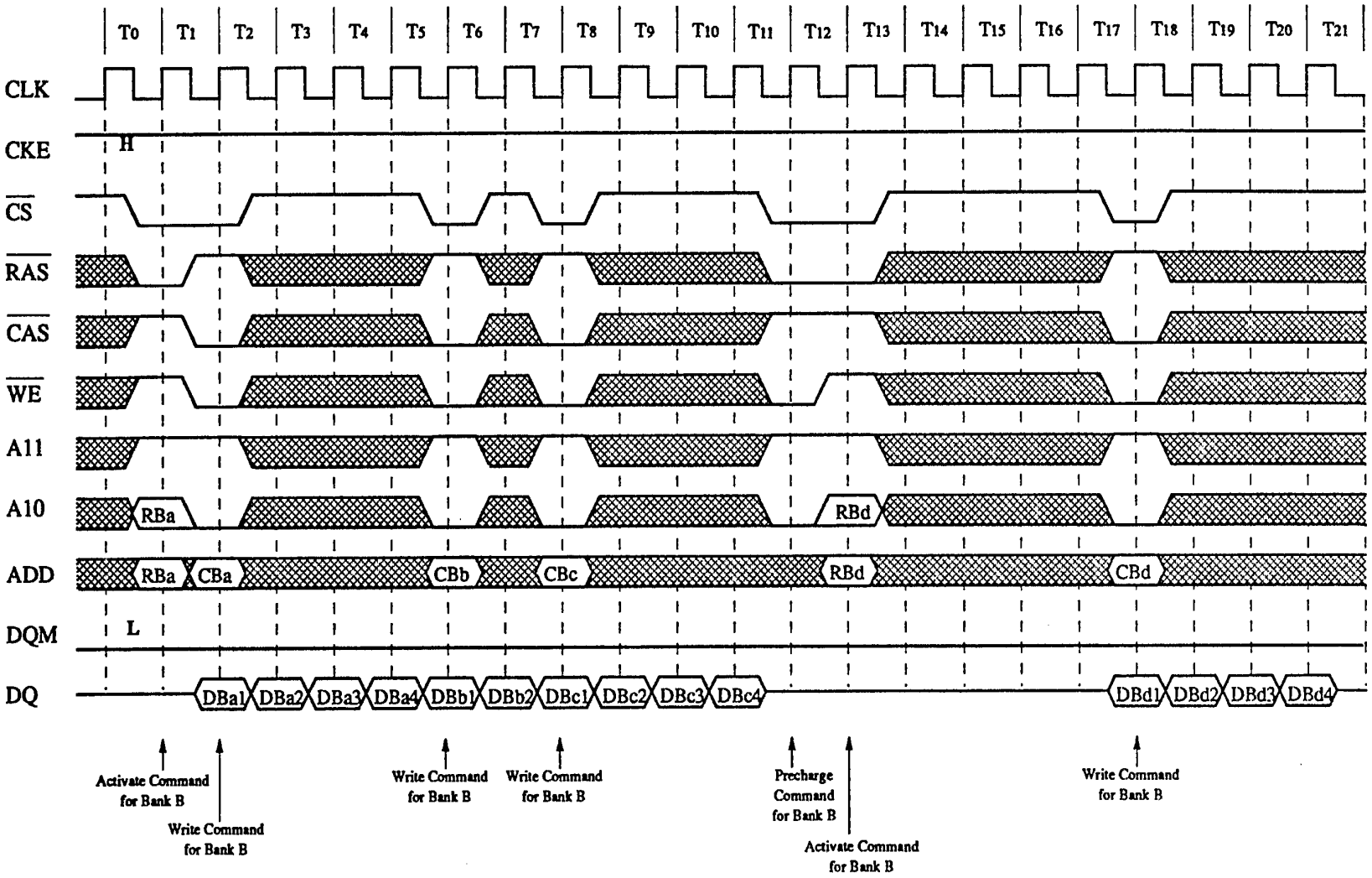
Random Column Read
(page with same bank)

Burst Length= 4 CAS Latency = 3



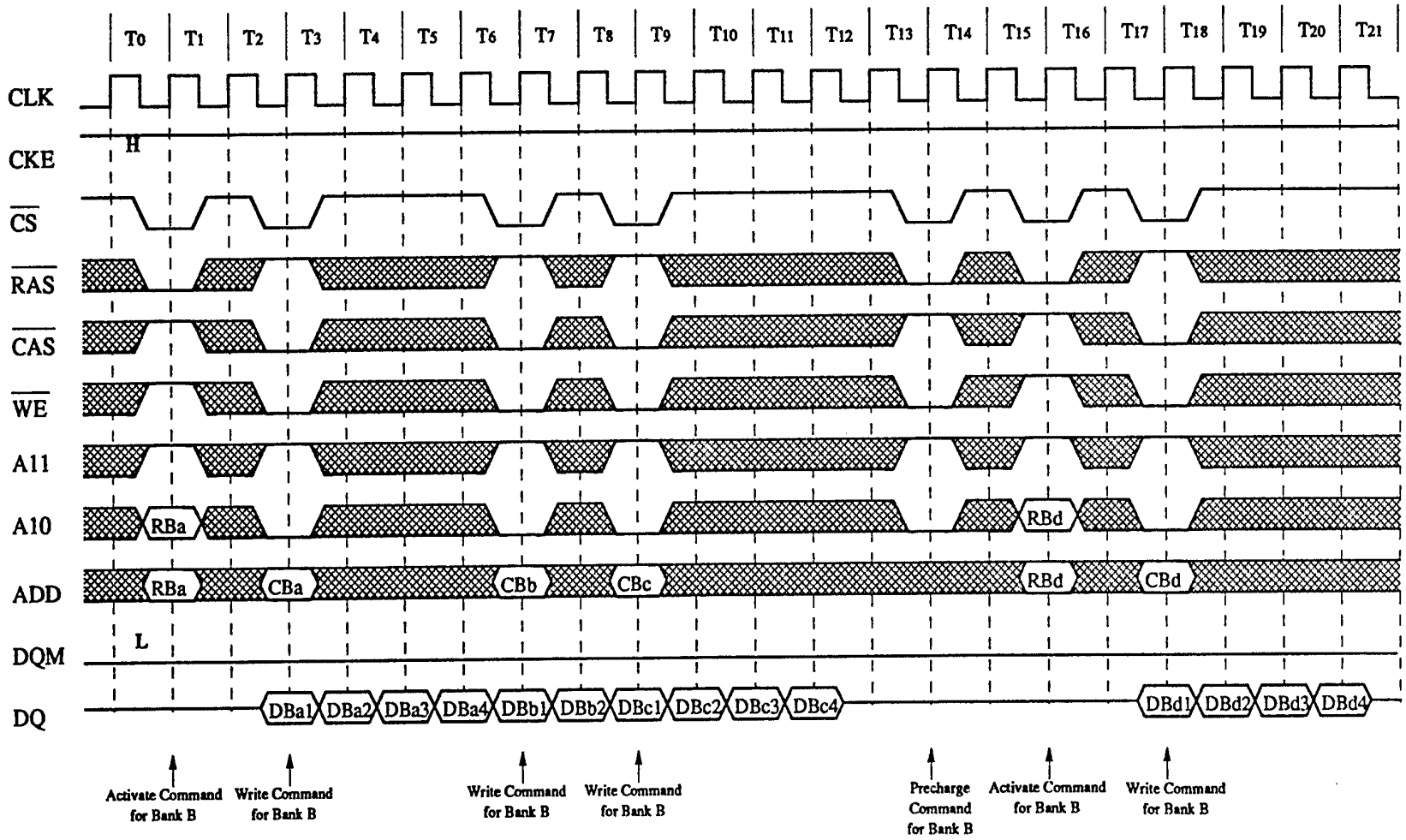
Random Column Write
(page with same bank)

Burst Length= 4 CAS Latency = 1



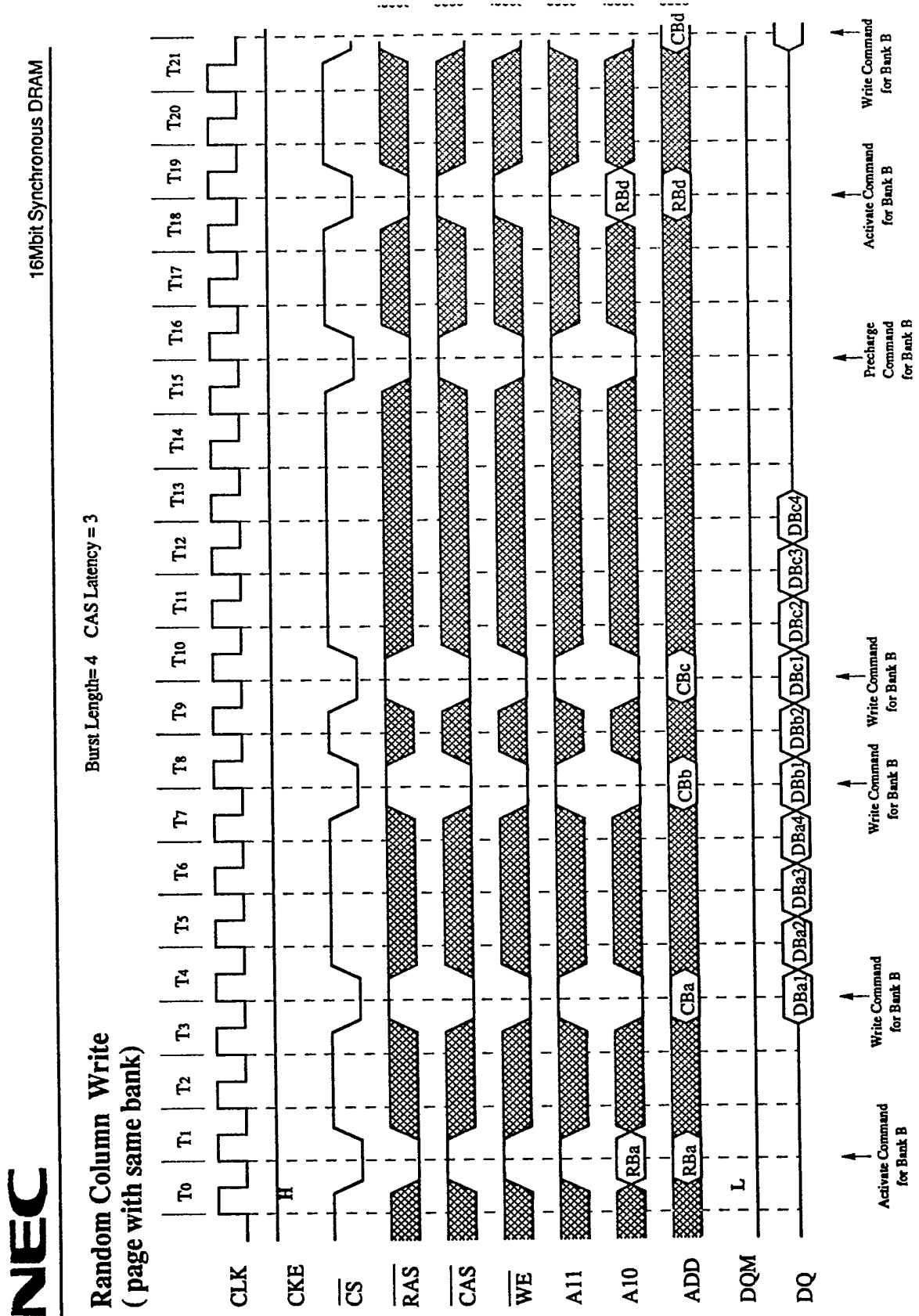
Random Column Write
(page with same bank)

Burst Length = 4 CAS Latency = 2



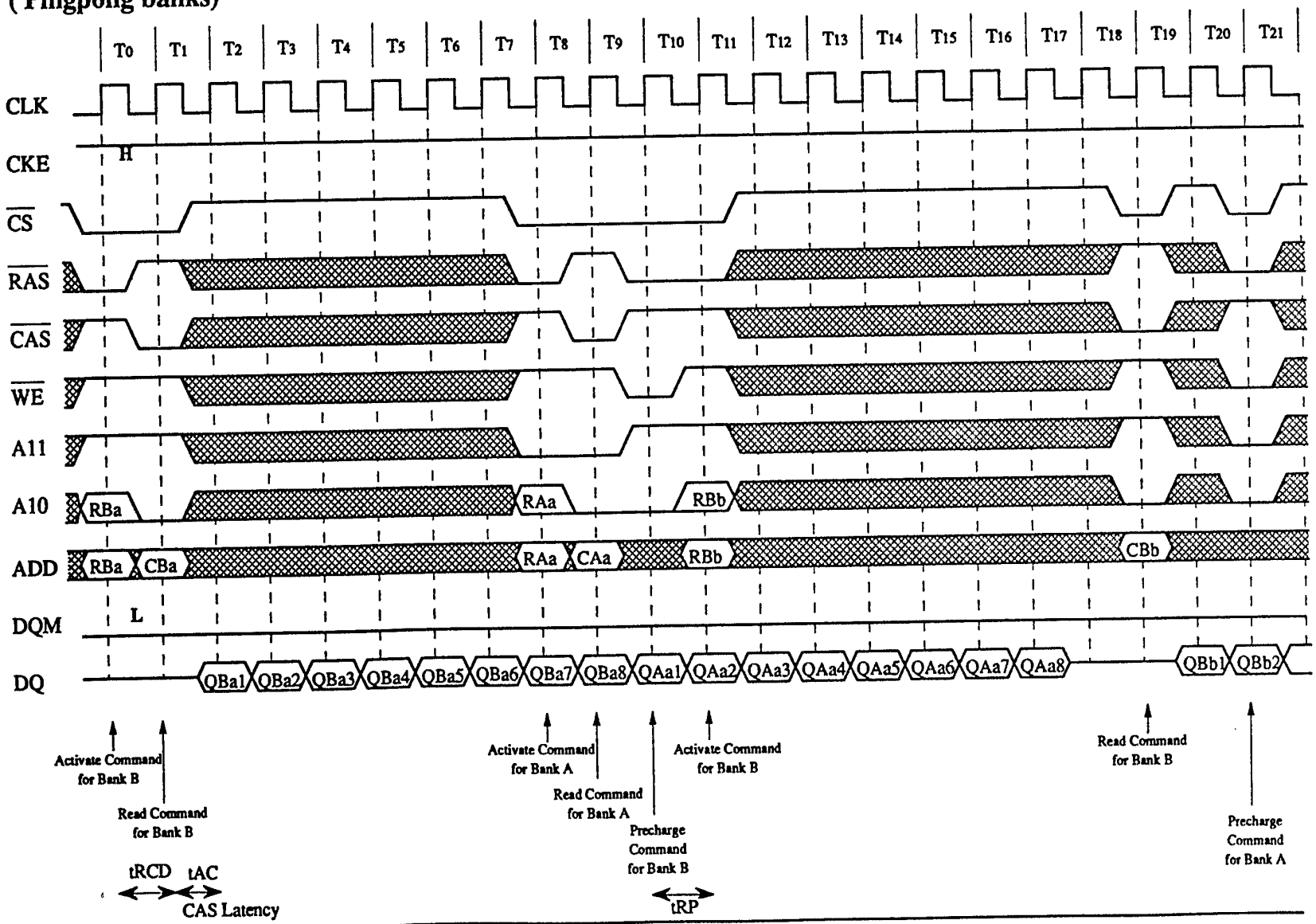
Random Column Write (page with same bank)

Burst Length= 4 CAS Latency = 3



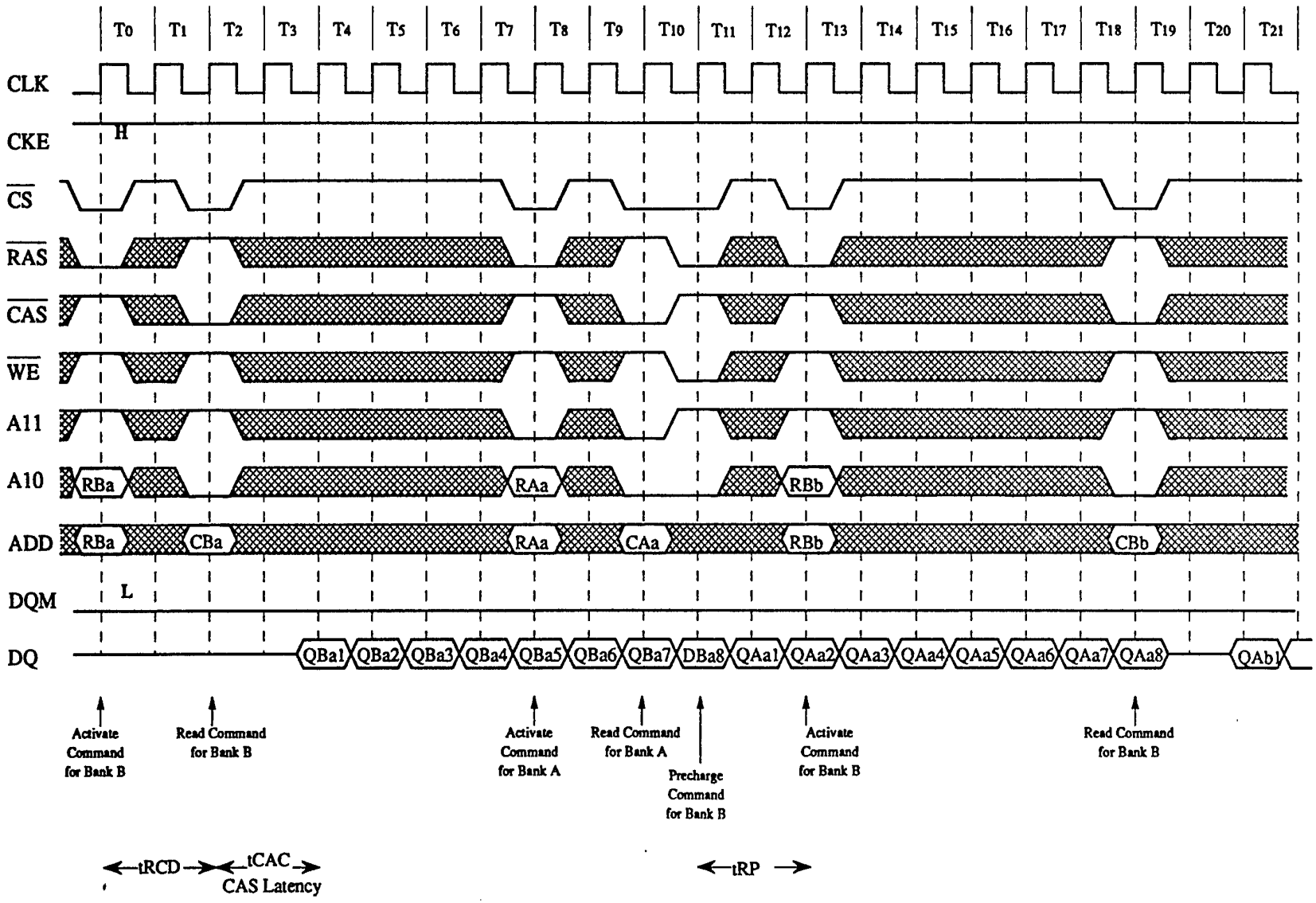
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 1



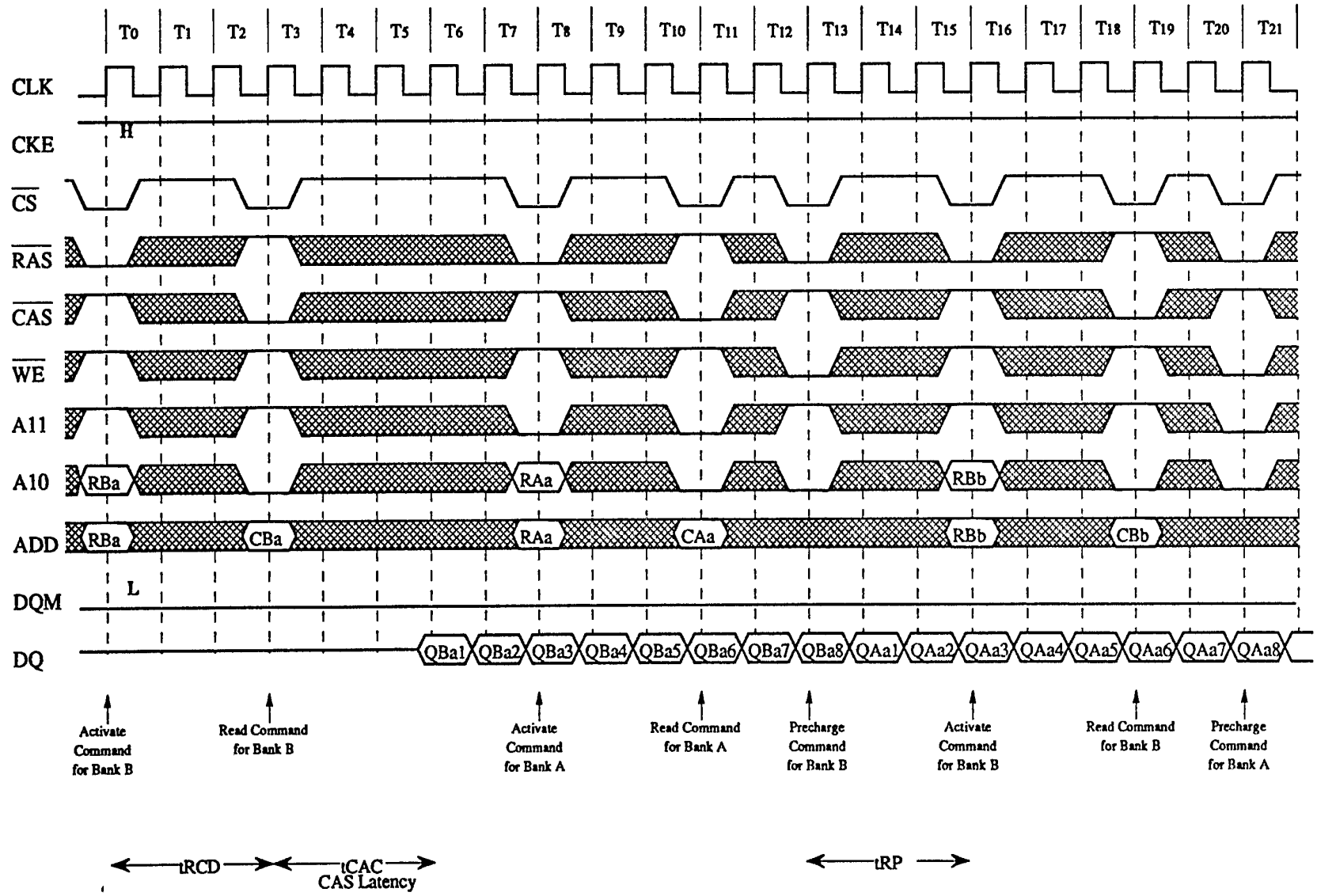
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 2



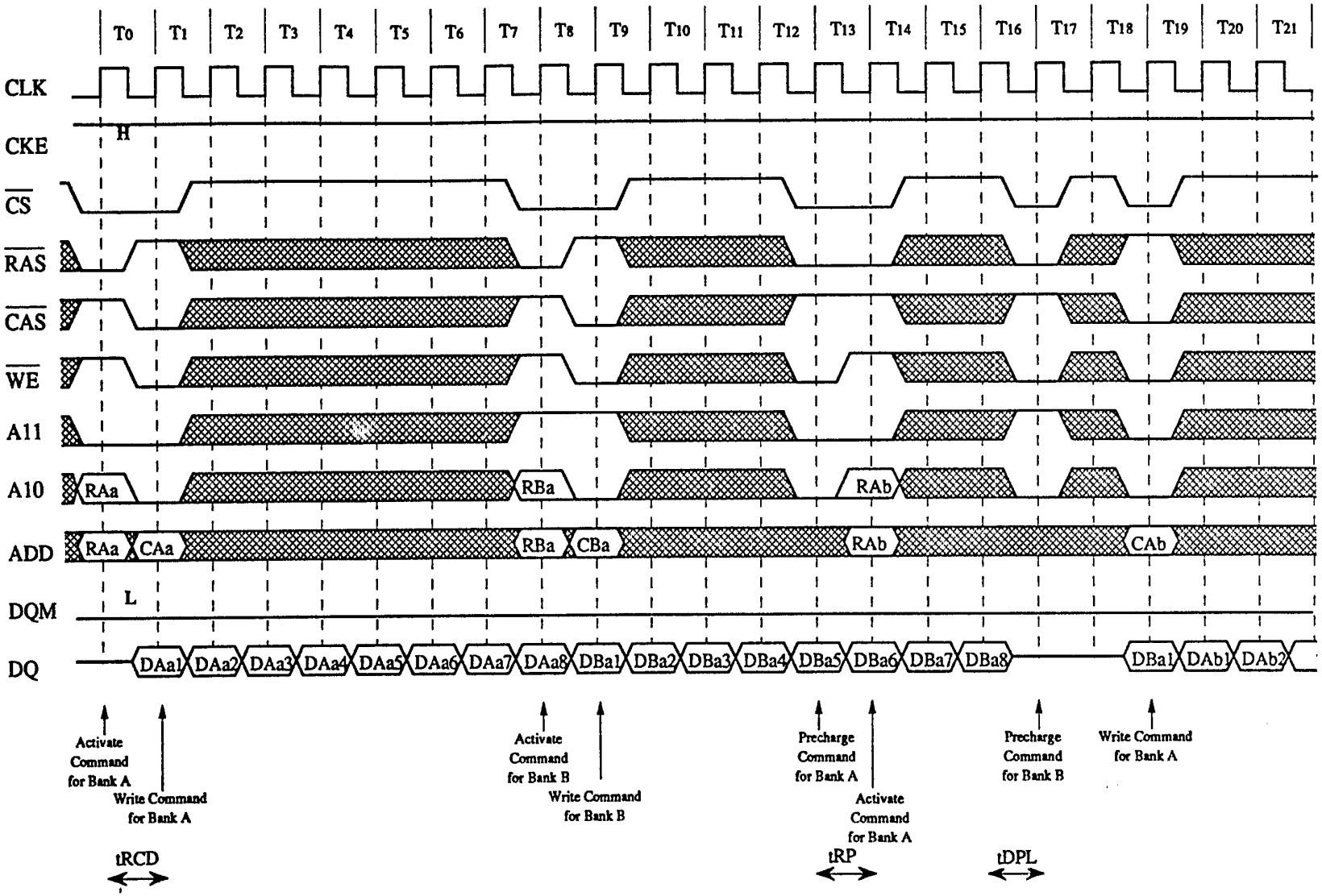
Random Row READ
(Pingpong banks)

Burst Length = 8 CAS Latency = 3



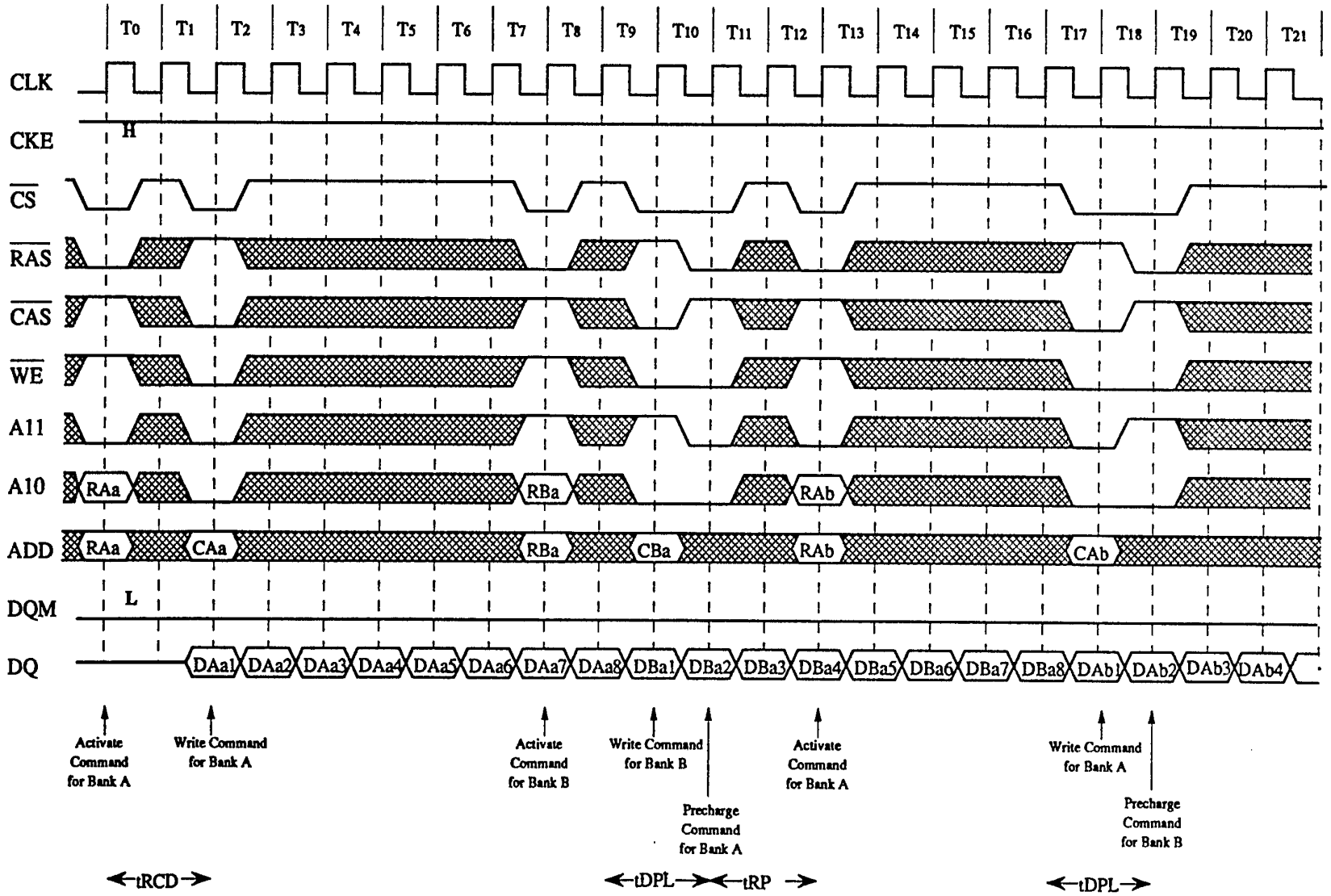
Random Row Write
(Pingpong banks)

Burst Length = 8 CAS Latency = 1



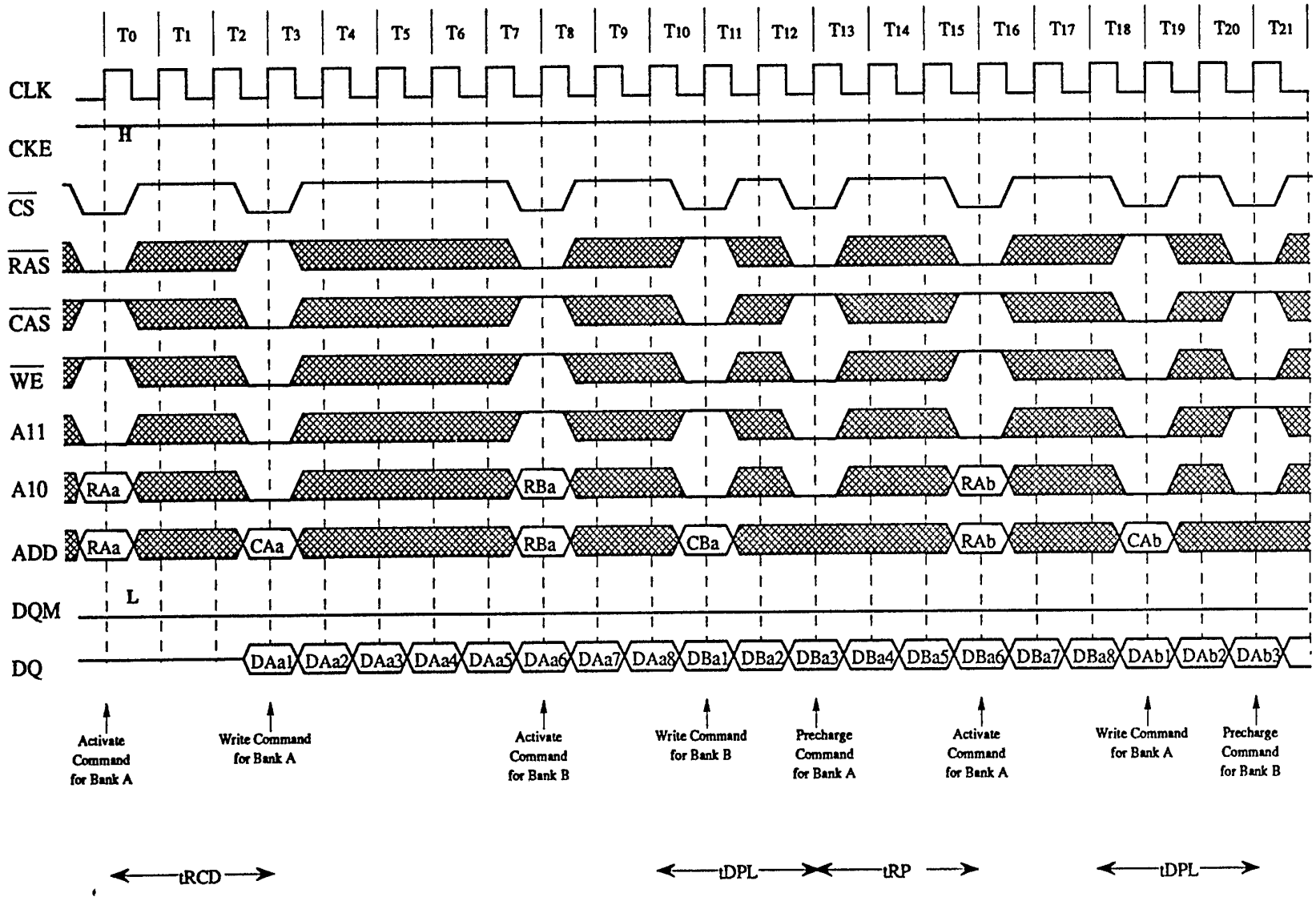
Random Row Write
(Pingpong banks)

Burst Length = 8 CAS Latency = 2



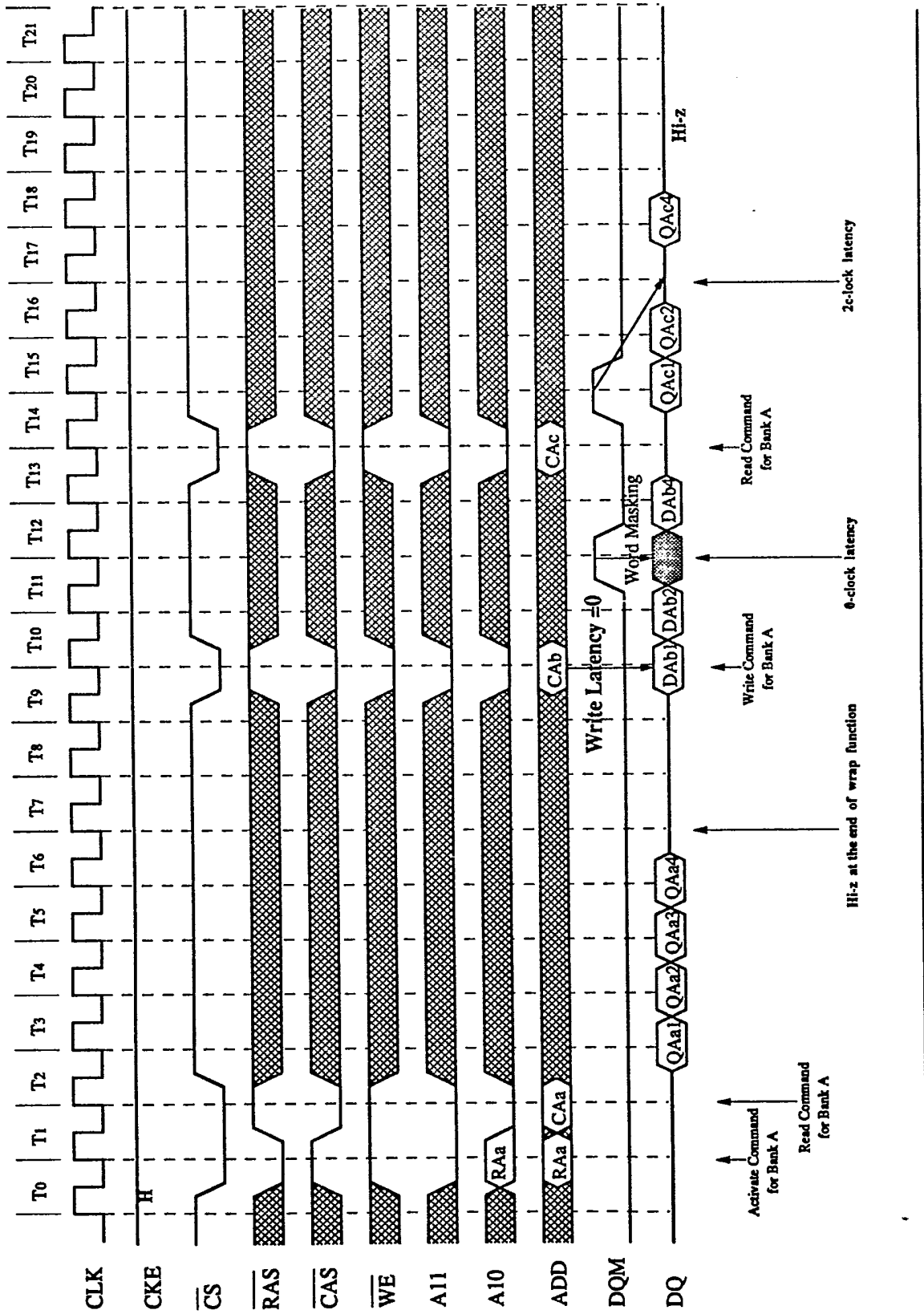
Random Row Write
(Pingpong banks)

Burst Length = 8 CAS Latency = 3



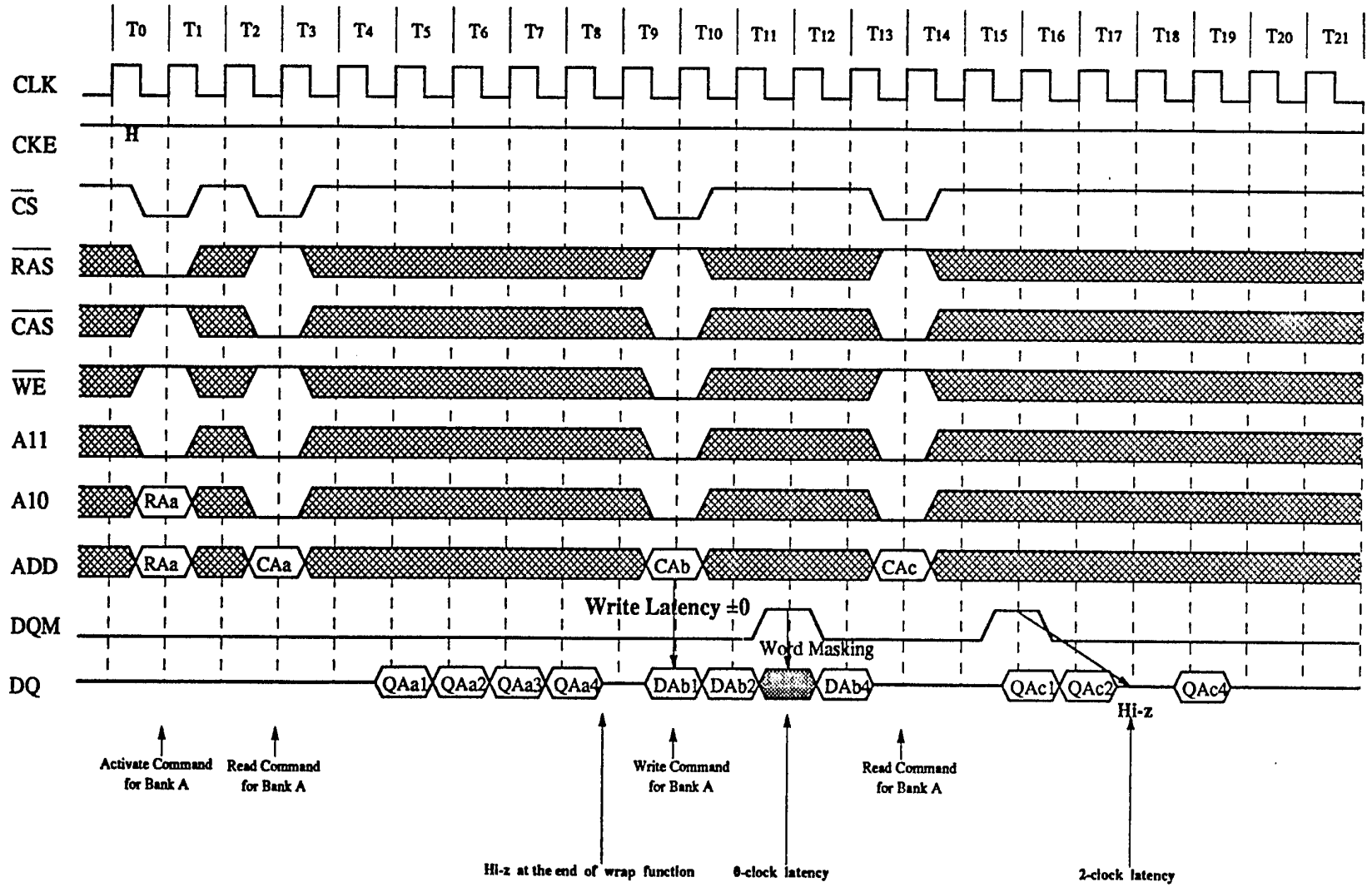
READ and WRITE

Burst Length = 4 CAS Latency = 1



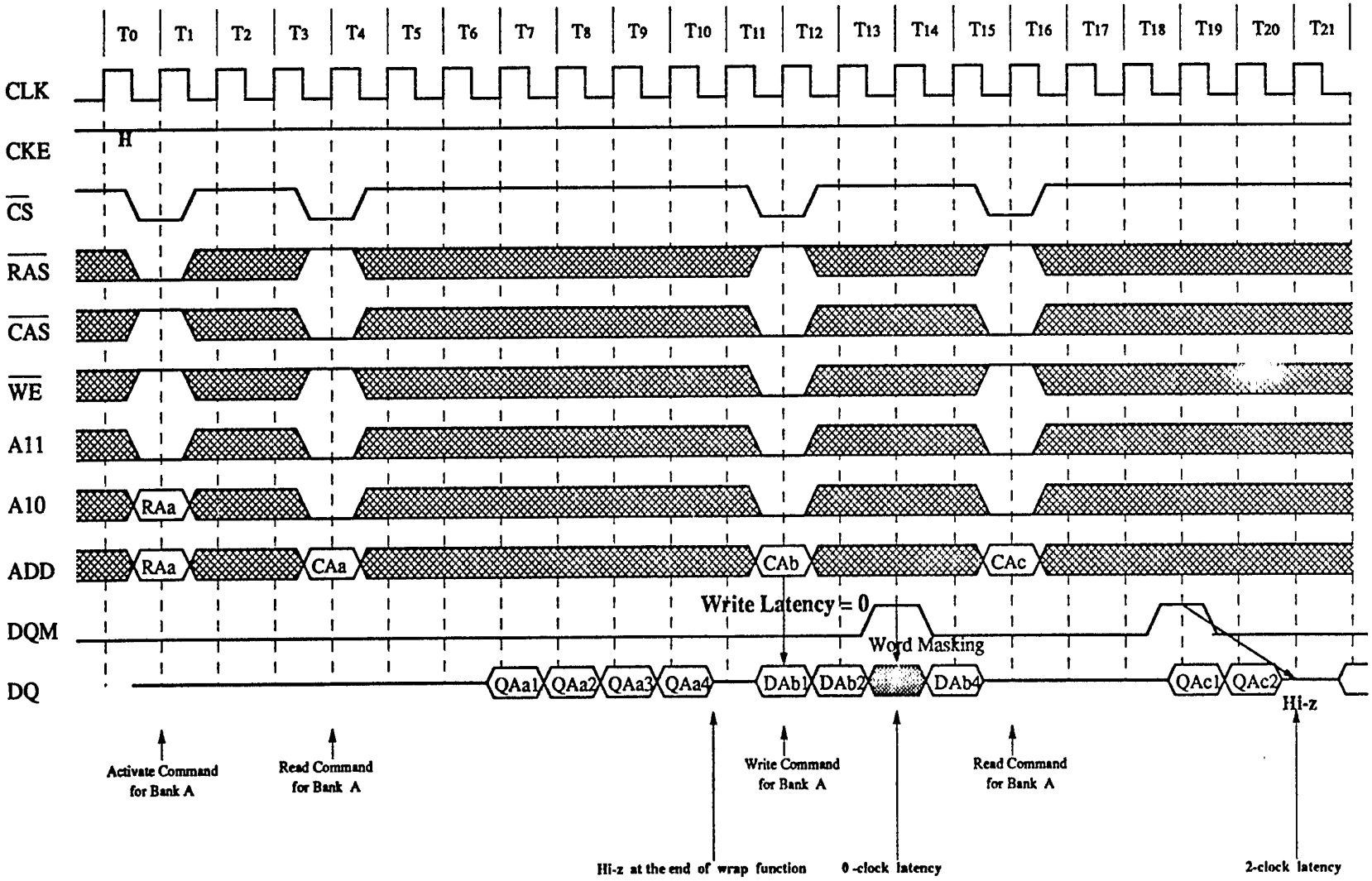
READ and WRITE

Burst Length = 4 CAS Latency = 2



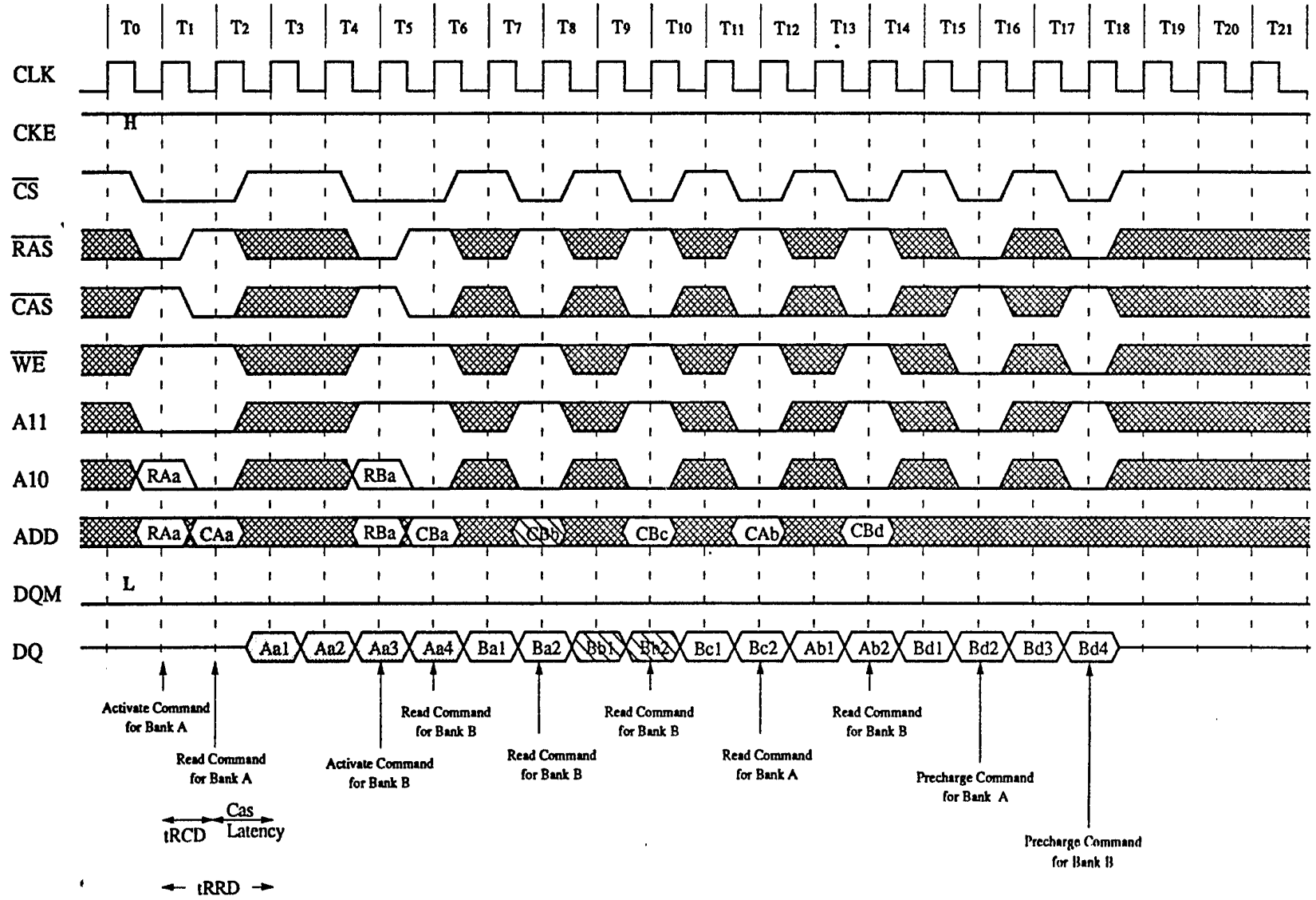
READ and WRITE

Burst Length = 4 CAS Latency = 3



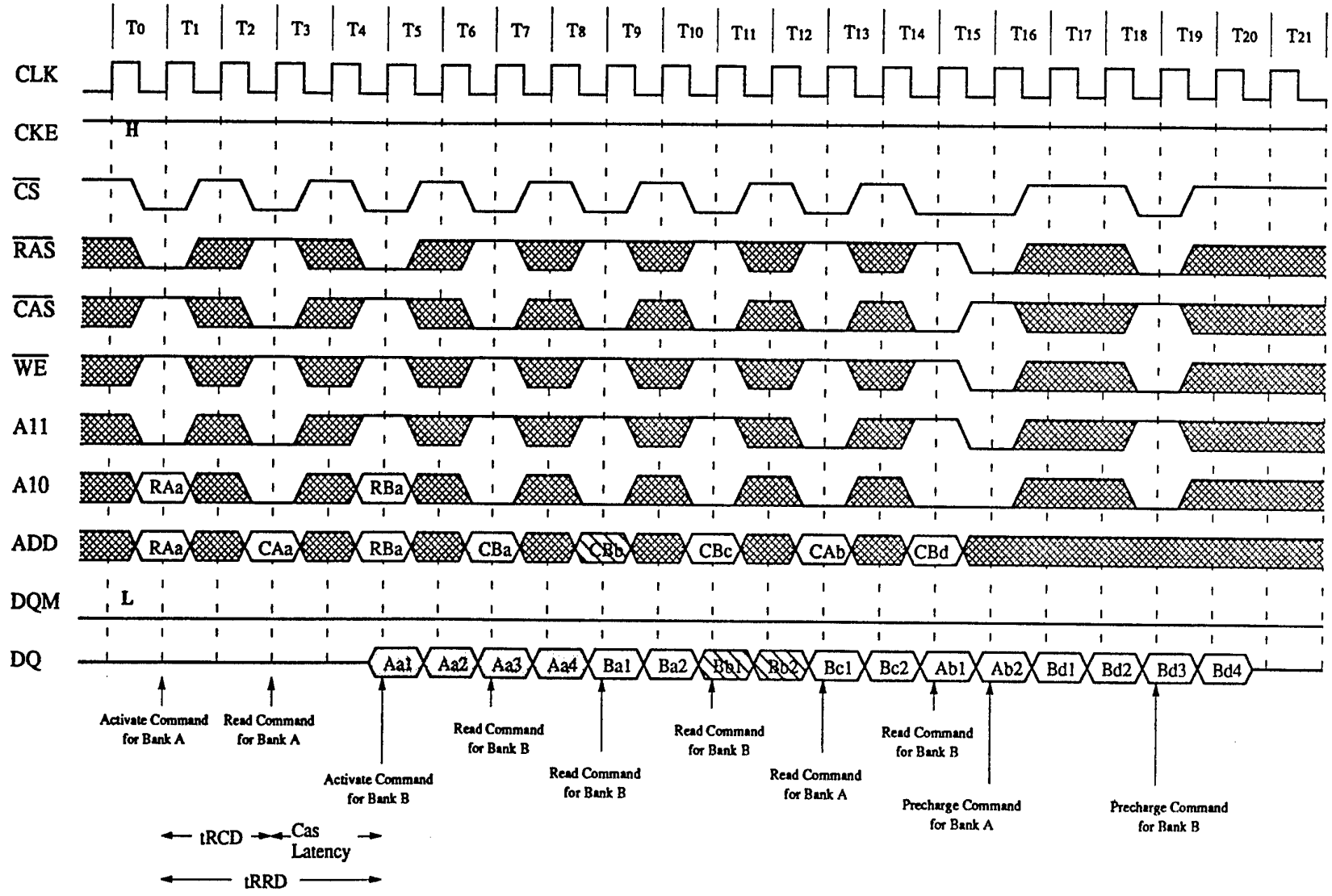
Interleaved Column READ CYCLE

Burst Length = 4 Cas Latency = 1



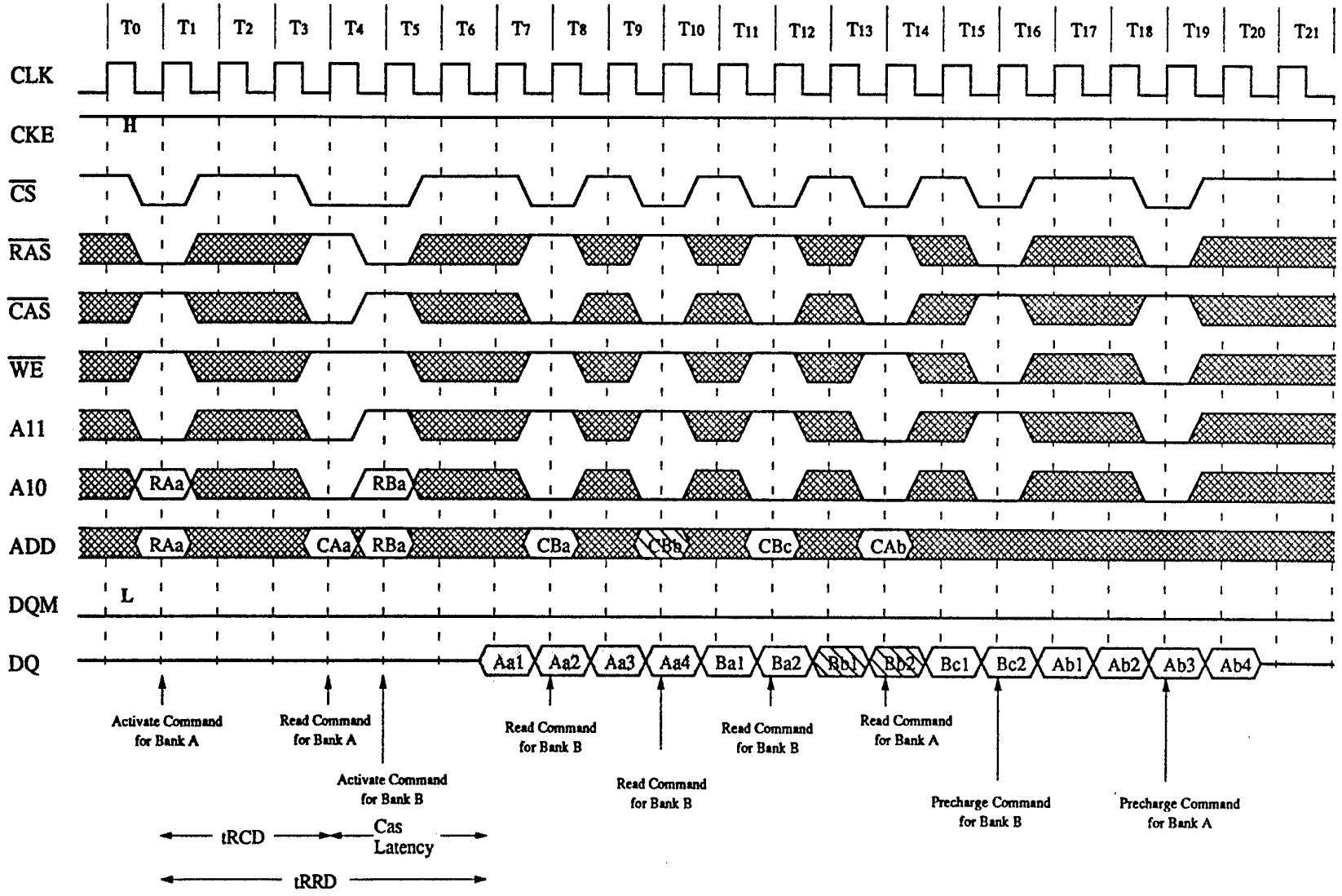
Interleaved Column READ CYCLE

Burst Length = 4 Cas Latency = 2



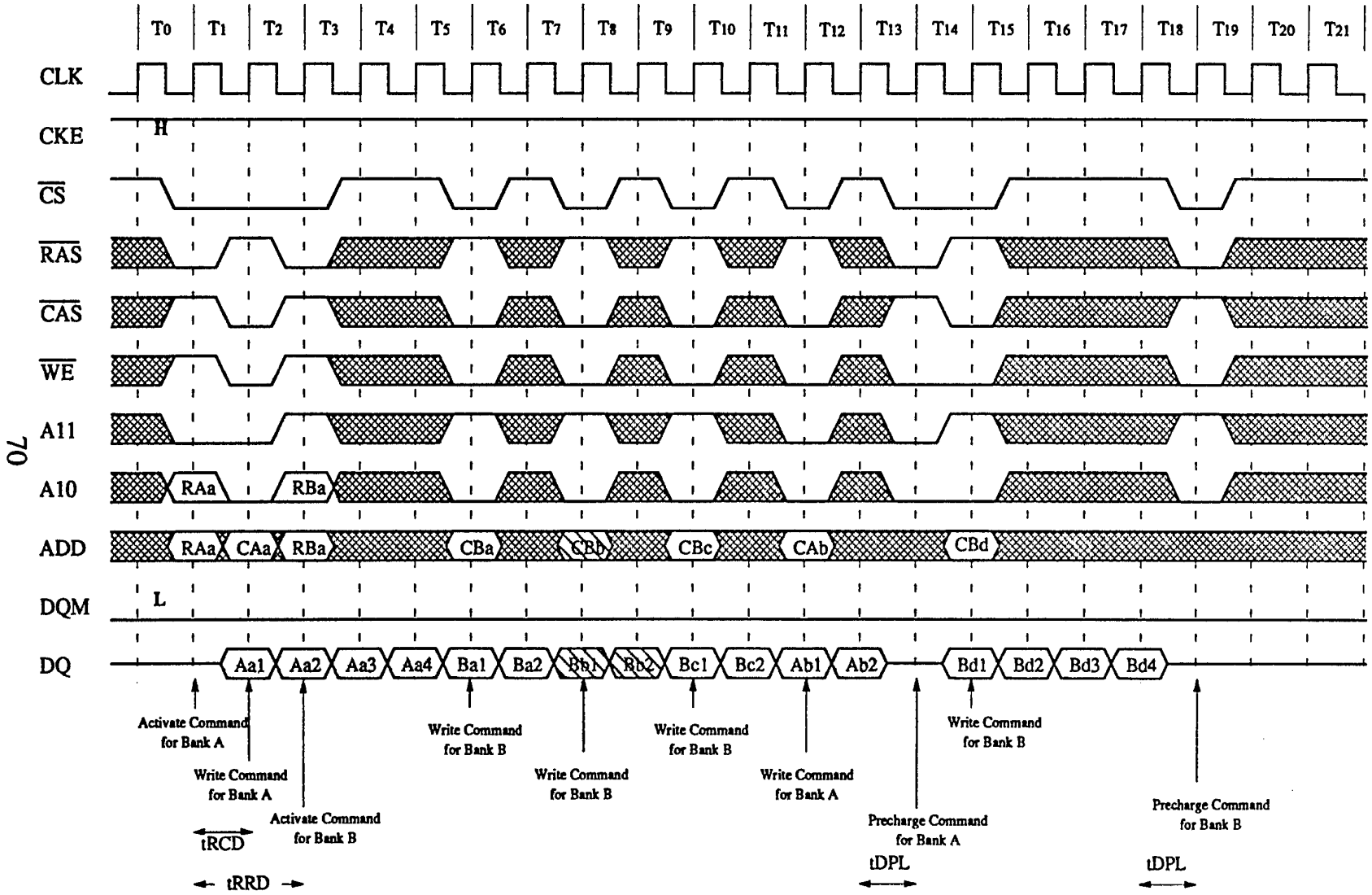
Interleaved Column READ CYCLE

Burst Length = 4 Cas Latency = 3



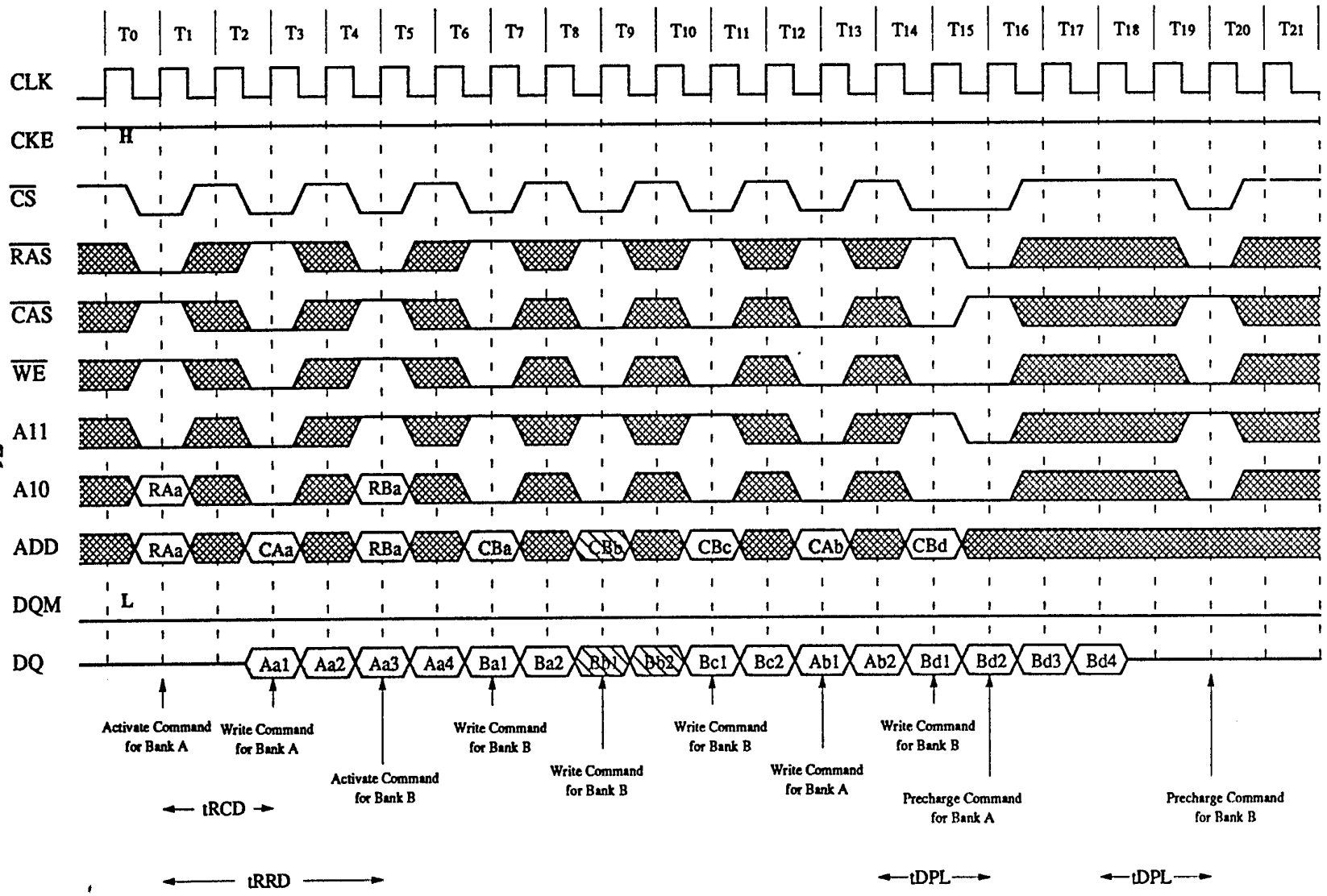
Interleaved Column WRITE CYCLE

Burst Length = 4 Cas Latency = 1



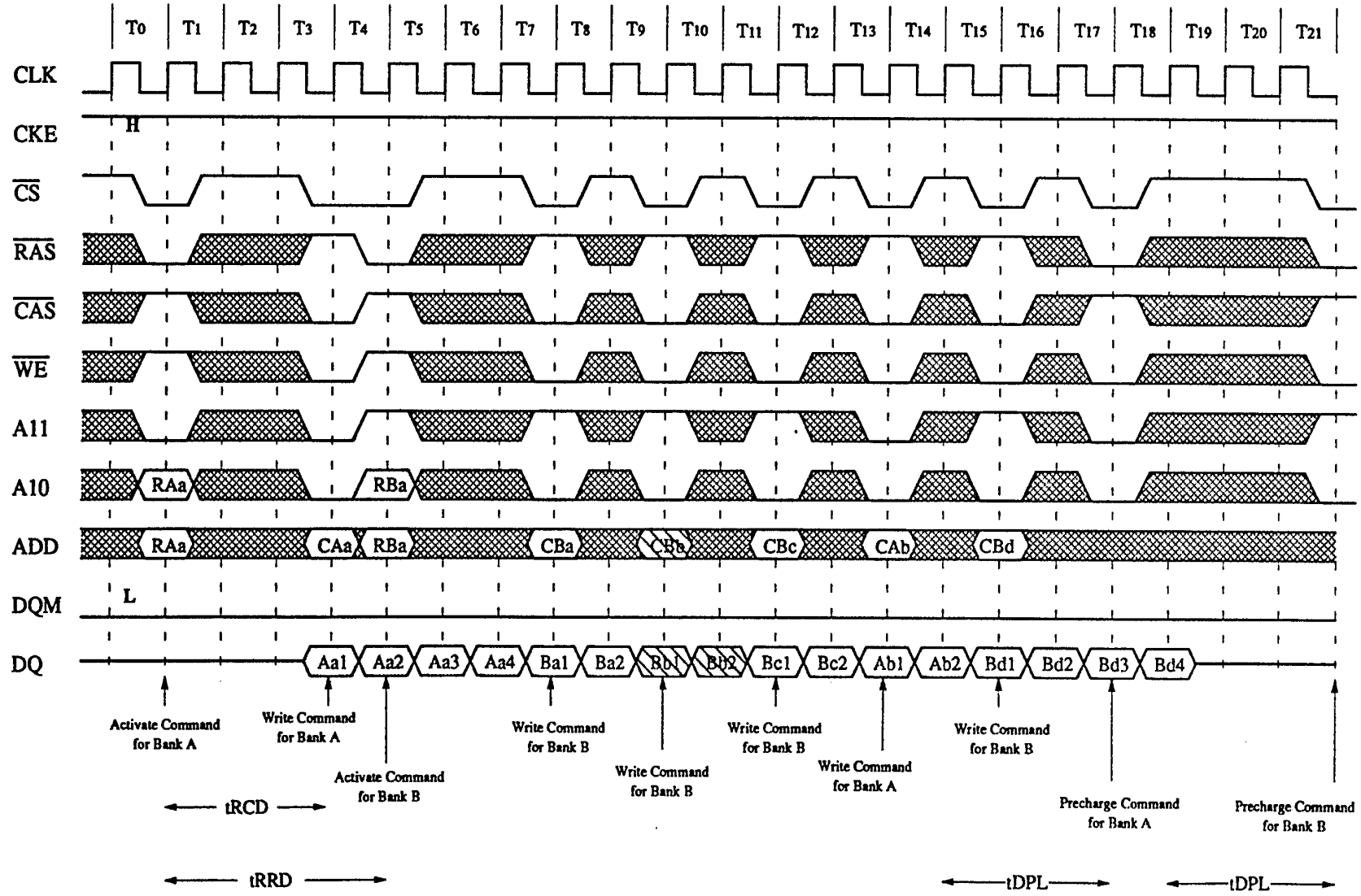
Interleaved Column WRITE CYCLE

Burst Length = 4 Cas Latency = 2



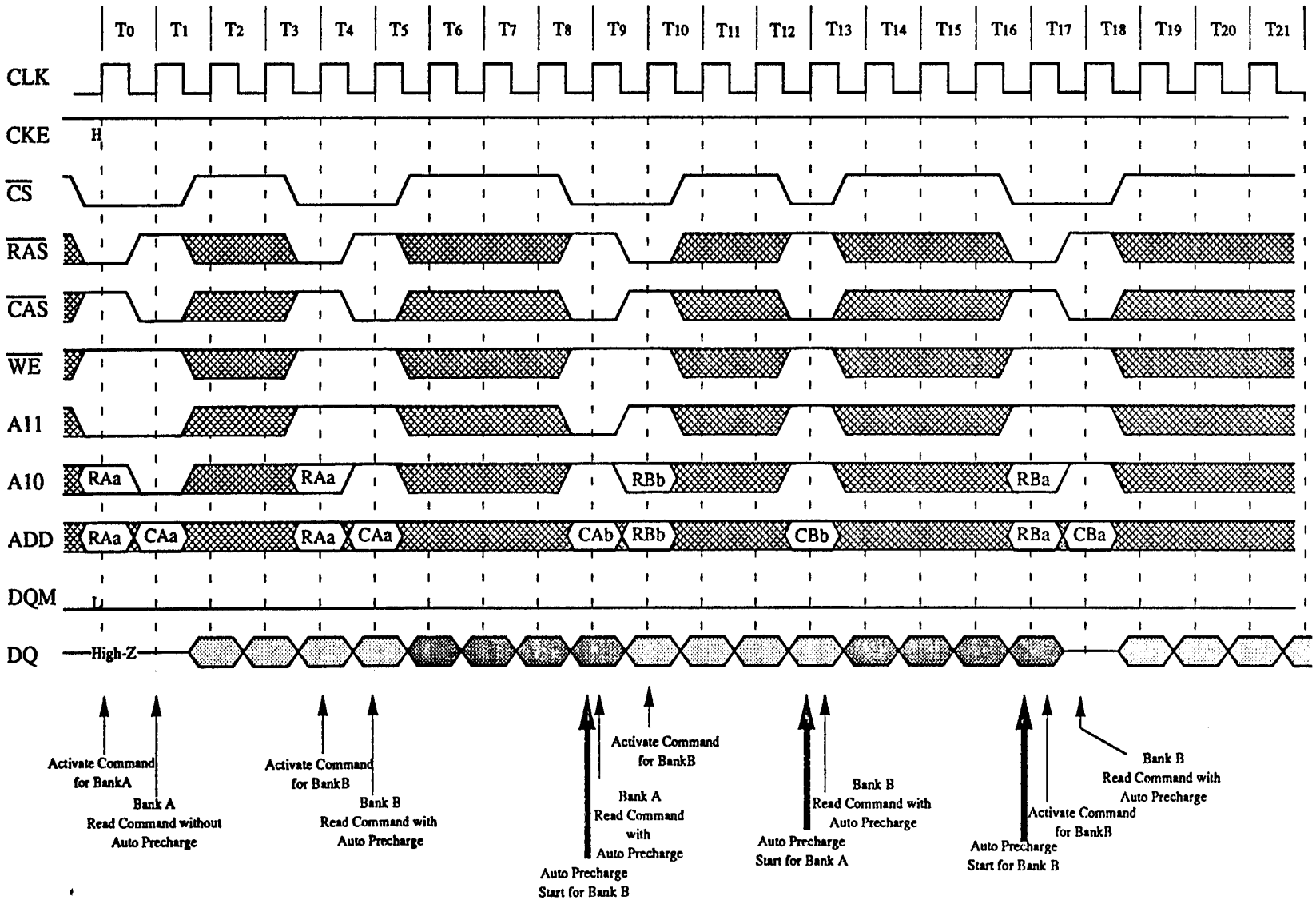
Interleaved Column WRITE CYCLE

Burst Length = 4 Cas Latency = 3



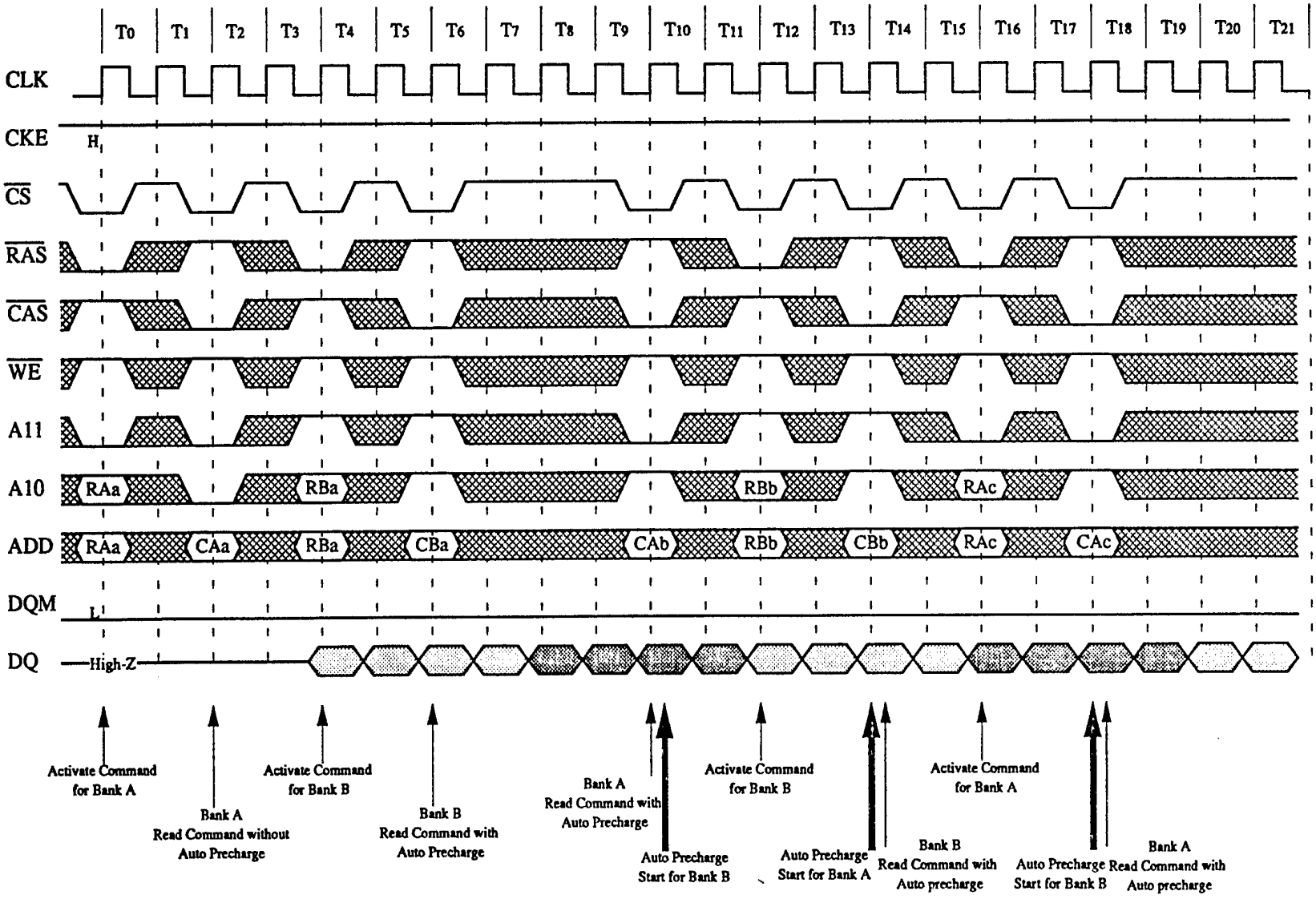
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 1



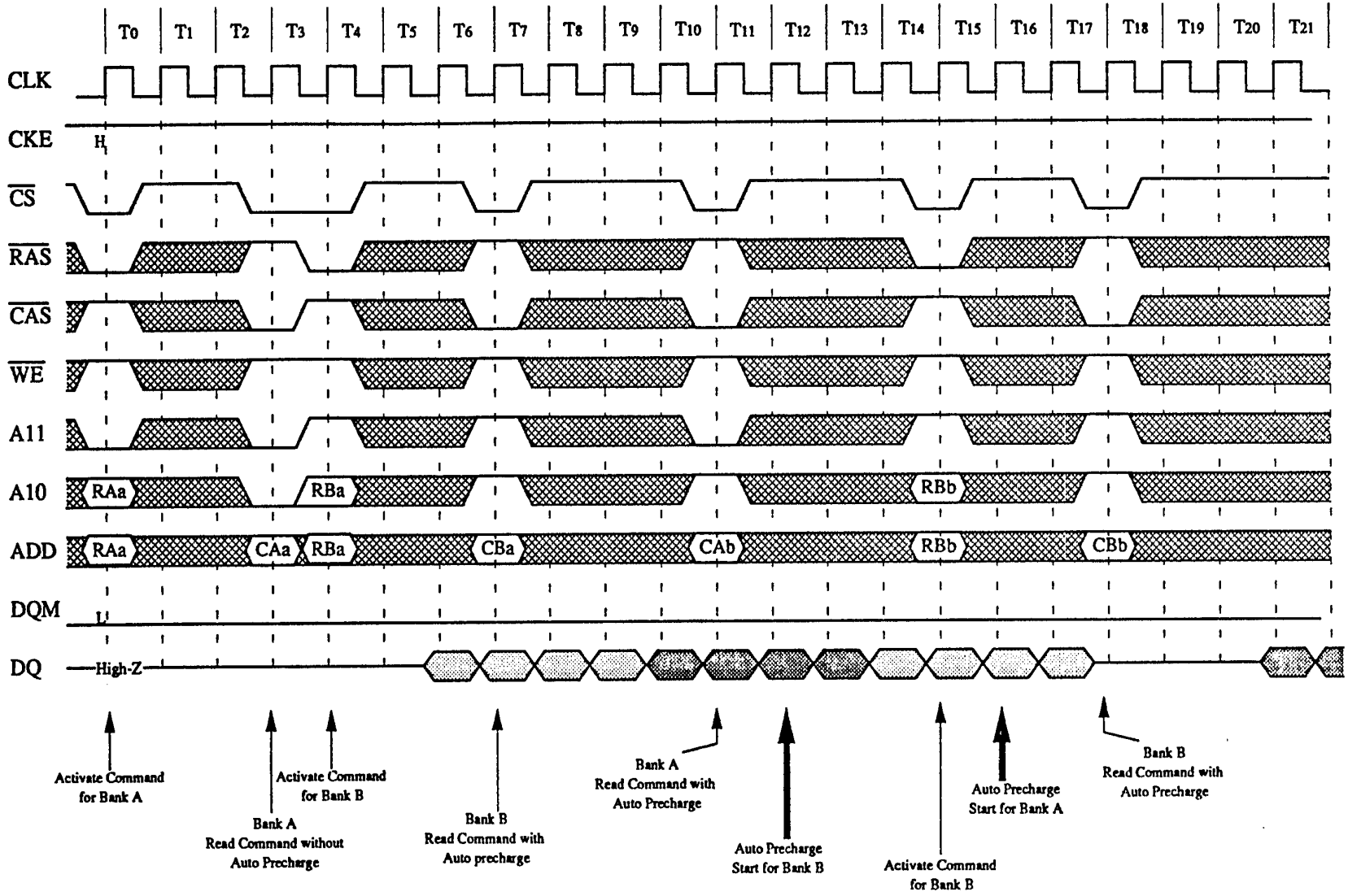
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 2



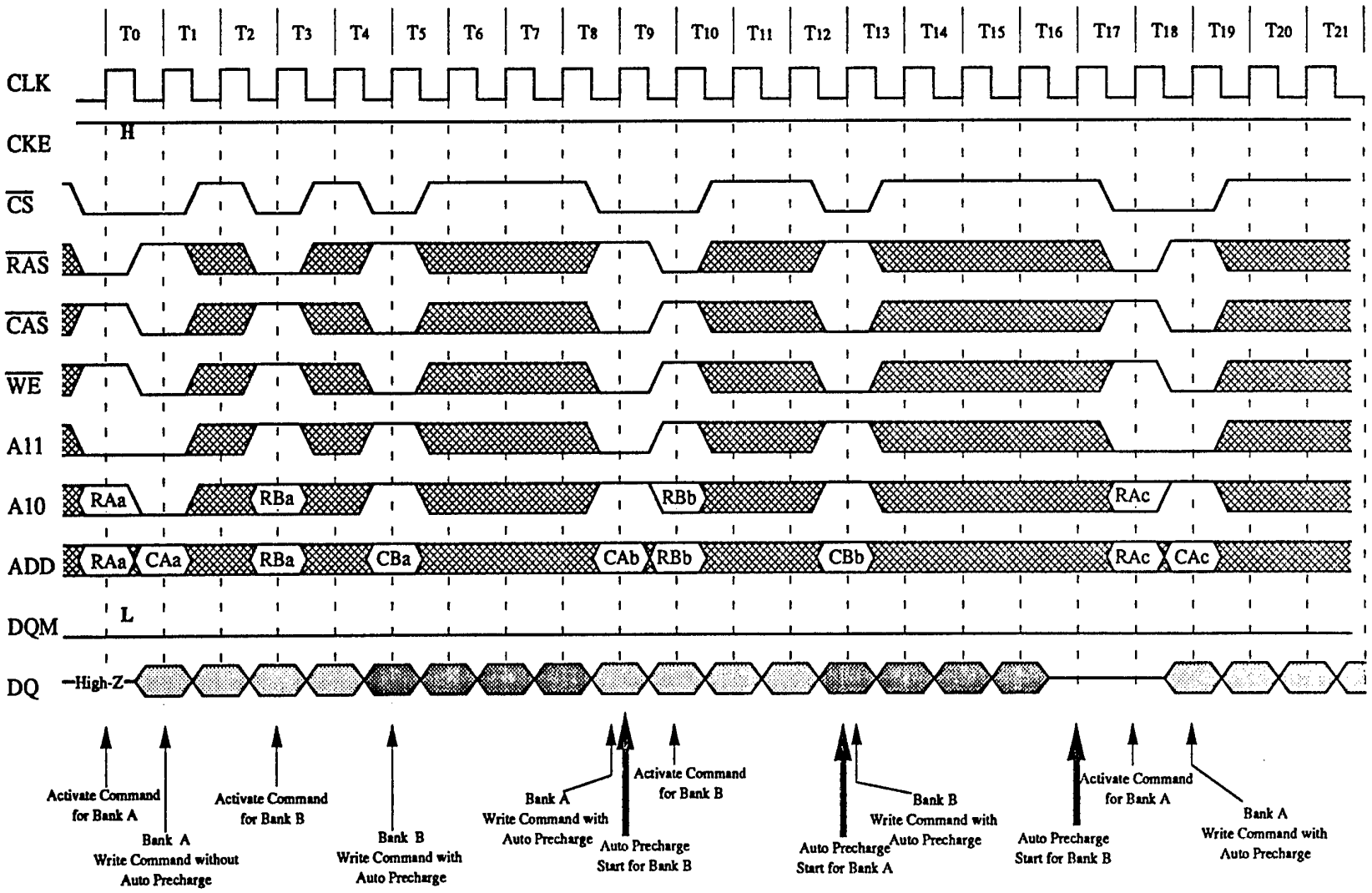
Auto Precharge after Read Burst

Burst Length = 4 CAS Latency = 3



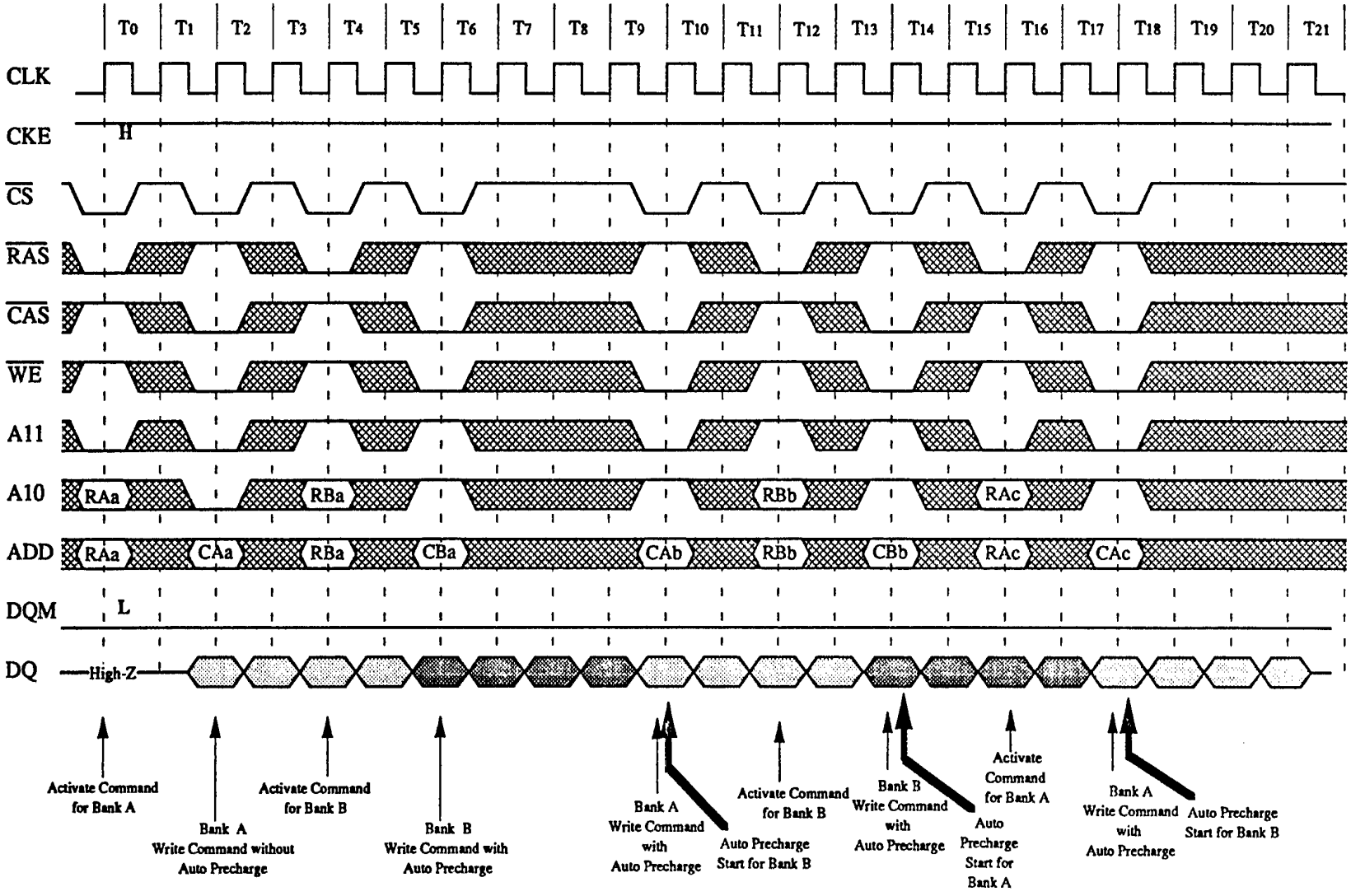
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 1



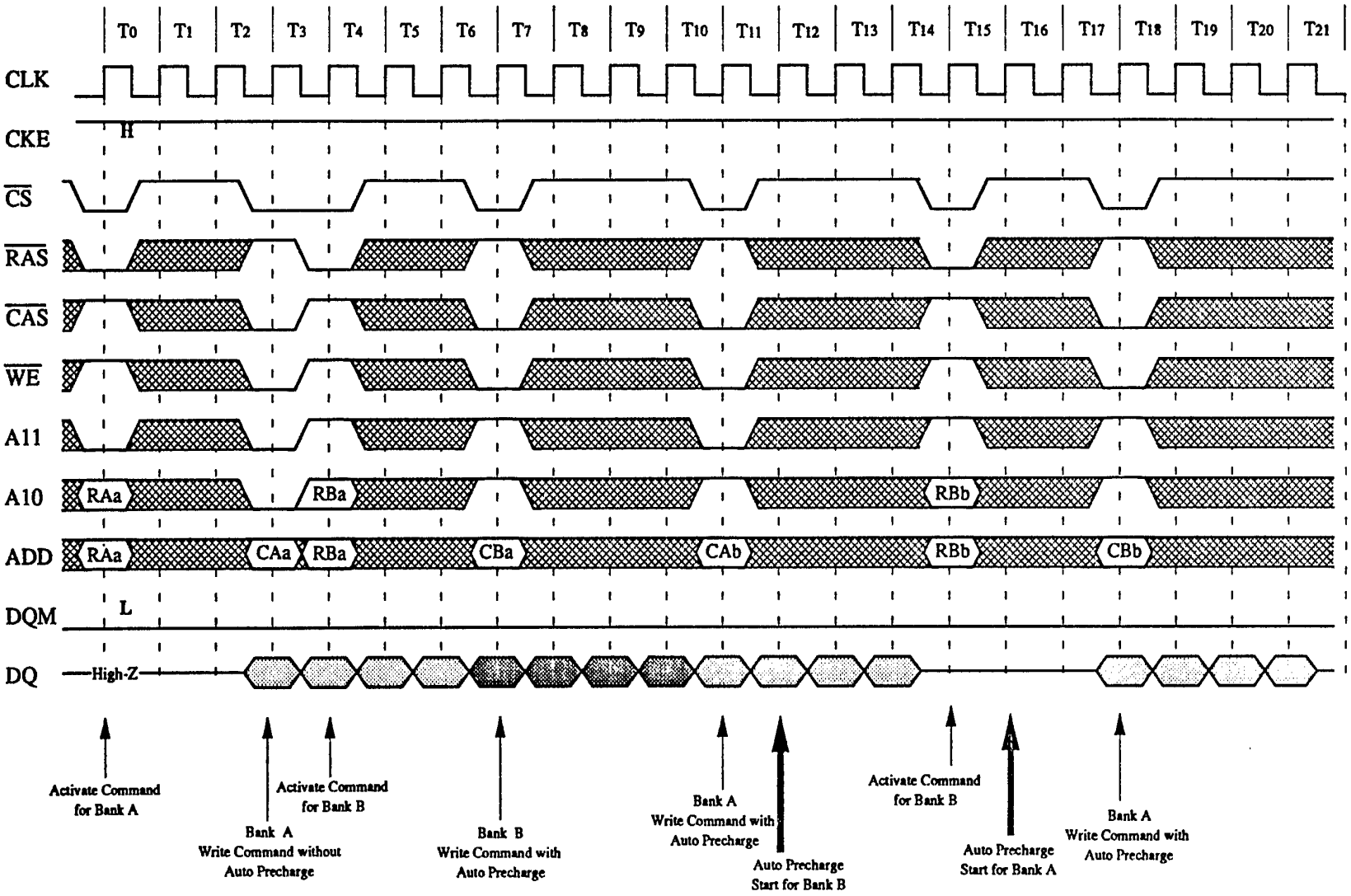
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 2



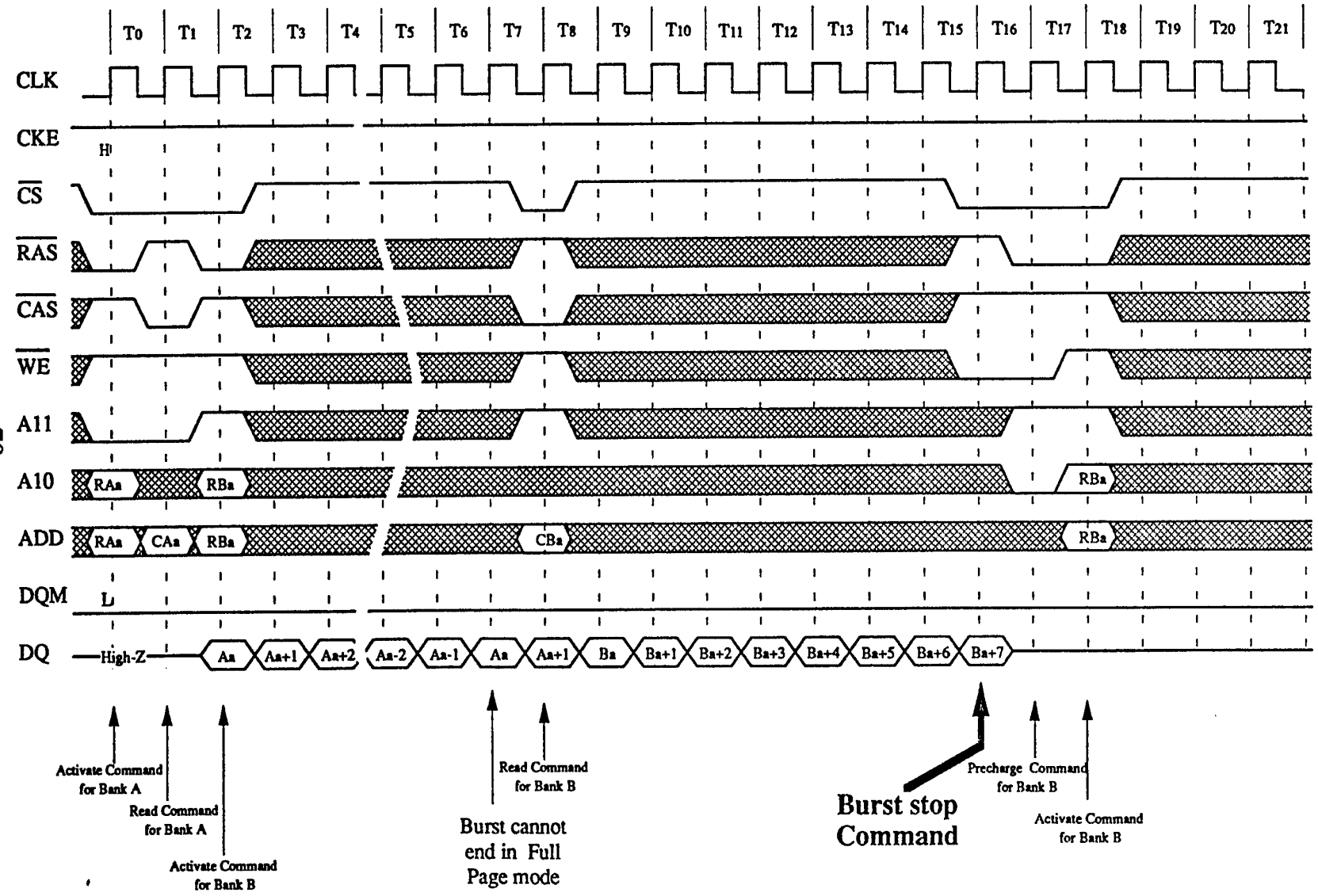
Auto Precharge after Write Burst

Burst Length = 4 CAS Latency = 3



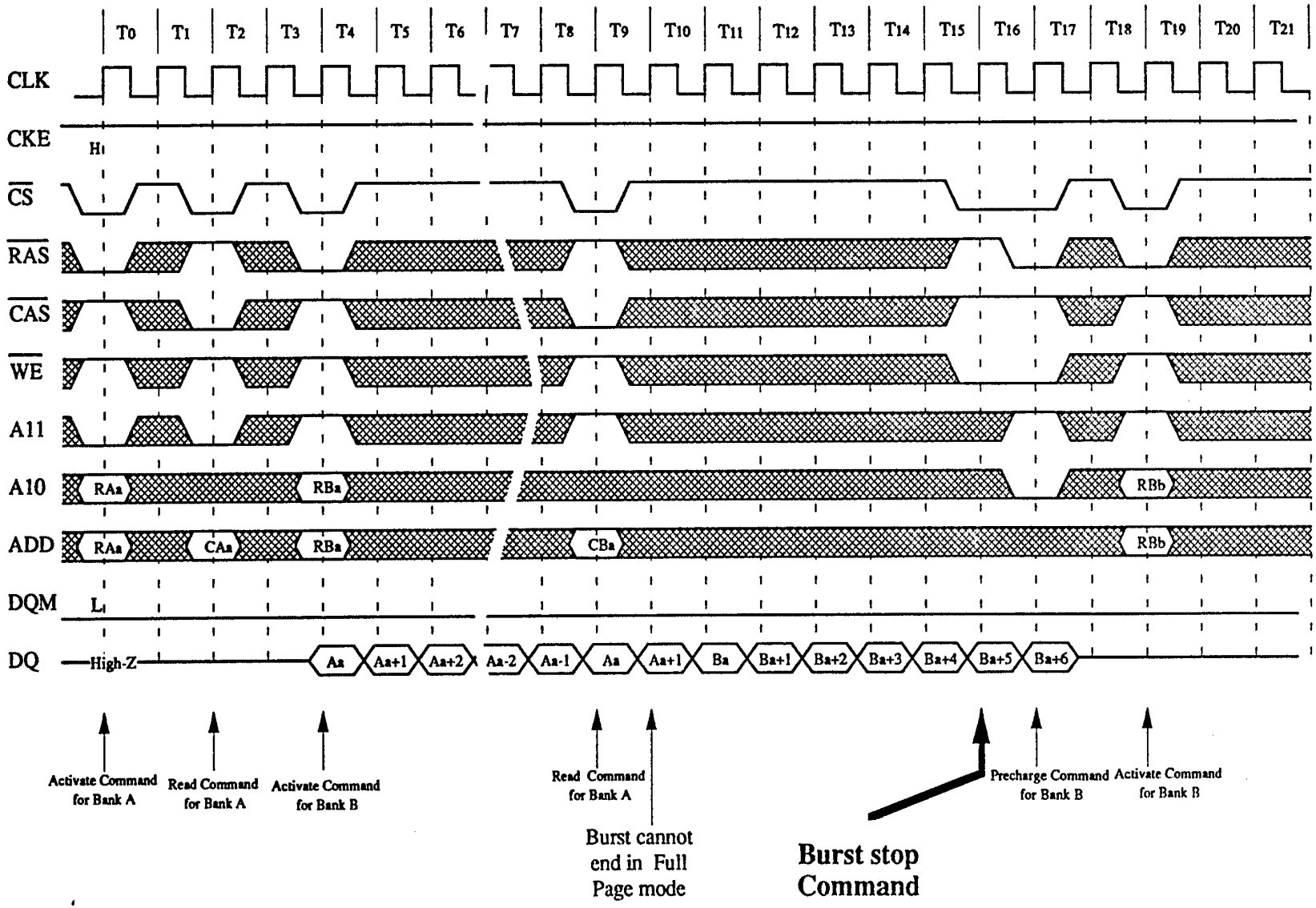
Full Page READ CYCLE

CAS Latency = 1



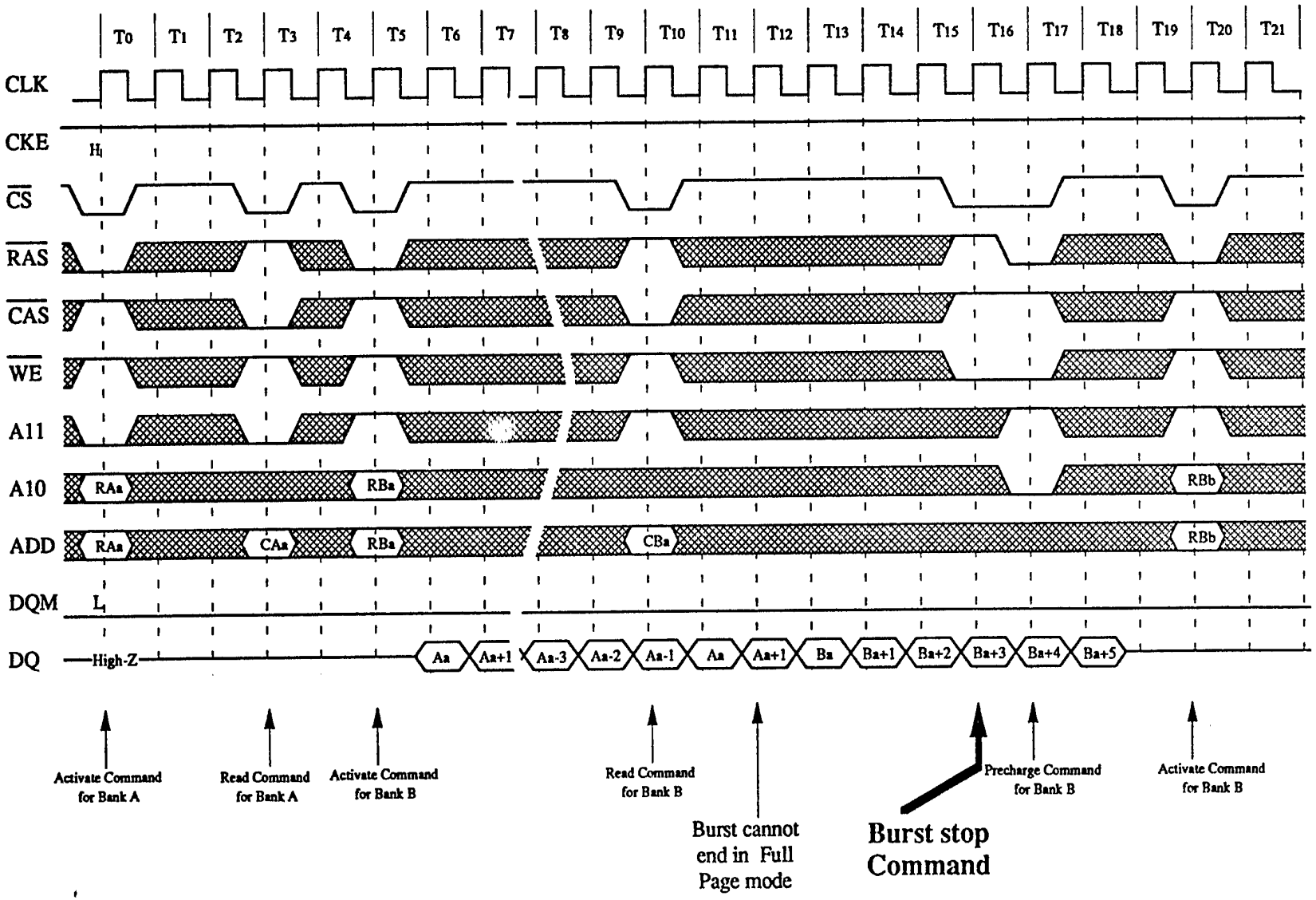
Full Page READ CYCLE

CAS Latency = 2



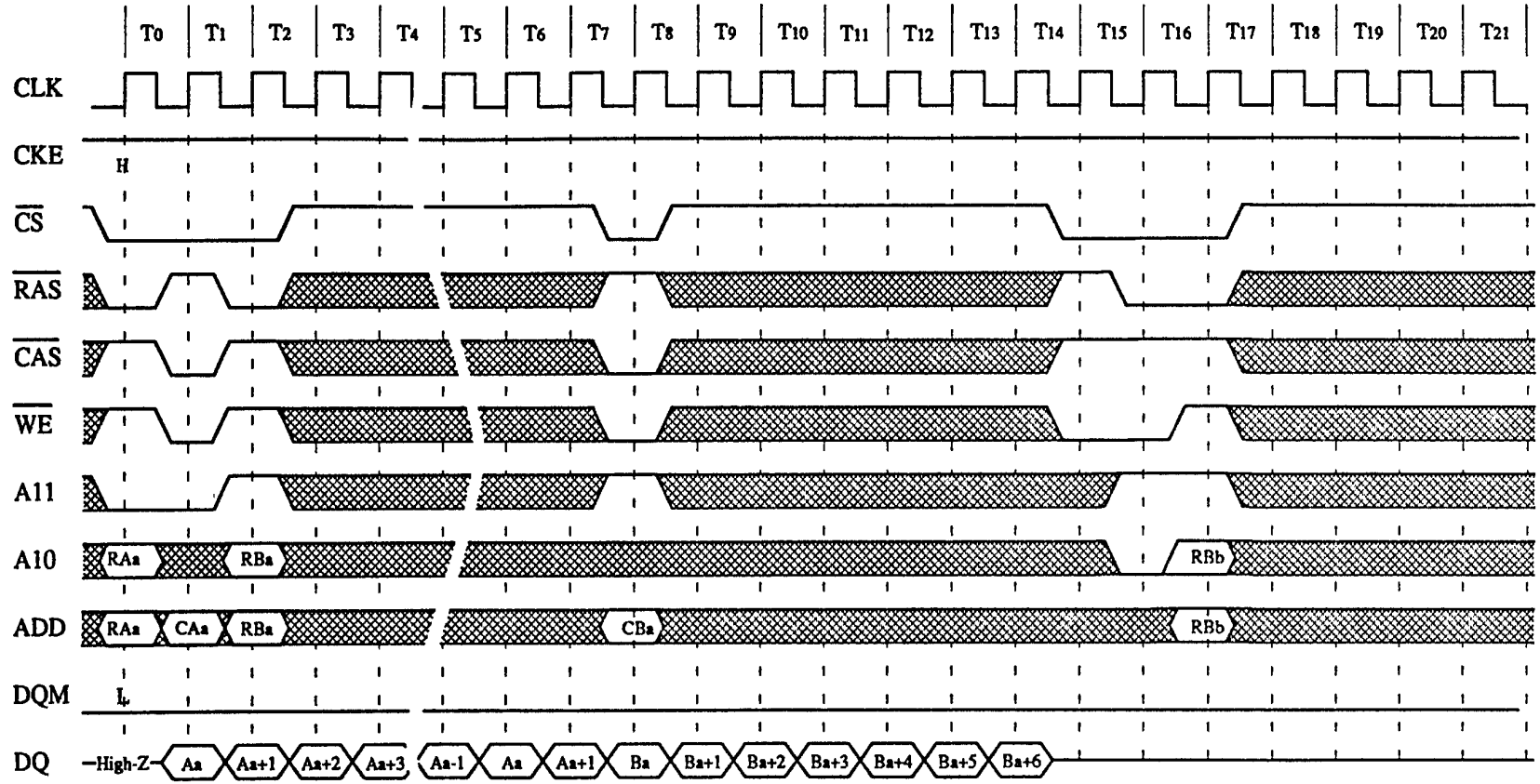
Full Page READ CYCLE

CAS Latency = 3



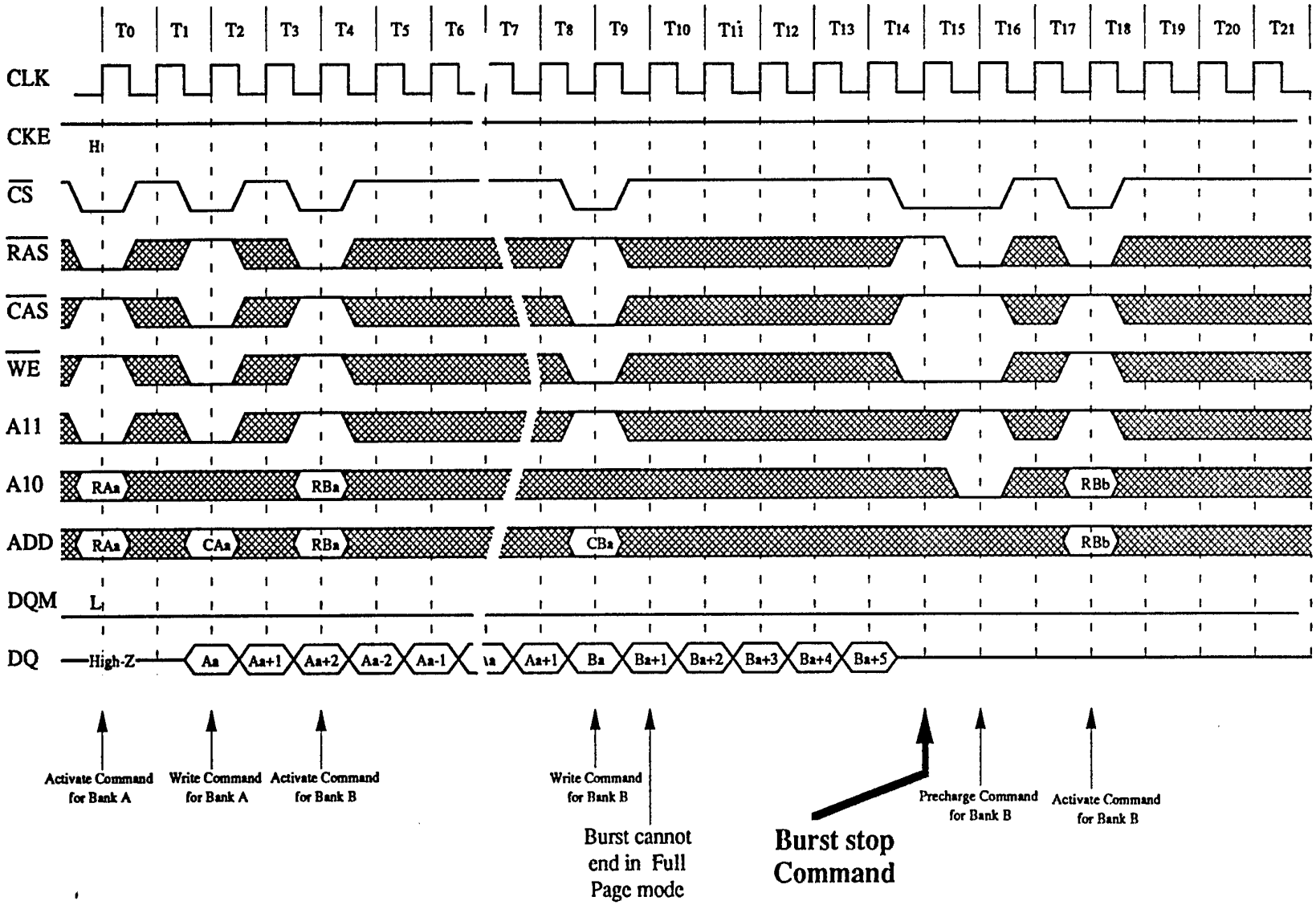
Full Page WRITE CYCLE

CAS Latency = 1



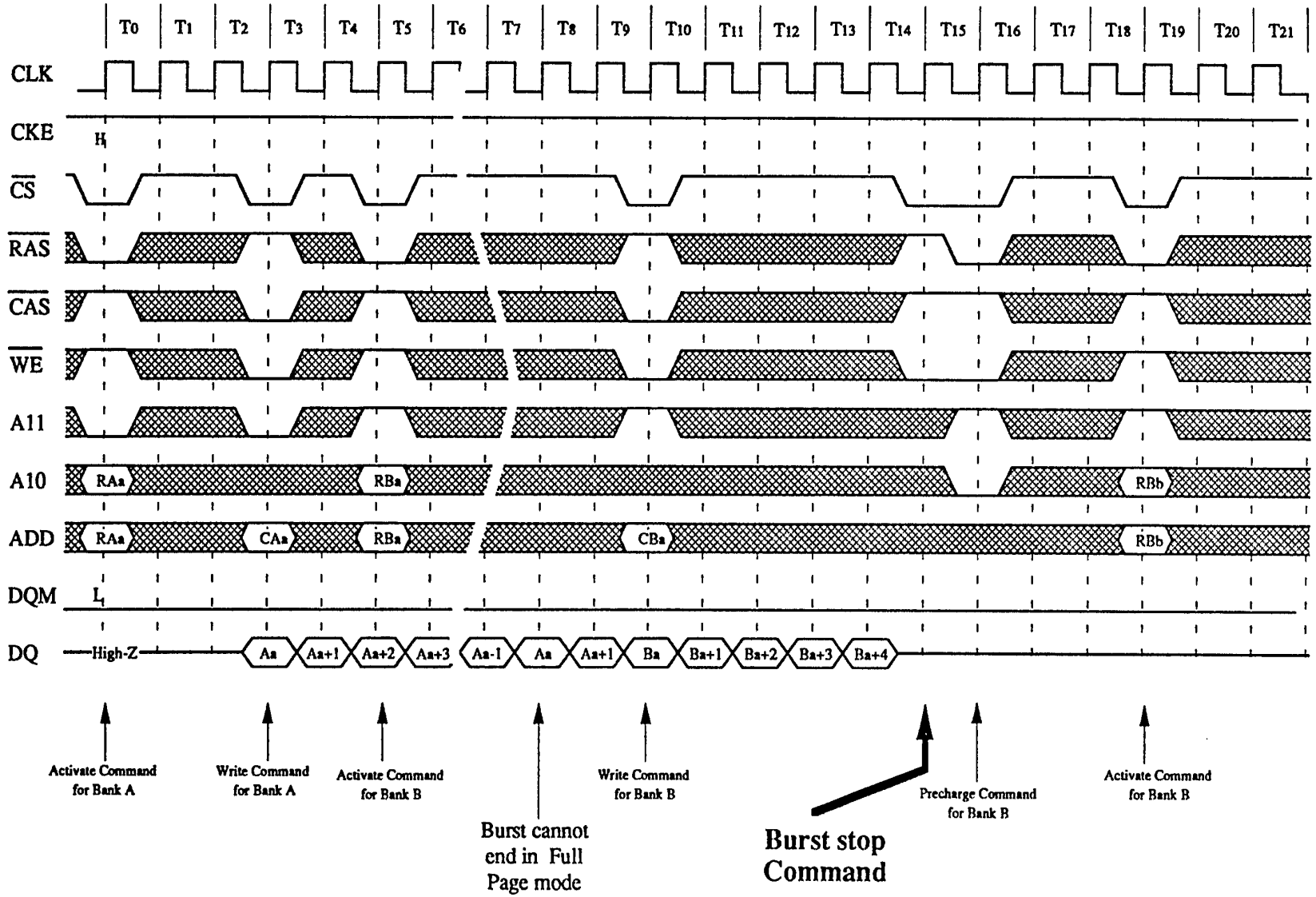
Full Page WRITE CYCLE

CAS Latency = 2



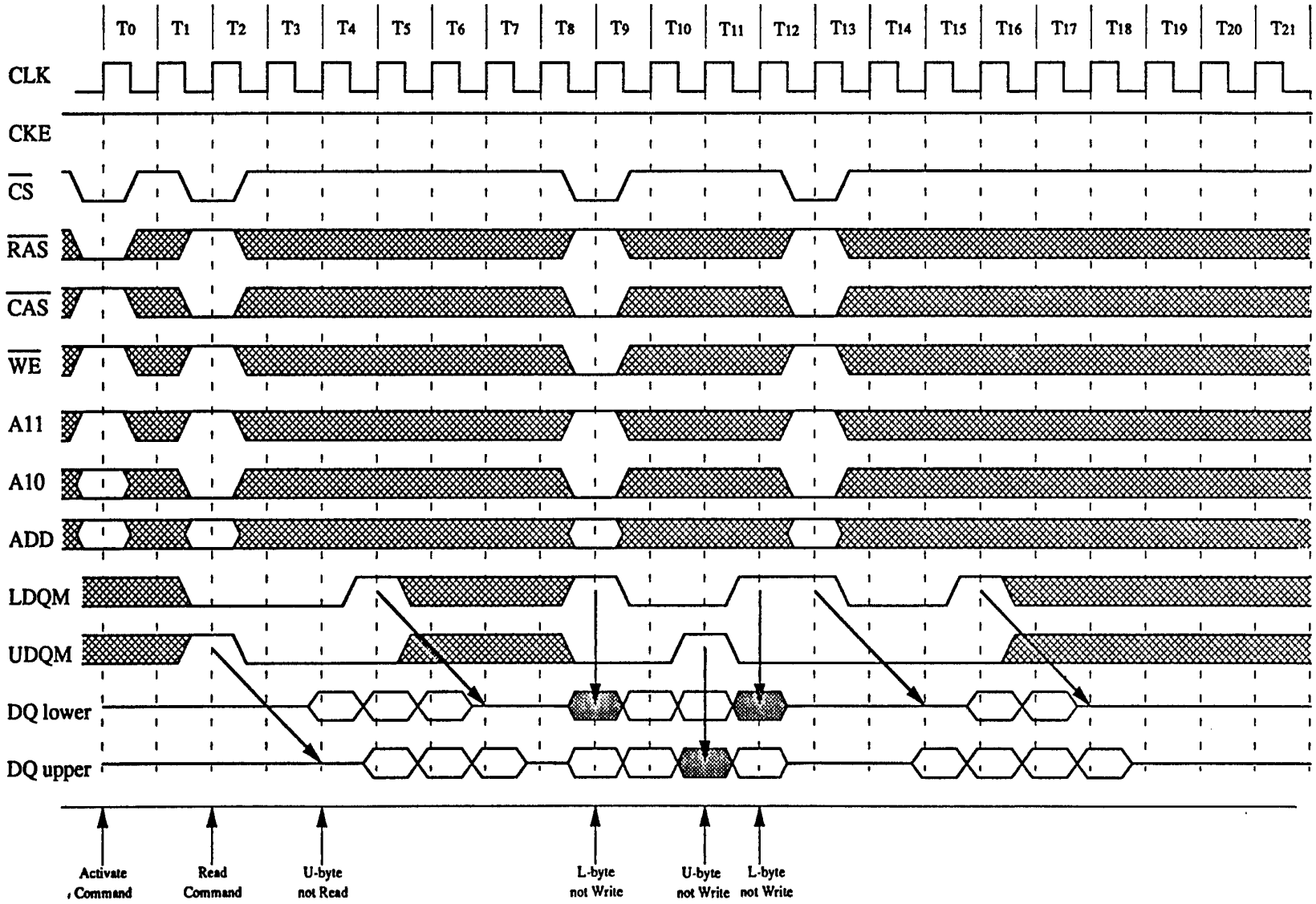
Full Page WRITE CYCLE

CAS Latency = 3



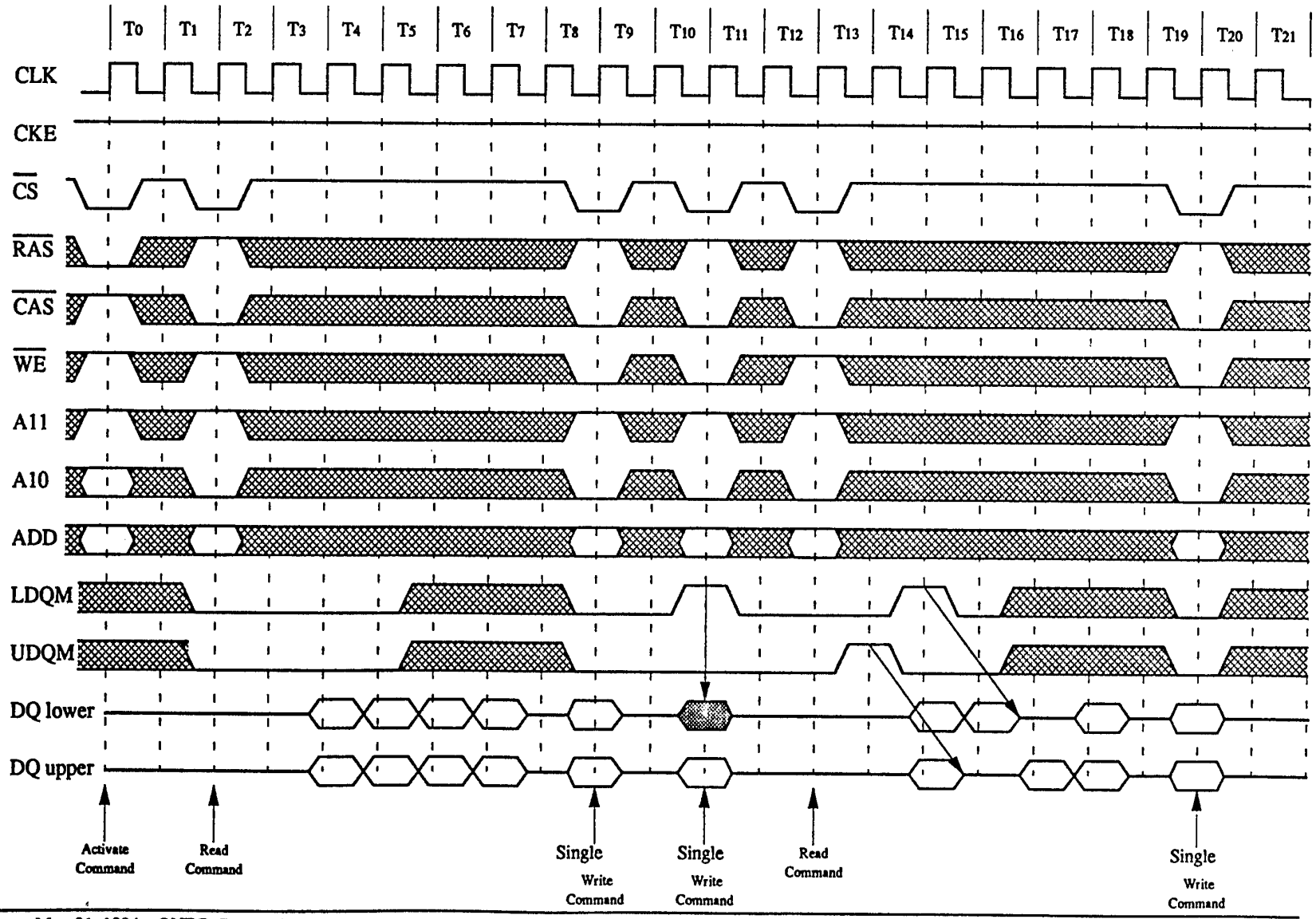
Byte Write Operation

Burst Length = 4 CAS Latency = 2



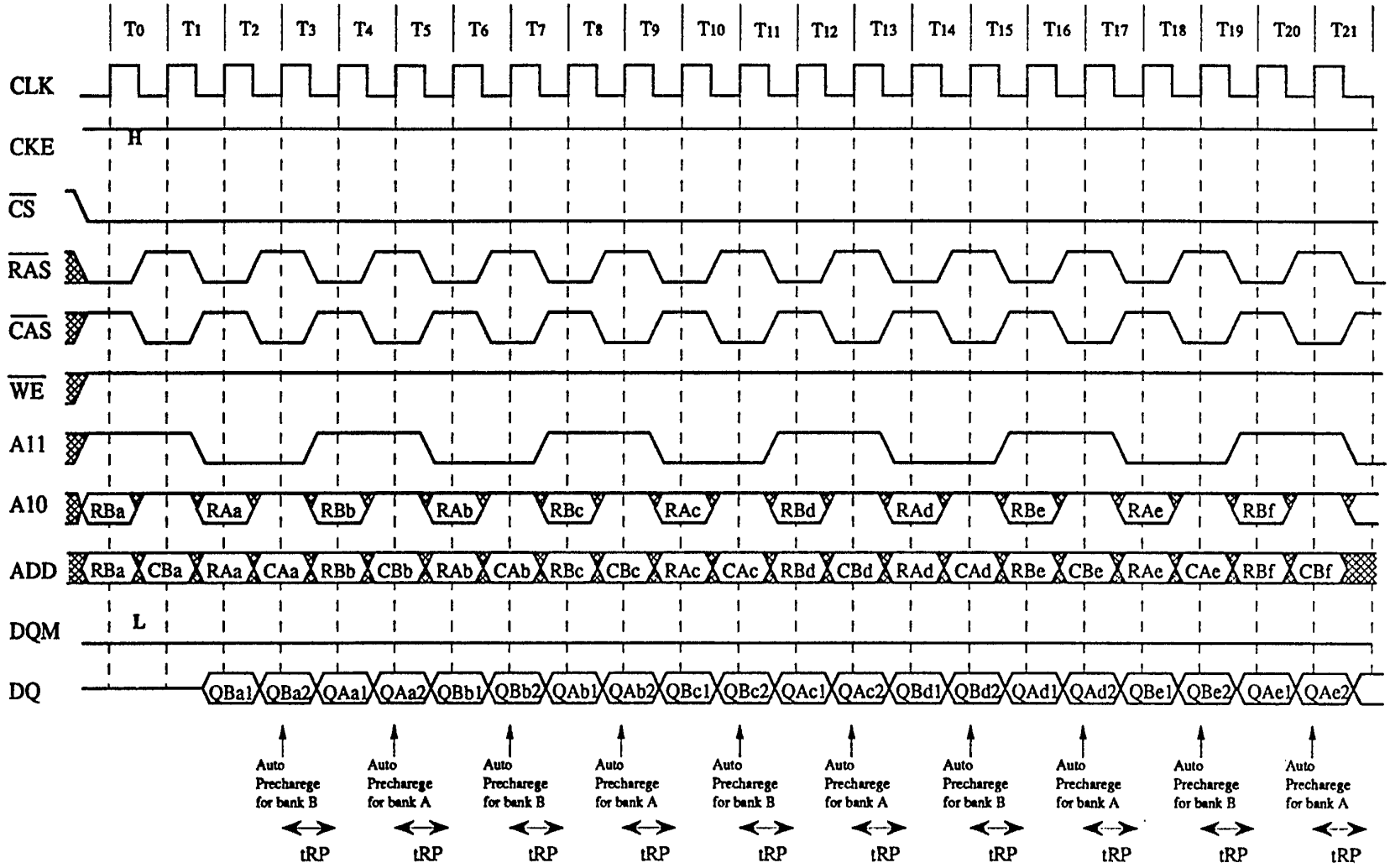
Burst Read and Single Write (Option)

Burst Length = 4 CAS Latency = 2



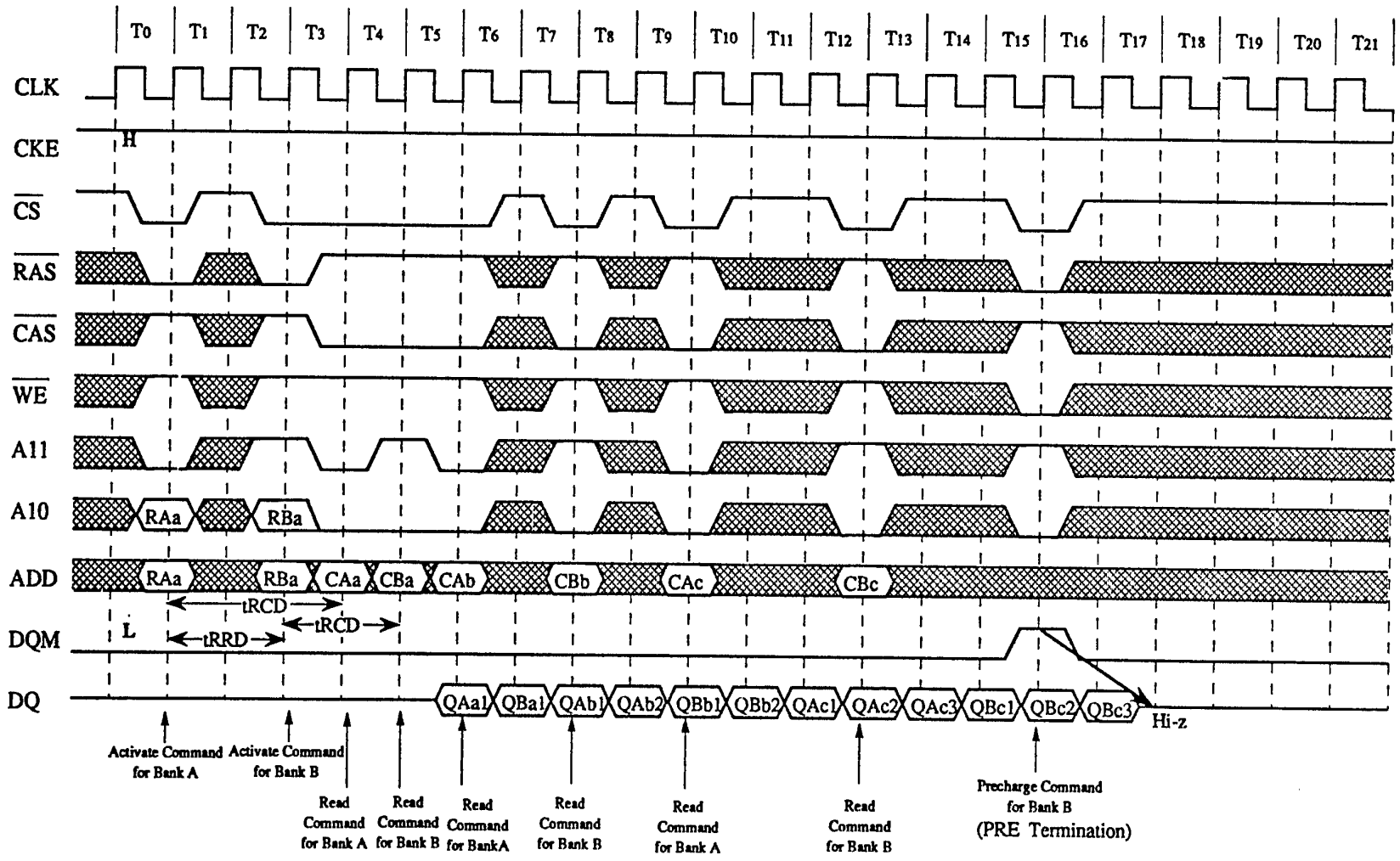
Random Row READ
(Pingpong banks)

Burst Length = 2 CAS Latency = 1



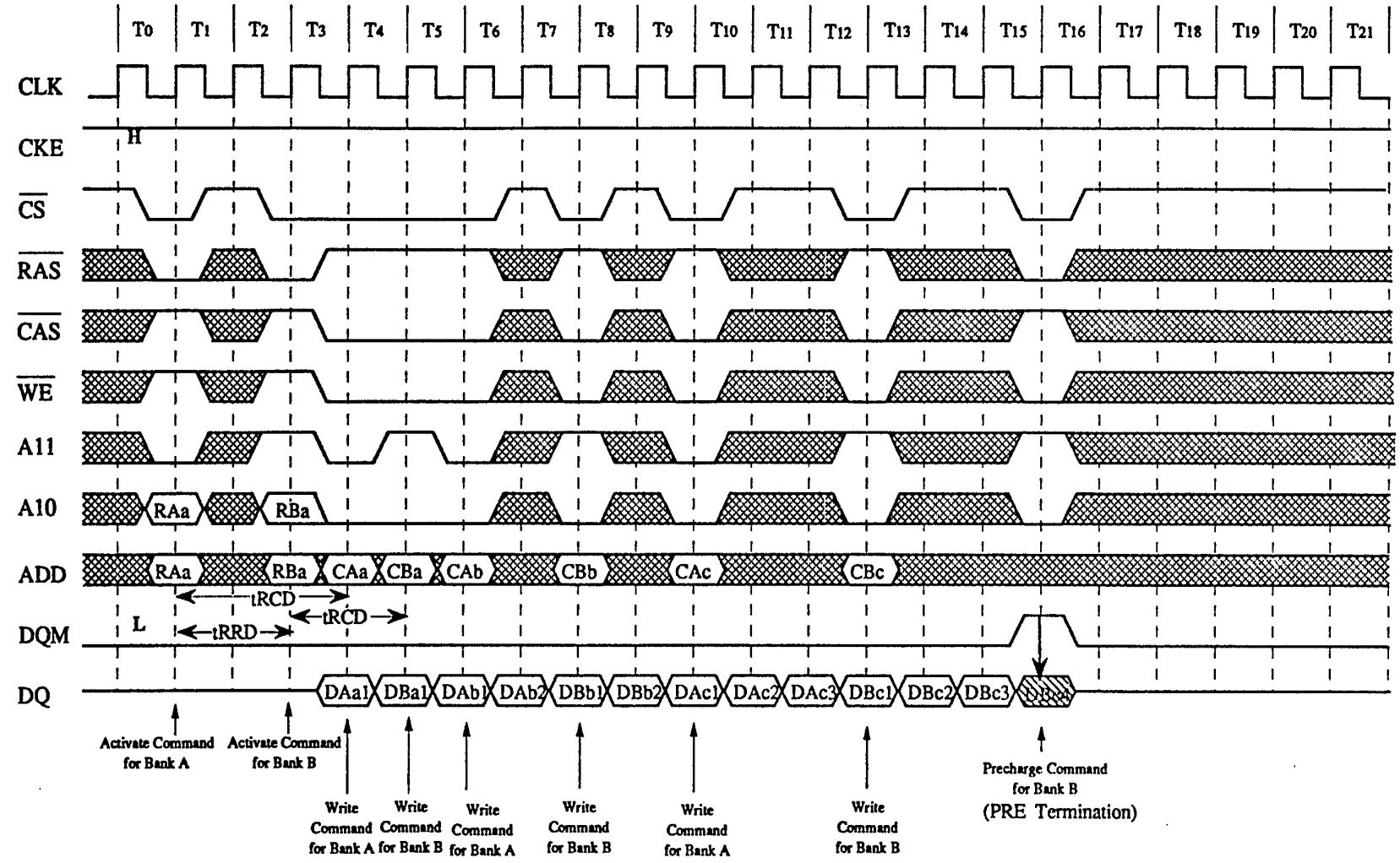
Full Page Random Column Read

Burst Length= Full Page CAS Latency = 2



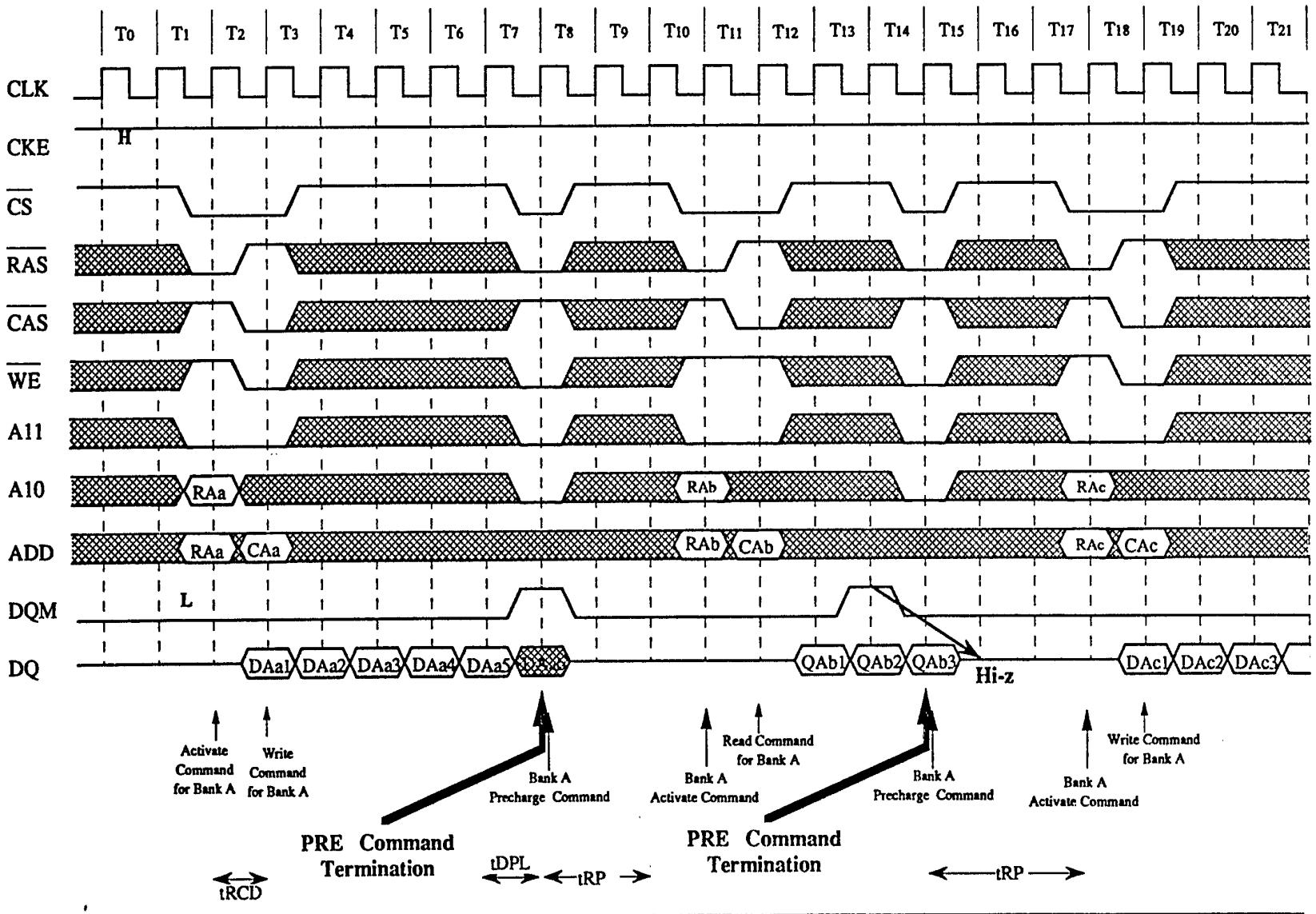
Full Page Random Column Write

Burst Length= Full Page CAS Latency = 2



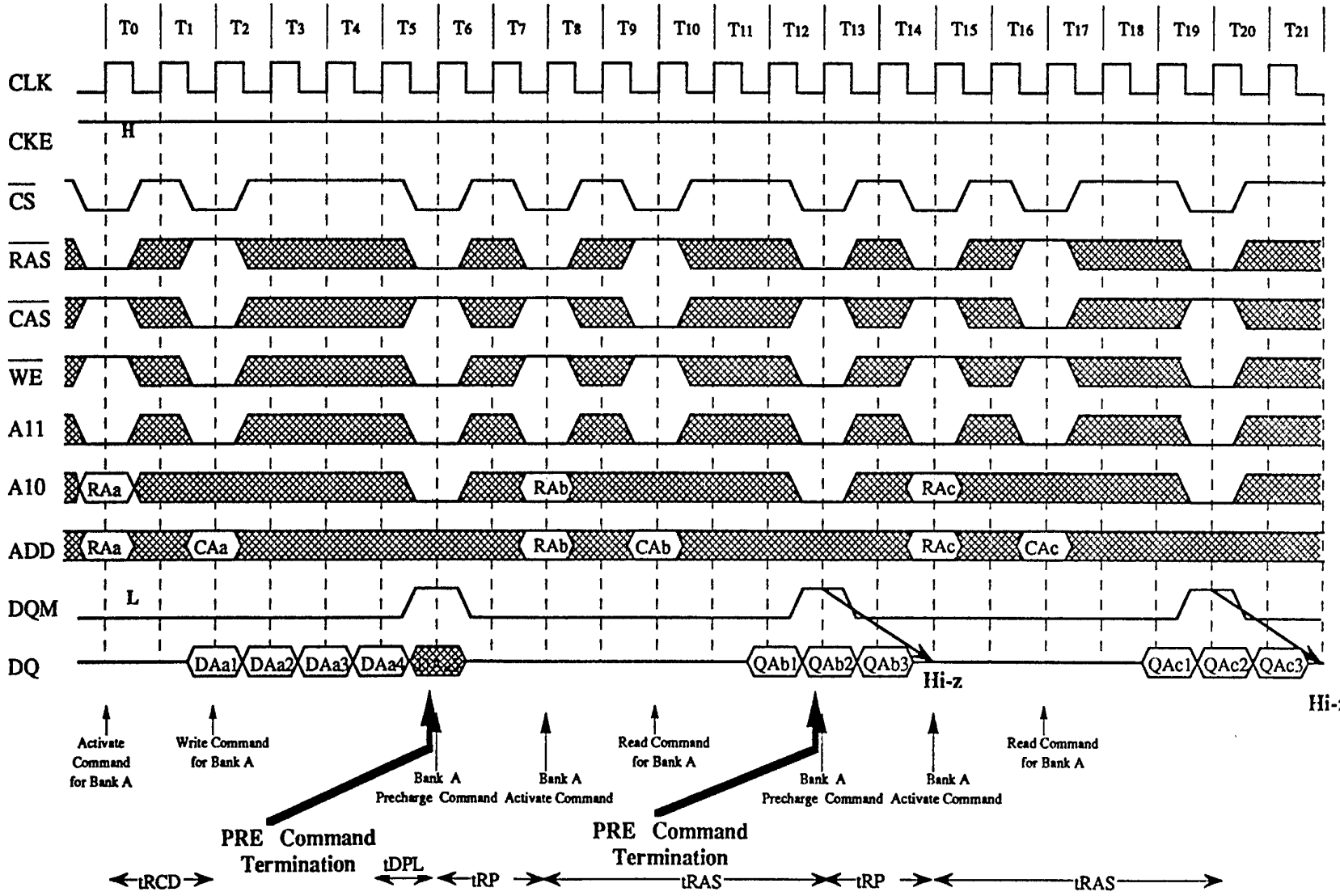
PRE(Precharge)Termination of Burst

Burst Length = 2,4,8,FULL CAS Latency = 1



PRE(Precharge)Termination of Burst

Burst Length = 2,4,8,FULL CAS Latency = 2



PRE(Precharge)Termination of Burst

Burst Length = 2,4,8,FULL CAS Latency = 3