PRELIMINARY

Integrated Circuit Systems, Inc.

ICS84025

CRYSTAL-TO-LVCMOS / LVTTL FREQUENCY SYNTHESIZER WITH FANOUT BUFFER

GENERAL DESCRIPTION

The ICS84025 is a Crystal-to-LVCMOS/LVTTL Frequency Synthesizer with Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO frequency is programmed in steps equal to the value of the crystal frequency. The VCO and output frequency can be programmed using the feedback and output frequency select pins. The low phase noise characteristics of the ICS84025 make it an ideal clock source for Fibre Channel 1 and Gigabit Ethernet applications.

FUNCTION TABLE

Inputs			XTAL	Output Frequency
MR	F_SEL1	F_SEL0		F_OUT
1	X	X		LOW
0	0	0	25.5MHz	53.125MHz
0	0	1	25.5MHz	106.25MHz
0	1	0	25MHz	62.5MHz
0	1	1	25MHz	125MHz

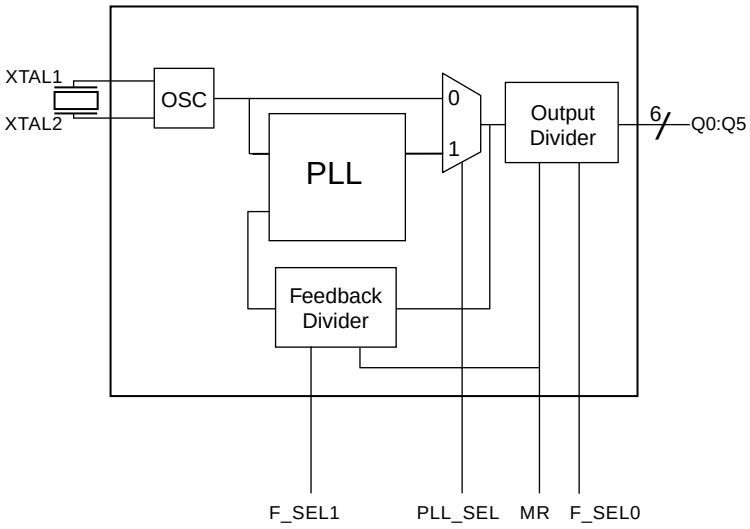
FEATURES

- 6 LVCMOS/LVTTL outputs
- Crystal oscillator interface
- Output frequency range: 53.125MHz to 125MHz
- Crystal input frequency: 25MHz and 25.5MHz
- RMS phase jitter at 106.25, using a 25.5MHz crystal (637KHz to 10MHz): 3.25ps
- Phase noise:

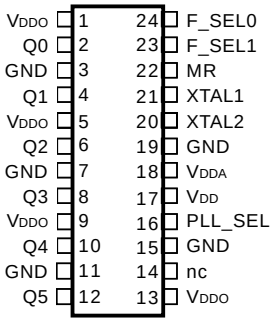
Offset	Noise Power
100Hz	-100 dBc/Hz
1KHz	-115 dBc/Hz
10KHz	-125 dBc/Hz
100KHz	-127 dBc/Hz

- 3.3V core, outputs may either be 3.3V, 2.5V or 1.8V
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS84025
24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm body package
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5, 9, 13	V_{DDO}	Power		Output supply pins.
2	Q0	Output		Clock output. LVCMOS/LVTTL interface levels.
3, 7, 11, 15, 19	GND	Power		Power supply ground.
4	Q1	Output		Clock output. LVCMOS/LVTTL interface levels.
6	Q2	Output		Clock output. LVCMOS/LVTTL interface levels.
8	Q3	Output		Clock output. LVCMOS/LVTTL interface levels.
10	Q4	Output		Clock output. LVCMOS/LVTTL interface levels.
12	Q5	Output		Clock output. LVCMOS/LVTTL interface levels.
14	nc	Unused		No connect.
16	PLL_SEL	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When HIGH, selects PLL. When LOW, selects XTAL1, XTAL2. LVCMOS / LVTTL interface levels.
17	V_{DD}	Power		Core supply pin.
18	V_{DDA}	Power		Analog supply pin.
20, 21	XTAL2, XTAL1	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
22	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
23	F_SEL1	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTL interface levels.
24	F_SEL0	Input	Pullup	Output frequency select pin. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V		TBD		pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V		TBD		pF
		V_{DD} = 3.465V, V_{DDO} = 1.95V		TBD		pF

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
I_{DD}	Power Supply Current			71		mA
I_{DDA}	Analog Supply Current			15		mA
I_{DDO}	Output Supply Current			70		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, MR, F_SEL0, F_SEL1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	PLL_SEL, MR, F_SEL0, F_SEL1		-0.3		0.8	V
I_{IH}	Input High Current	MR, F_SEL1	$V_{DD} = V_{IN} = 3.465V$			150	µA
		PLL_SEL, F_SEL0	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	MR, F_SEL1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL, F_SEL0	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO} = 2.5V \pm 5\%$	1.8			V
			$V_{DDO} = 1.8V \pm 0.15V$	V_{DDO} - 0.45			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$			0.5	V
			$V_{DDO} = 2.5V \pm 5\%$			0.5	V
			$V_{DDO} = 1.8V \pm 0.15V$			0.45	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		25		25.5	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		125	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2			50		ps
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle			50		%
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - TBD		t_{PERIOD}/2 + TBD	ps
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		125	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2			30		ps
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle			50		%
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - TBD		t_{PERIOD}/2 + TBD	ps
t_{LOCK}	PLL Lock Time				1	ms

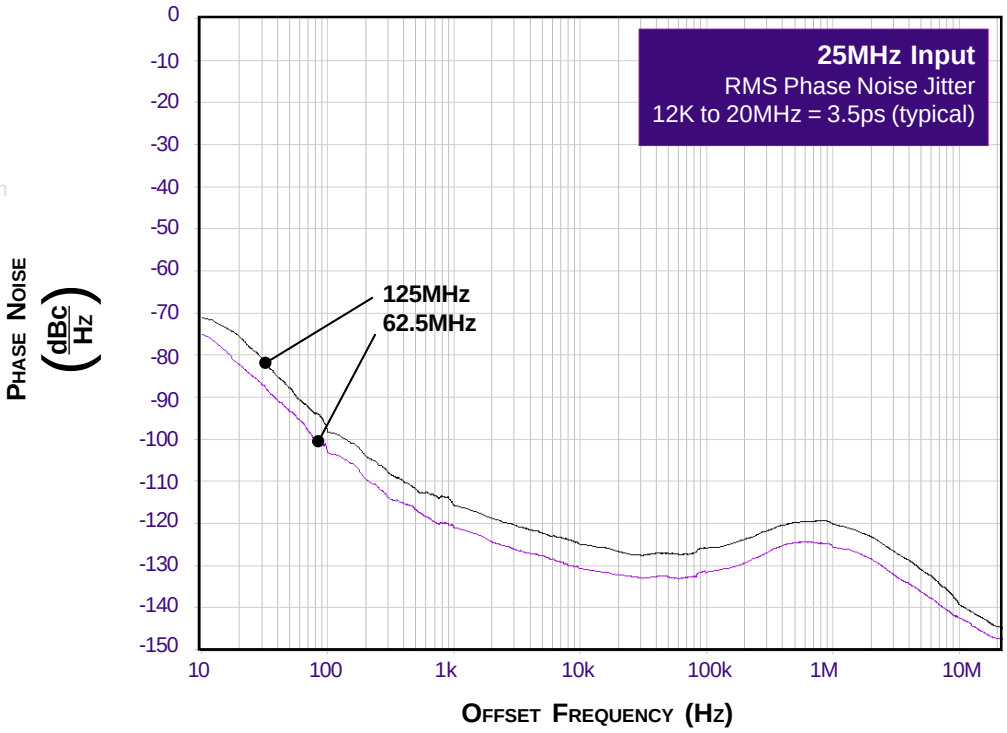
See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

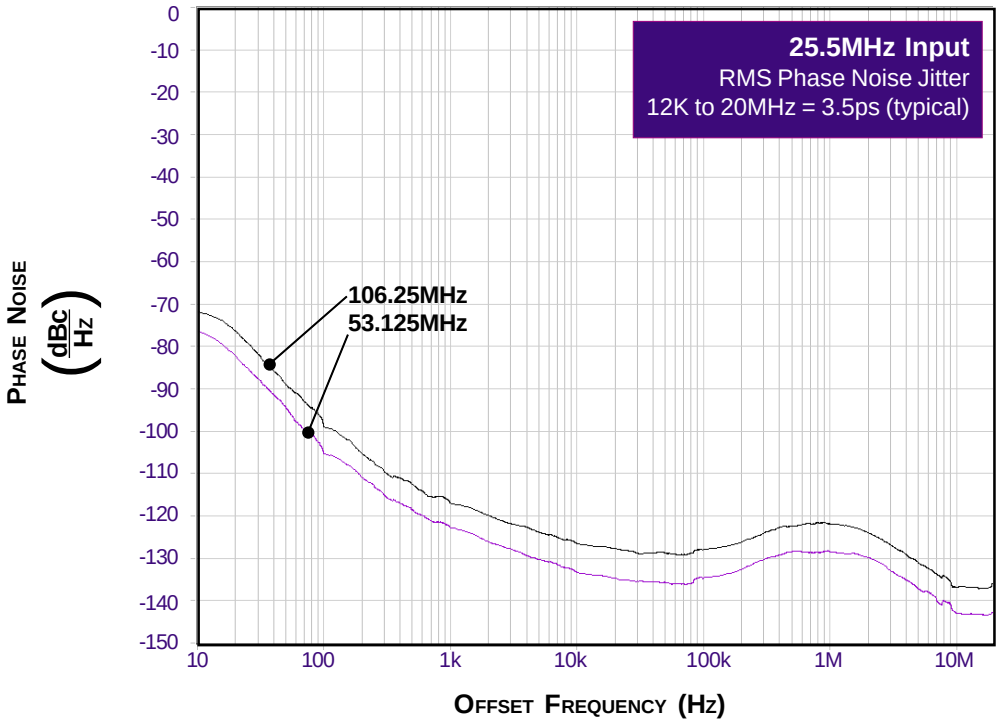
TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		125	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2			30		ps
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle			50		%
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - TBD		t_{PERIOD}/2 + TBD	ps
t_{LOCK}	PLL Lock Time				1	ms

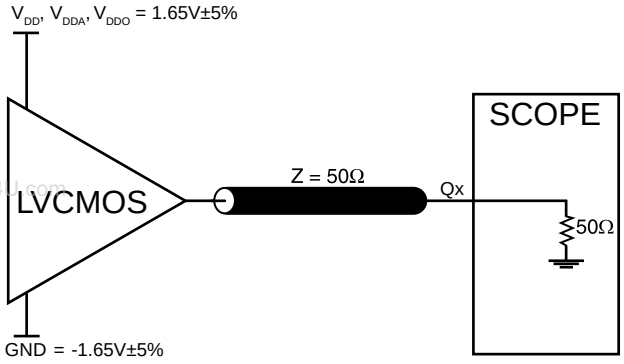
See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TYPICAL PHASE NOISE

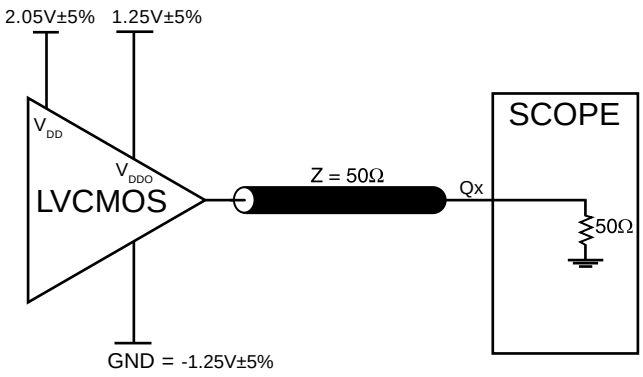




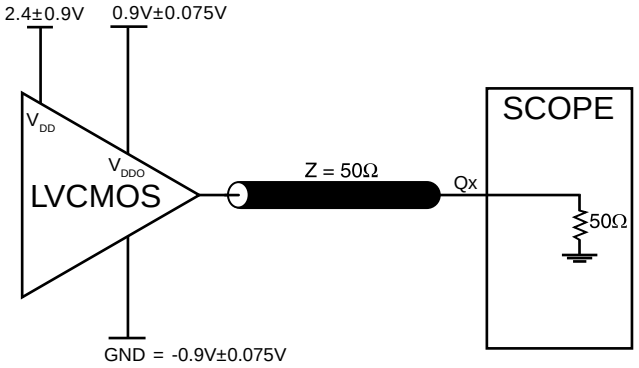
PARAMETER MEASUREMENT INFORMATION



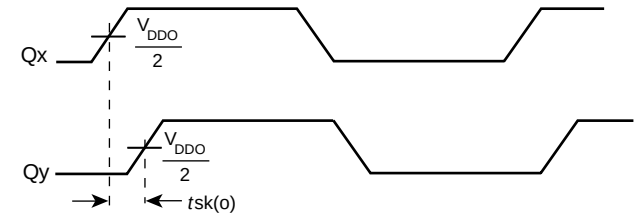
3.3V OUTPUT LOAD AC TEST CIRCUIT



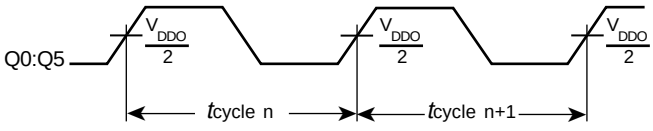
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



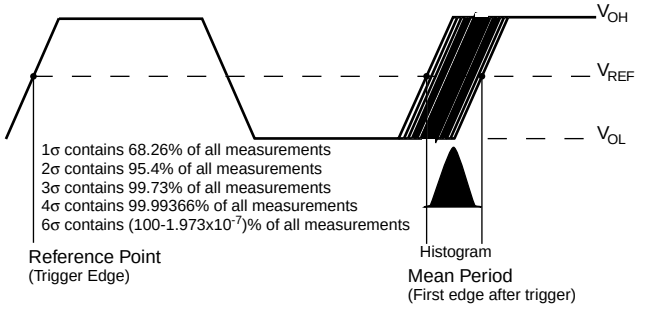
OUTPUT SKEW



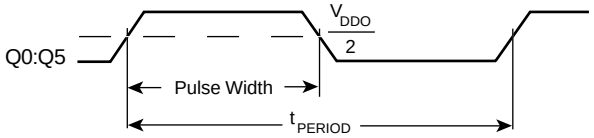
$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$

1000 Cycles

Cycle-to-Cycle Jitter

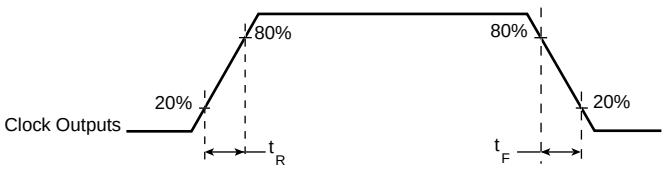


Period Jitter



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc, t_{PW} & t_{PERIOD}



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84025 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

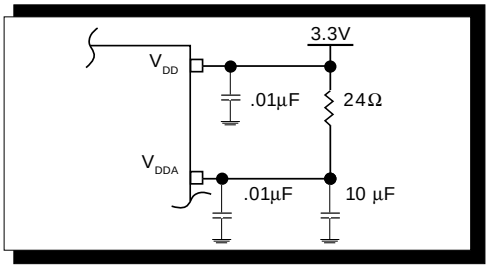


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS84025 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 3*.

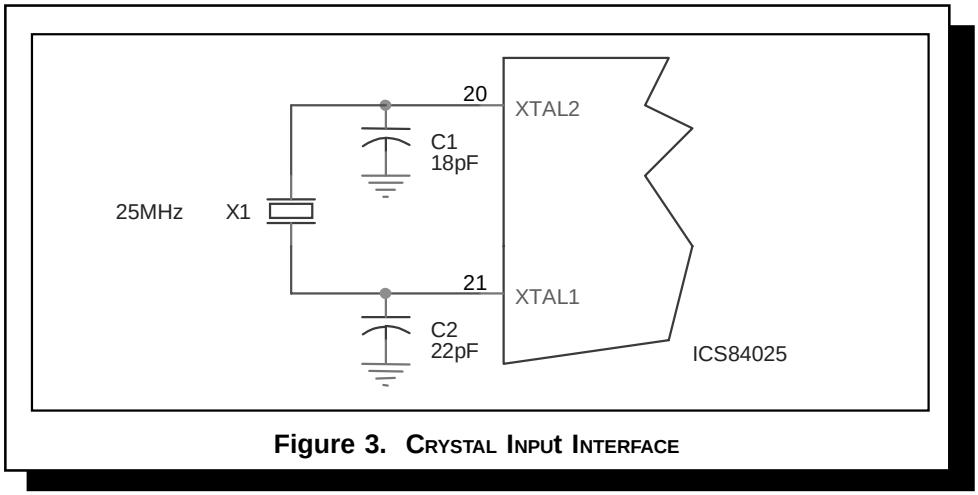


Figure 3. CRYSTAL INPUT INTERFACE

SCHEMATIC EXAMPLE

Figure 4A shows a schematic example of using an ICS84025. In this example, the input is a 25MHz parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 is 22pF and 18pF respectively. This example also shows logic control input handling. The configuration is set at F_SEL[1:0]=11 therefore the output frequency is 125MHz. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{DDA} pin as possible.

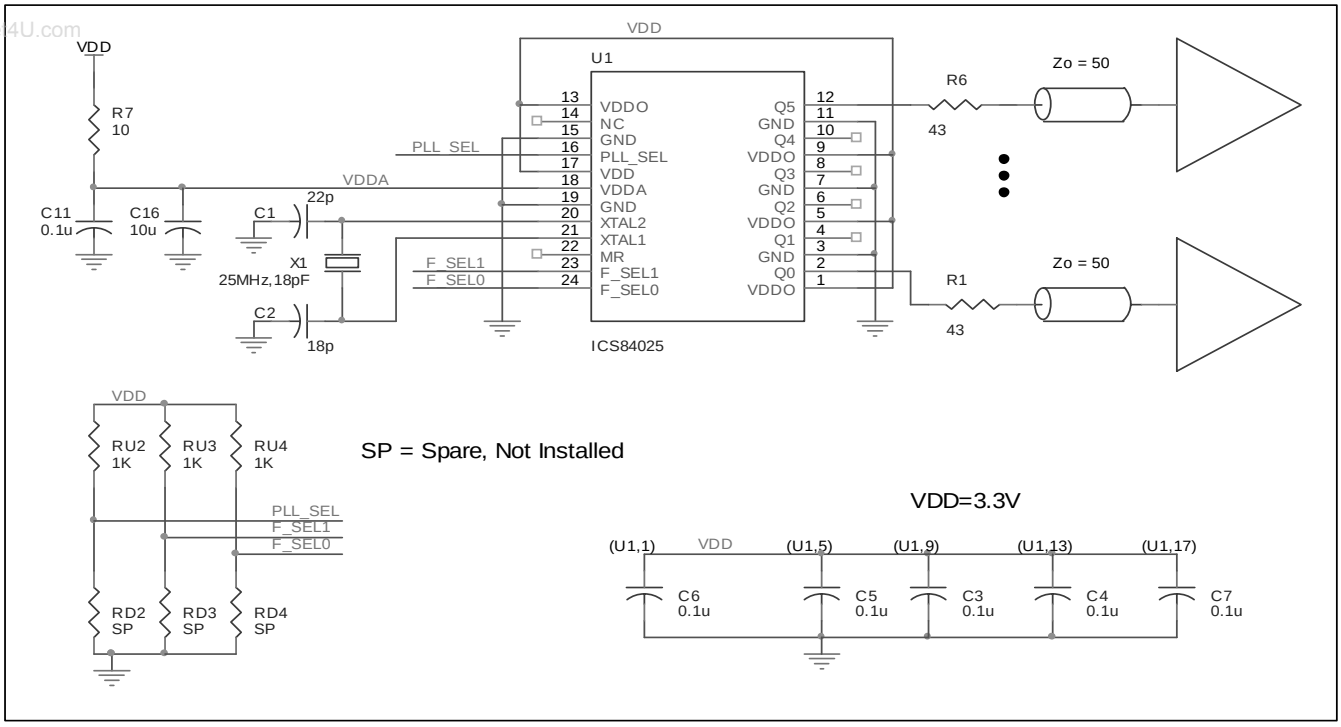


FIGURE 4A. ICS84025 SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

CRYSTAL

The crystal X1 should be located as close as possible to the pins 21 (XTAL1) and 20 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

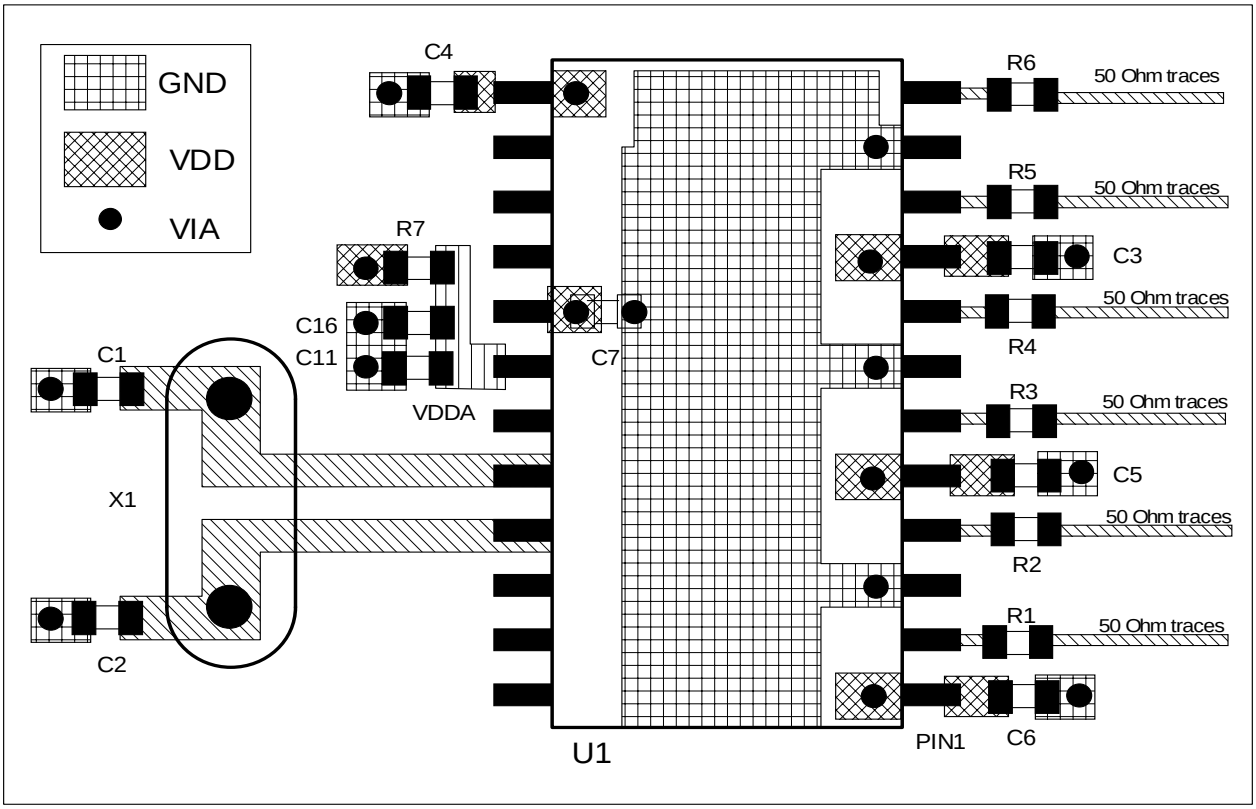


FIGURE 4B. PCB BOARD LAYOUT FOR ICS84025

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS84025 is: 2949

PACKAGE OUTLINE - M SUFFIX

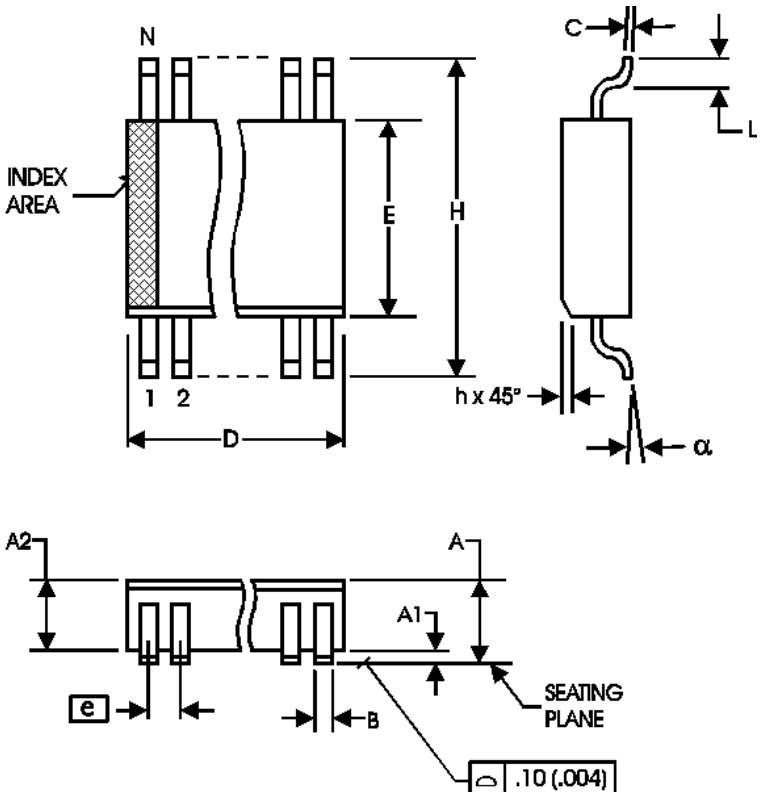


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS84025EM	ICS84025EM	24 Lead SOIC	30 per tube	0°C to 70°C
ICS84025EMT	ICS84025EM	24 Lead SOIC on Tape and Reel	1000	0°C to 70°C