Integrated Circuit Systems, Inc.

ICS840011
FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS840011 is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840011 uses a 26.5625MHz or 25MHz crystal to synthesize 106.25MHz or 100MHz respectively. The ICS840011 has excellent phase jitter performance, from 637KHz – 10MHz integration range. The ICS840011 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 LVCMOS/LVTTL output, 7Ω output impedence

- Crystal oscillator interface designed for a 26.5625MHz or 25MHz, 18pF parallel resonant crystal

- Output frequency: 106.25MHz (typical)

- VCO range: 560MHz to 680MHz

- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637KHz - 10MHz): 0.780ps (typical)

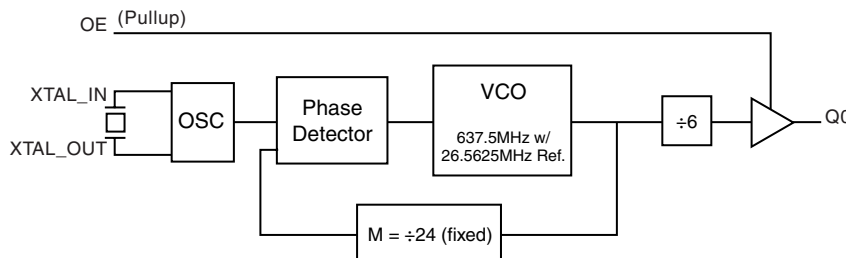- RMS phase noise at 106.25MHz (typical)

  Phase noise:

Offset	Noise Power
100Hz	-95.7 dBc/Hz
1KHz	-121 dBc/Hz
10KHz	-129 dBc/Hz
100KHz	-129.6 dBc/Hz

- 3.3V operating supply
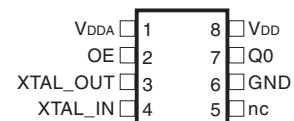
- -30°C to 85°C ambient operating temperature

FREQUENCY TABLE

Inputs	Output Frequency (MHz)
Crystal Frequency (MHz)	
26.5625	106.25
25	100

BLOCK DIAGRAM

PIN ASSIGNMENT

ICS840011
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	OE	Input	Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to HiZ state. LVCMOS/LVTTL interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	nc	Unused		No connect.
6	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 7Ω output impedance.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA} = 3.465V		24		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3. CONTROL FUNCTION TABLE

Control Inputs	Output
OE	Q0
0	Hi-Z
1	Active

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 4.6V

Inputs, V_I -0.5V to V_{DD} + 0.5 V

Outputs, V_O -0.5V to V_{DD} + 0.5V

Package Thermal Impedance, θ_{JA} 101.7°C/W (0 mps)

Storage Temperature, T_{STG} -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, $T_A = -30°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				10	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, $T_A = -30°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency				26.5625	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, $T_A = -30°C$ TO $85°C$

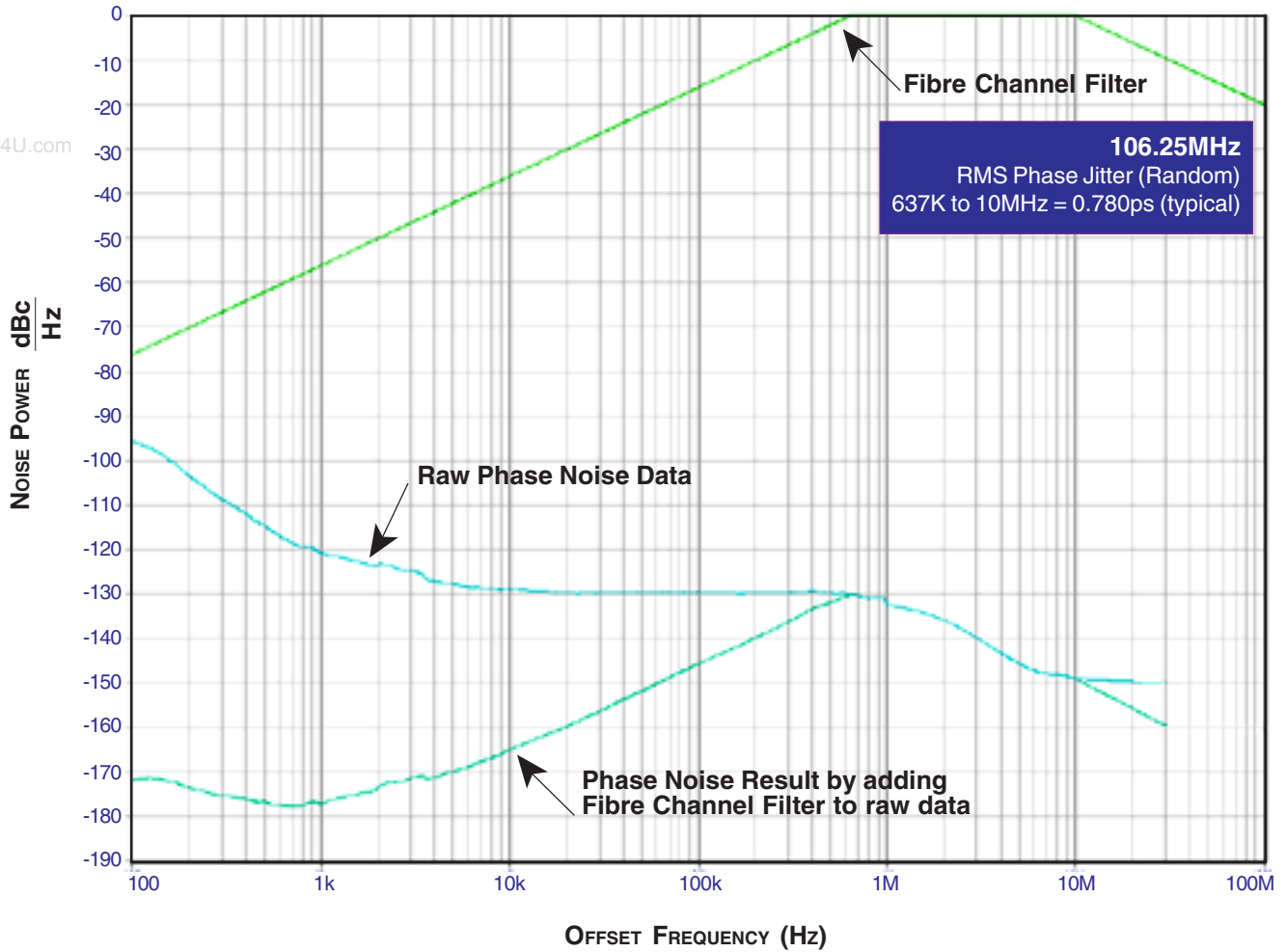| Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		93.33	106.25	113.33	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	fOUT = 106.25MHz, (637KHz to 10MHz)		0.780		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle	fOUT = 106.25MHz	48		52	%

All parameters are characterized @ 106.25MHz.
NOTE 1: Please refer to the Phase Noise Plot.

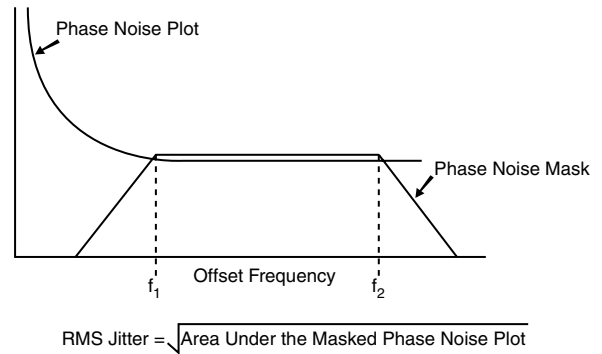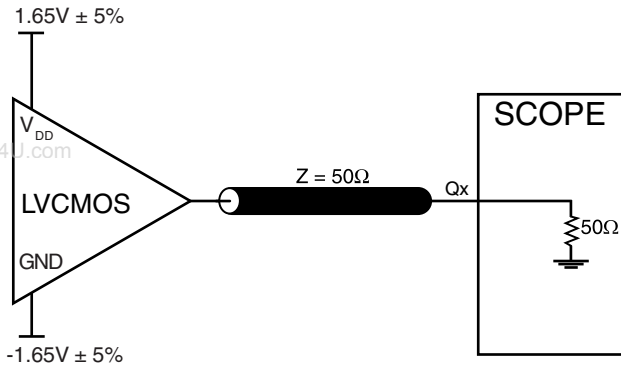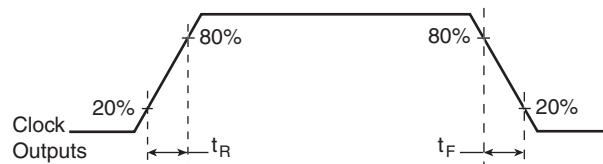Integrated
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TYPICAL PHASE NOISE AT 106.25MHz

Fibre Channel Filter

106.25MHz
RMS Phase Jitter (Random)
637K to 10MHz = 0.780ps (typical)

Raw Phase Noise Data

Phase Noise Result by adding
Fibre Channel Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

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PARAMETER MEASUREMENT INFORMATION

1.65V ± 5%

V_{DD}

LVCMOS

GND

-1.65V ± 5%

$Z = 50\Omega$

Qx

SCOPE

50Ω

3.3V OUTPUT LOAD AC TEST CIRCUIT

Phase Noise Plot

Phase Noise Mask

f_1 Offset Frequency f_2

RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

RMS PHASE JITTER

Q0

$\dfrac{V_{DD}}{2}$

Pulse Width

t_{PERIOD}

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$
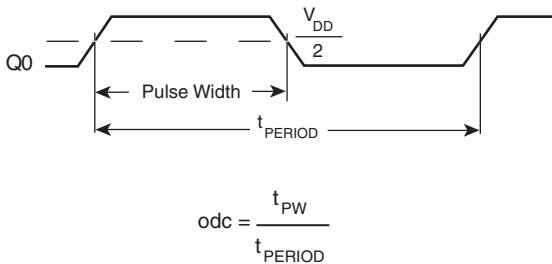
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

80%   80%

20%   20%

Clock
Outputs

t_R t_F

OUTPUT RISE/FALL TIME

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APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840011 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} pin.
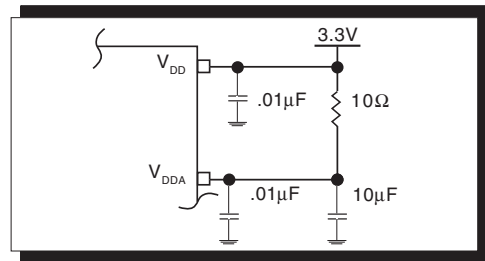
FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840011 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
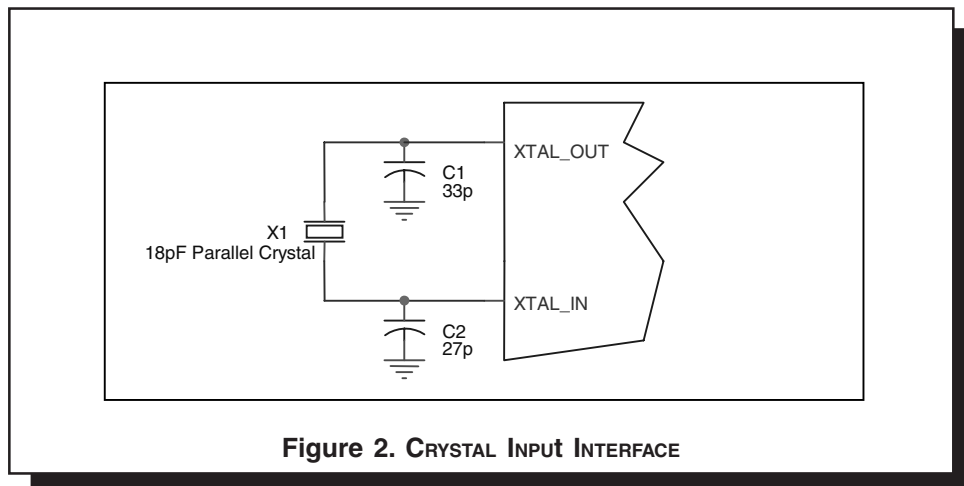

Figure 2. CRYSTAL INPUT INTERFACE

ICS840011

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APPLICATION SCHEMATIC

Figure 3A shows a schematic example of the ICS840011. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 26.5625MHz crystal is used for generating 106.25MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.
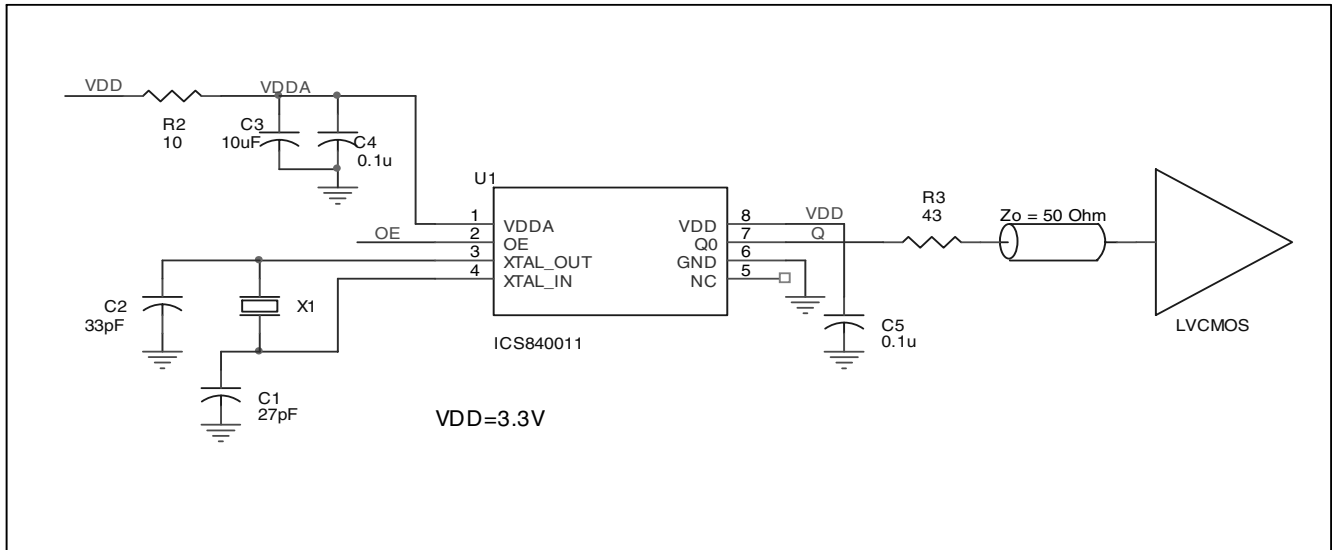
FIGURE 3A. ICS840011 SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of P.C. board layout. The crystal X1 footprint in this example allows either surface mount (HC49S) or through hole (HC49) package. C3 is 0805. C1 and C2 are 0402. Other resistors and capacitors are 0603. This layout assumes that the board has clean analog power and ground planes.
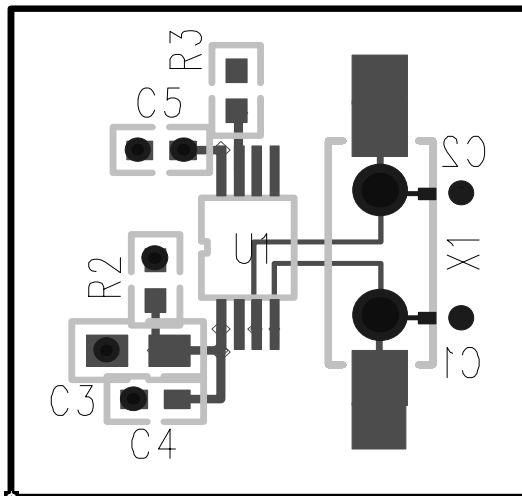

FIGURE 3B. ICS840011 PC BOARD LAYOUT EXAMPLE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} **VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

	θ_{JA} by Velocity (Meters Per Second)		
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS840011 is: 1521

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PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

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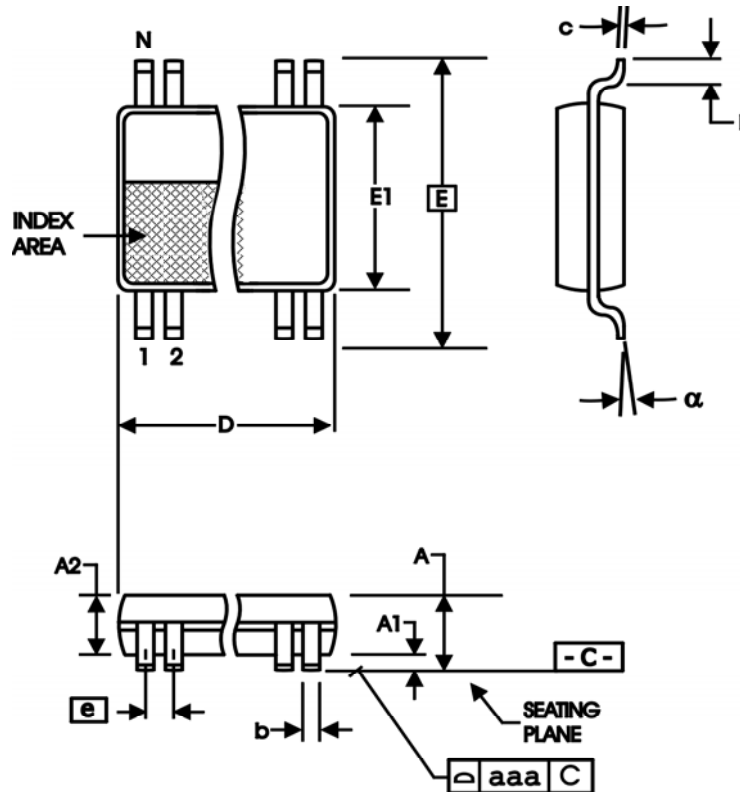
TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS840011AG	011A	8 lead TSSOP	100 per tube	-30°C to 85°C
ICS840011AGT	011A	8 lead TSSOP on Tape and Reel	2500	-30°C to 85°C
ICS840011AGLN	011AN	8 lead "Lead Free Annealed" TSSOP	100 per tube	-30°C to 85°C
ICS840011AGLNT	011AN	8 lead "Lead Free Annealed" TSSOP on Tape and Reel	2500	-30°C to 85°C

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		REVISION HISTORY SHEET		
Rev	Table	Page	Description of Change	Date
A	T9	10	Ordering Information Table - corrected count from 154 per tube to 100.	10/15/04