

## 32M (2M x 16-bit) and (4M x 8-bit) Mask ROM

### ■ DESCRIPTION

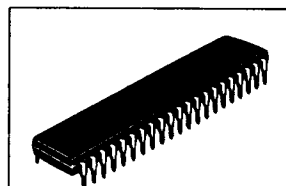
The Hitachi HN624032 is a 32-Megabit CMOS Mask Programmable Read Only Memory organized as 2,097,152 x 16-bit and 4,194,304 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

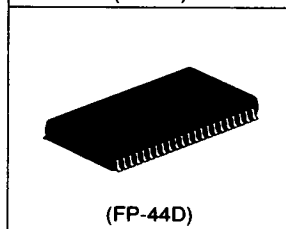
Hitachi's HN624032 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic SOP packages.

### ■ FEATURES

- Single Power Supply:  
 $V_{CC} = 5\text{ V} \pm 10\%$
- Fast Access Times:  
150 ns/200 ns (max)
- Low Power Consumption:  
Active Current: 200 mW (typ)  
Standby Current: 5  $\mu$ W (typ)
- User Selectable Organization:  
2M x 16-bit (Word-Wide)  
4M x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:  
42-pin Plastic DIP  
44-lead Plastic SOP



(DP-42)



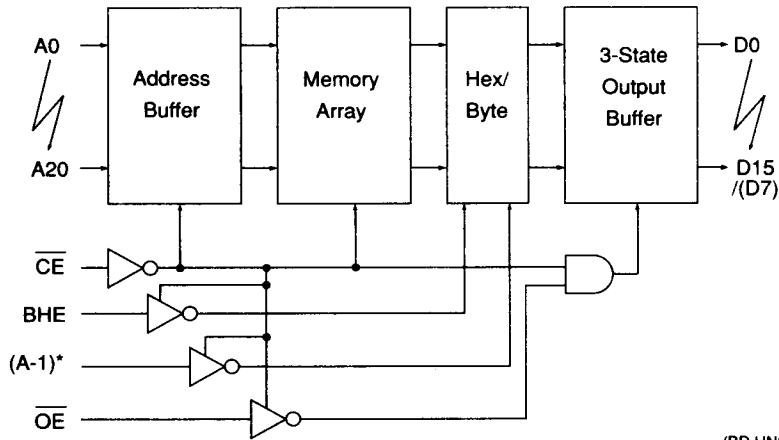
(FP-44D)

### ■ ORDERING INFORMATION

| Type No.      | Access Time | Package            |
|---------------|-------------|--------------------|
| HN624032P-15  | 150 ns      | 42-pin Plastic DIP |
| HN624032P-20  | 200 ns      | (DP-42)            |
| HN624032FB-15 | 150 ns      | 44-pin Plastic SOP |
| HN624032FB-20 | 200 ns      | (FP-44D)           |

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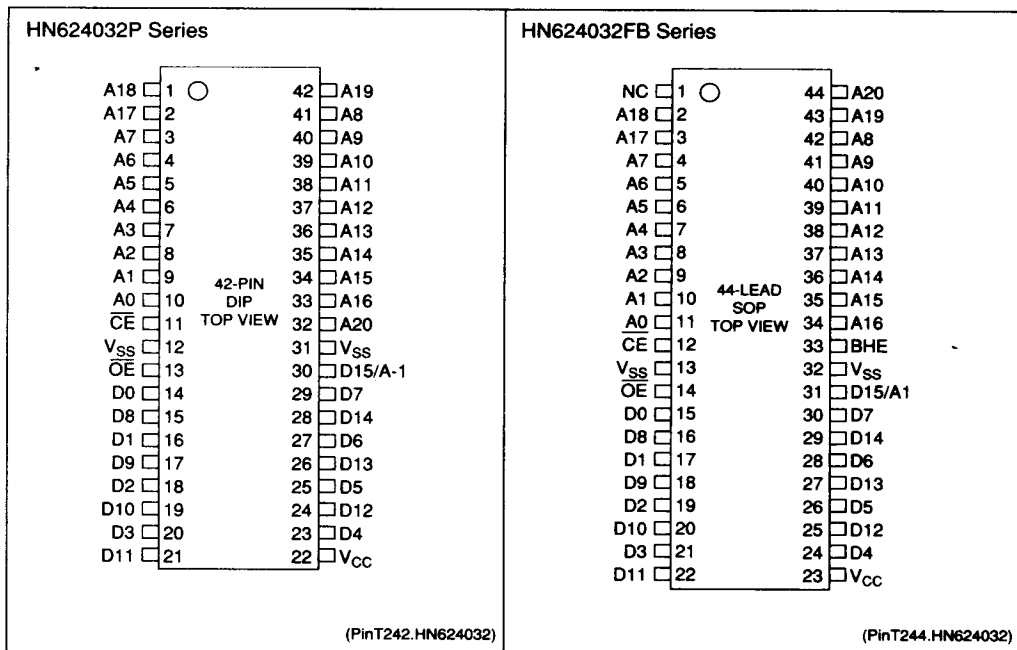
## ■ BLOCK DIAGRAM



(BD.HN624032)

- Notes:
1. \* :  $A_1$  is the Least Significant Address bit in Byte-Wide Mode.
  2.  $BHE = V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE = V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
 When BHE is low,  $D_{14} - D_8$  are in high impedance states.

## PIN ARRANGEMENT



## PIN DESCRIPTION

| Pin Name                         | Function            |
|----------------------------------|---------------------|
| A <sub>0</sub> - A <sub>20</sub> | Address             |
| A <sub>-1</sub>                  | Address (Word-Wide) |
| D <sub>0</sub> - D <sub>15</sub> | Output              |
| CE                               | Chip Enable         |
| OE                               | Output Enable       |
| BHE                              | Byte Enable         |
| V <sub>CC</sub>                  | Power Supply        |
| V <sub>SS</sub>                  | Ground              |
| NC                               | No Connection       |

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### ■ ABSOLUTE MAXIMUM RATINGS

| Item                                      | Symbol     | Value                  | Unit |
|-------------------------------------------|------------|------------------------|------|
| Supply Voltage <sup>1</sup>               | $V_{CC}$   | -0.3 to +7.0           | V    |
| All Input and Output Voltage <sup>1</sup> | $V_T$      | -0.3 to $V_{CC} + 0.3$ | V    |
| Operating Temperature Range               | $T_{OPR}$  | 0 to +70               | °C   |
| Storage Temperature Range                 | $T_{STG}$  | -55 to +125            | °C   |
| Temperature Under Bias                    | $T_{BIAS}$ | -20 to +85             | °C   |

Note: 1. Relative to  $V_{SS}$ .

### ■ CAPACITANCE

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $V_{IN} = 0V$ ,  $f = 1MHz$ )

| Item                            | Symbol    | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------|------|------|------|------|
| Input Capacitance <sup>1</sup>  | $C_{IN}$  | -    | -    | 15   | pF   |
| Output Capacitance <sup>1</sup> | $C_{OUT}$ | -    | -    | 15   | pF   |

Note: 1. This parameter is sampled and not 100% tested.

### ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $+70^\circ C$ )

| Item                       | Symbol   | Min. | Typ. | Max.           | Unit    | Test Condition                                           |
|----------------------------|----------|------|------|----------------|---------|----------------------------------------------------------|
| Input Leakage Current      | $I_{LI}$ | -    | -    | 10             | $\mu A$ | $V_{IN} = 0$ to $V_{CC}$                                 |
| Output Leakage Current     | $I_{LO}$ | -    | -    | 10             | $\mu A$ | $\overline{CE} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$       |
| Operating $V_{CC}$ Current | $I_{CC}$ | -    | -    | 100            | mA      | $V_{CC} = 5.5V$ , $ID_{OUT} = 0mA$ , $t_{RC} = min.$     |
| Standby $V_{CC}$ Current   | $I_{SB}$ | -    | -    | 30             | $\mu A$ | $V_{CC} = 5.5V$ , $\overline{CE} \geq V_{\infty} - 0.2V$ |
| Input Voltage              | $V_{IH}$ | 2.2  | -    | $V_{CC} + 0.3$ | V       |                                                          |
|                            | $V_{IL}$ | -0.3 | -    | 0.8            | V       |                                                          |
| Output Voltage             | $V_{OH}$ | 2.4  | -    | -              | V       | $I_{OH} = -205 \mu A$                                    |
|                            | $V_{OL}$ | -    | -    | 0.4            | V       | $I_{OL} = 1.6mA$                                         |

**■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**
 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0V, T_a = 0 \text{ to } +70^\circ\text{C})$ 
**Test Conditions**

- Input pulse levels: 0.8 / 2.4V
- Input rise and fall times:  $\leq 10 \text{ ns}$
- Output load: 1 TTL Gate +  $CL = 100 \text{ pF}$  (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

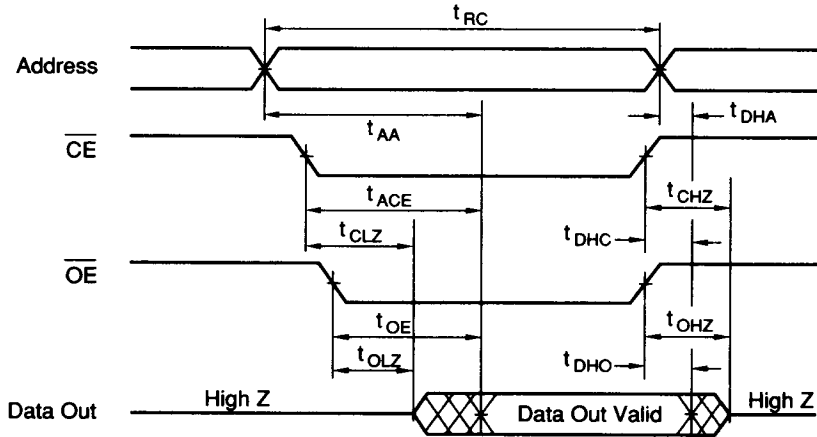
| Item                                           | Symbol    | HN624032-15 |      | HN624032-20 |      | Unit |
|------------------------------------------------|-----------|-------------|------|-------------|------|------|
|                                                |           | Min.        | Max. | Min.        | Max. |      |
| Read Cycle Time                                | $t_{RC}$  | 150         | -    | 200         | -    | ns   |
| Address Access Time                            | $t_{AA}$  | -           | 150  | -           | 200  | ns   |
| Chip Enable Access Time                        | $t_{ACE}$ | -           | 150  | -           | 200  | ns   |
| Output Enable Access Time                      | $t_{OE}$  | -           | 70   | -           | 100  | ns   |
| BHE Access Time                                | $t_{BHE}$ | -           | 150  | -           | 200  | ns   |
| Output Hold Time from Address Change           | $t_{DHA}$ | 0           | -    | 0           | -    | ns   |
| Output Hold Time from Chip Enable              | $t_{DHC}$ | 0           | -    | 0           | -    | ns   |
| Output Hold Time from Output Enable            | $t_{DHO}$ | 0           | -    | 0           | -    | ns   |
| Output Hold Time from BHE                      | $t_{DHB}$ | 0           | -    | 0           | -    | ns   |
| Chip Enable to Output in High-Z <sup>1</sup>   | $t_{CHZ}$ | -           | 70   | -           | 70   | ns   |
| Output Enable to Output in High-Z <sup>1</sup> | $t_{OHZ}$ | -           | 70   | -           | 70   | ns   |
| BHE to Output in High-Z <sup>1</sup>           | $t_{BHZ}$ | -           | 70   | -           | 70   | ns   |
| Chip Enable to Output in Low-Z                 | $t_{CLZ}$ | 10          | -    | 10          | -    | ns   |
| Output Enable to Output in Low-Z               | $t_{OLZ}$ | 10          | -    | 10          | -    | ns   |
| BHE to Output in Low-Z                         | $t_{BLZ}$ | 10          | -    | 10          | -    | ns   |

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

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■ READ TIMING WAVEFORM

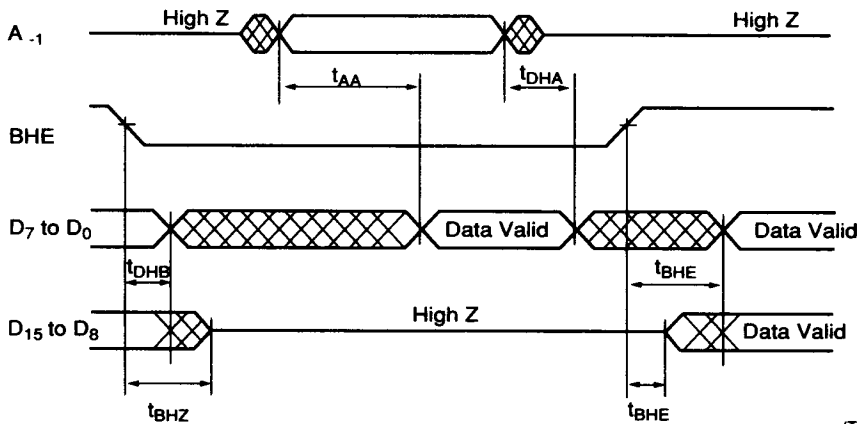
Word Mode ( $\text{BHE} = V_{\text{H}}$ ) or Byte Mode ( $\text{BHE} = V_{\text{L}}$ )



(TD.R.624032)

- Note:
1.  $t_{\text{DHA}}$ ,  $t_{\text{DHC}}$ ,  $t_{\text{DHO}}$  are determined by the faster time.
  2.  $t_{\text{AA}}$ ,  $t_{\text{ACE}}$ ,  $t_{\text{OE}}$  are determined by the slower time.
  3.  $t_{\text{CLZ}}$ ,  $t_{\text{OLZ}}$  are determined by the slower time.

Word Mode/ Byte Mode Switch



(TD.RI.HN624032)

- Note:
1. If  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are enabled,  $A_{20}$  to  $A_0$  are valid.
  2.  $D_{15}/A_{-1}$  pin is in the output state when  $\text{BHE}$  is high,  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.