Microtech
SEMICONDUCTORS

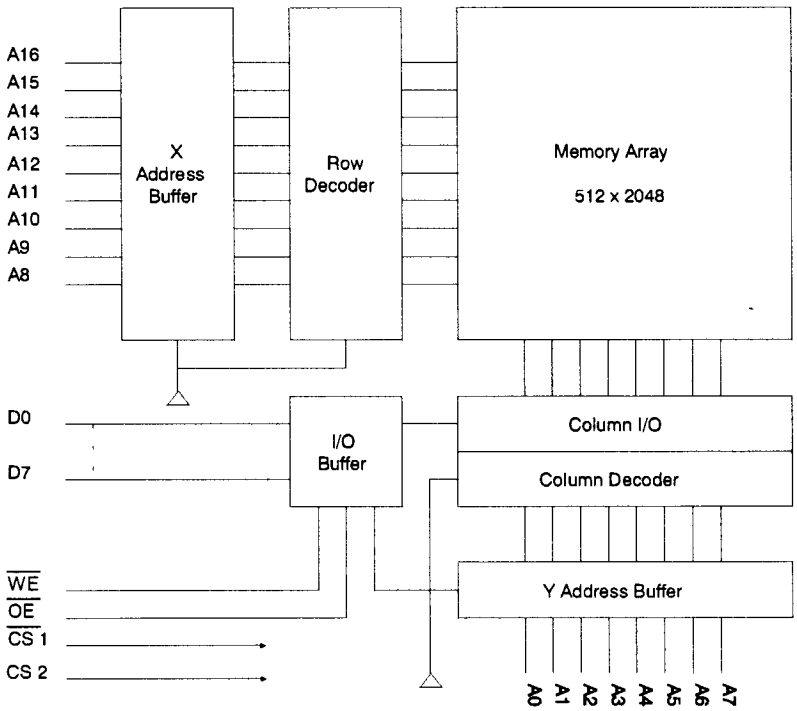
MS58128
- 35 / 45 / 55

1,048,576 bit High Speed CMOS Static RAM Module

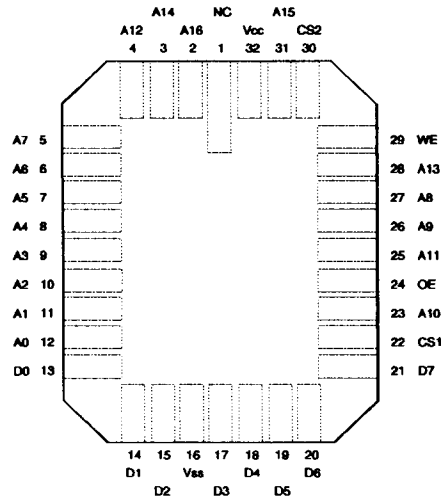
Features

- Full Military temperature range
- Very fast access times - 35/45/55ns
- Low power standby - 50μW (typical)
- Low power operation - 150mW (typical)
- Static operation - no clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible, all inputs and outputs

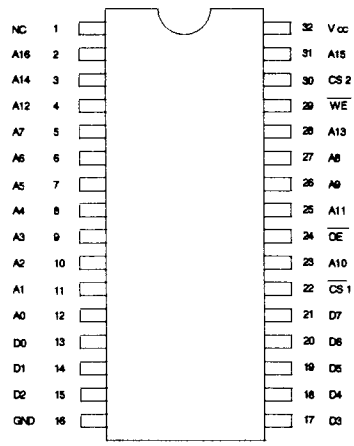
Block Diagram



Pin Assignments



32 pin LCC



32 pin DIL and 32 pin Flat-Pack

Pin Functions

A0-A16	Address inputs
D0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
V_{CC}	Power (+5V)
GND	Ground

General Description

The MS58128 is a high speed 128K x 8 bit CMOS static RAM for use in high speed and low-power applications. The device operates from a single 5V supply, is fabricated using silicon-gate CMOS technology and is available in a variety of speeds and package styles.

Maximum ratings, absolute values (1)

		Min.	Max.	Unit
V_{CC}	Supply voltage (2)	-0.5	+7.0	Volts
V_{IN}	Input voltage (2)	-0.5	V_{CC} + 0.5	Volts
$V_{IN/OUT}$	Input/ Output voltage (2)	-0.5	V_{CC} + 0.5	Volts
P_{tot}	Power dissipation		+1.0	Watts
T_{amb}	Operating temperature	-55	+125	°C
Tstg	Storage temperature	-65	+150	°C

Notes:
1. All voltage values are referenced to GND.
2. V_{CC}, V_{IN}, $V_{IN/OUT}$ = - 3.5V minimum for pulse width ≤ 20ns.

Static Electrical Characteristics(1)

		Test Conditions	Min.	Max.	Units
V_{IL}	Low level, input voltage			0.8	Volts
V_{IH}	High level, input voltage		2.2		Volts
$\|I_{IL}\|$	Input leakage current	V_{IN} = GND to V_{CC}		2.0	µA
$\|I_{LO}\|$	Output leakage current	$\overline{CS1}$ = V_{IH} or $\overline{OE}$ = V_{IH} or WE = V_{IL} or CS2 = V_{IL} $V_{I/O}$ = GND to V_{CC}		2.0	mA
I_{CC1}	Operating power supply current	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH} $I_{I/O}$ = 0mA, V_{IN} = V_{IL} or V_{IH}		80	mA
I_{CC2}	Average operating supply current	Minimum cycle, duty = 100%, $I_{I/O}$ = 0mA		120	mA
I_{SB1}	Standby power supply current	$\overline{CS1}$ ≥ V_{CC} - 0.2V or CS2 ≤ 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	2.0	mA	
I_{SB2}	Standby power supply current	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL} V_{IN} = V_{IL} or V_{IH}		15	mA
V_{OL}	Low level output voltage	I_{OL} = 8.0mA		0.4	Volts
V_{OH}	High level output voltage	-I_{OH} = 4.0mA	2.4		Volts

Note:
1. All limits over specified temperature and voltage range (unless otherwise stated)

Operating Conditions (1)

		Min.	Max.	Units
V_{CC}	Supply voltage	4.5	5.5	Volts
V_{IL}	Low-level input voltage (2)	-0.3	0.8	Volts
V_{IH}	High-level input voltage	2.2	V_{CC} + 0.3	Volts
t_{AA}	Address access time (option -35)		35	nS
t_{AA}	Address access time (option -45)		45	nS
t_{AA}	Address access time (option -55)		55	nS
T_{amb}	Operating temperature ambient	-55	+125	°C

Notes:
1. The obove are recommended conditions of use and the given values apply over the full operating temperature range. All voltages are referenced to the GND terminal.
2. V_{IL} = -3.0V minimum for pulse width ≤ 20nS.

Read Cycle (1)

		-35		-45		-55		
		Min	Max	Min	Max	Min	Max	Units
t_{RC}	Read cycle time	35		45		55		nS
t_{AA}	Address access time		35		45		55	nS
t_{ACS}	Chip select access time		35		45		55	nS
t_{OE}	Output enable to output valid		20		25		30	nS
t_{OH}	Output hold from address change	5		5		5		nS
t_{CLZ}	Chip select to output low Z	5		5		5		nS
t_{OLZ}	Output select to output low Z	0		0		0		nS
t_{CHZ}	Chip deselection to output high Z	0	15	0	20	0	25	nS
t_{PU}	Chip enable to power up time	0		0		0		nS
t_{SPD}	Chip enable to power down time	35		45		55		nS

Note:
1. All limits over specified temperature and voltage range (unless otherwise stated).

Key

Don't care

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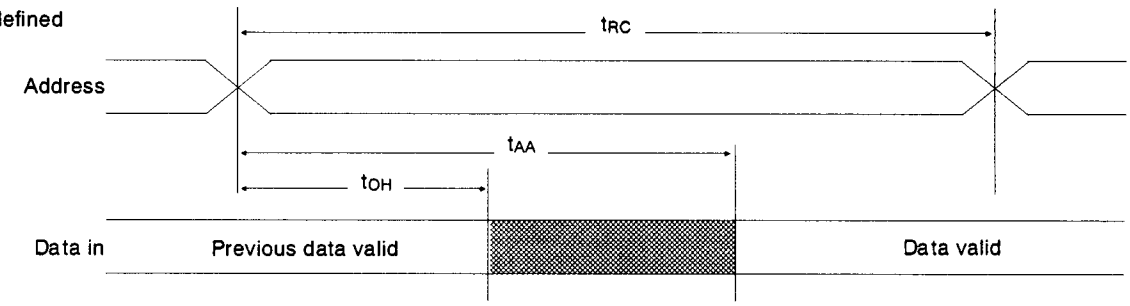

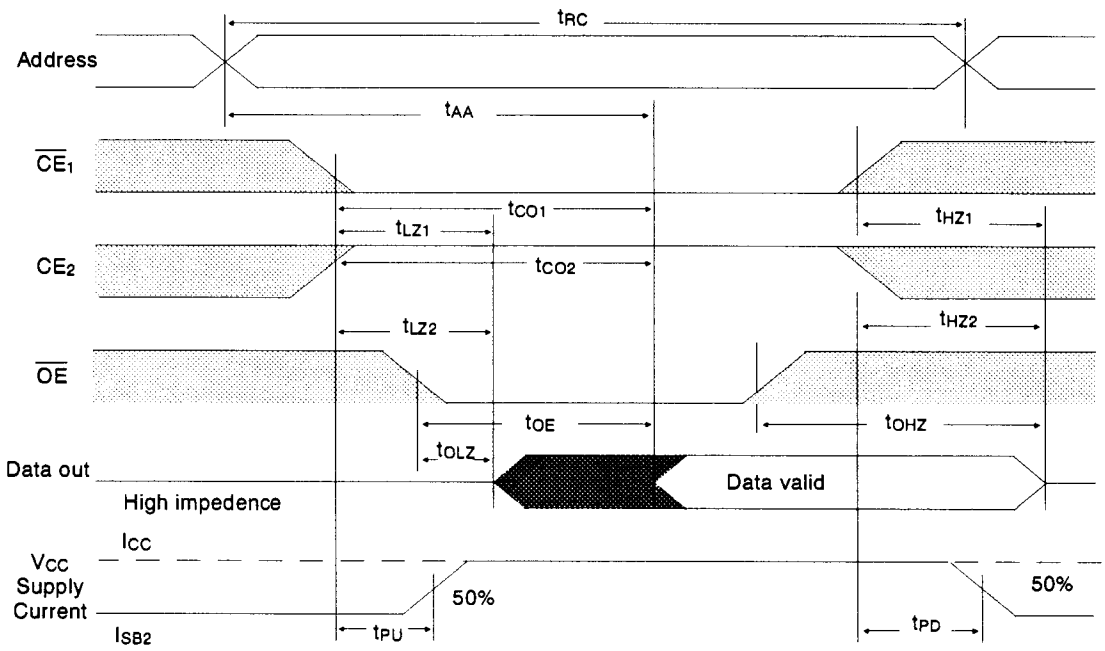

Write Cycle (1)

		-35		-45		-55		
		Min	Max	Min	Max	Min	Max	Units
t_{WC}	Write cycle time	35		45		55		nS
t_{AW}	Address valid to end of write	30		40		45		nS
t_{CW}	Chip enable to end of write	30		40		45		nS
t_{DW}	Data to write time overlap	18		20		25		nS
t_{DH}	Data hold from write time	0		0		0		nS
t_{WP}	Writ epulse width	30		35		40		nS
t_{AS}	Address set up time	0		0		0		nS
t_{WR1}	Write recovery time from $\overline{WE}$ or $\overline{CS1}$	3		3		3		nS
t_{WR2}	Write recovery time (CS2)	5		5		5		nS
t_{OW}	Output active from end of write	5		5		5		nS
t_{WHZ}	Write to utput in high Z	0	15	0	15	0	15	nS

Note:
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Key

Don't care

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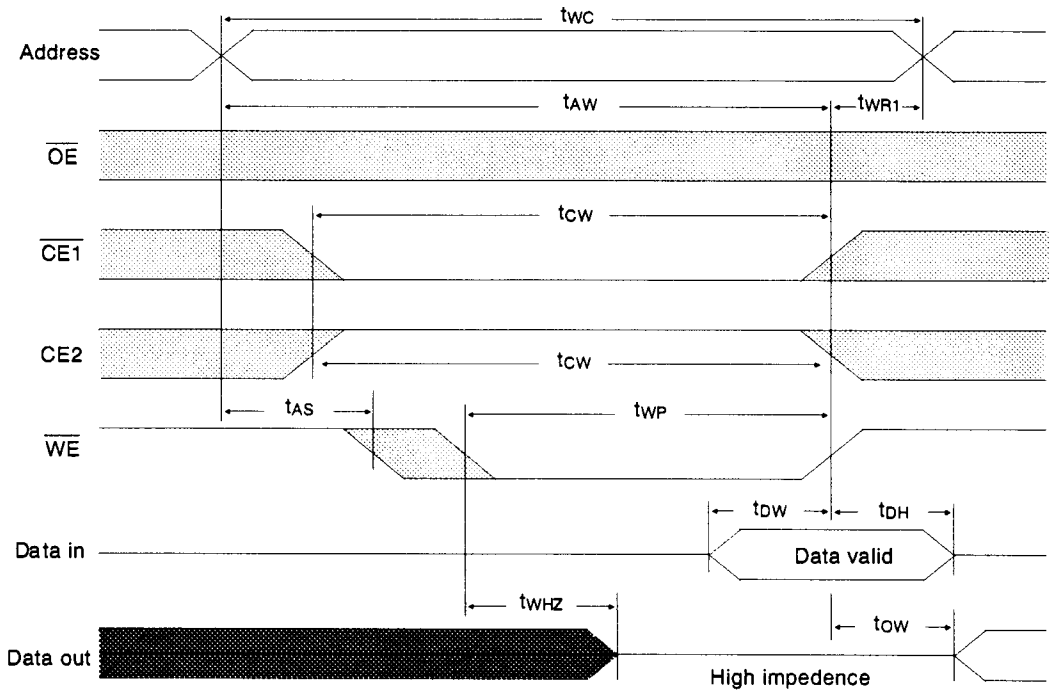
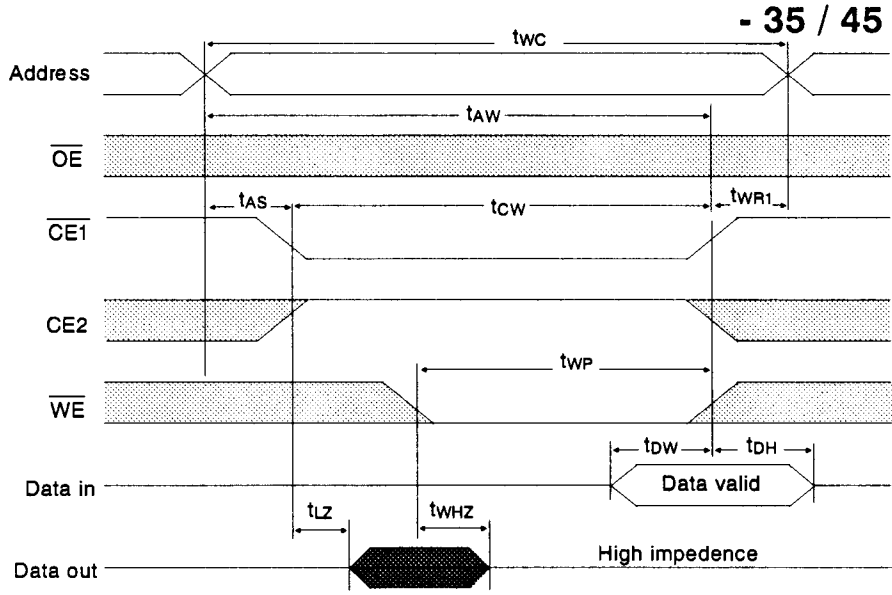
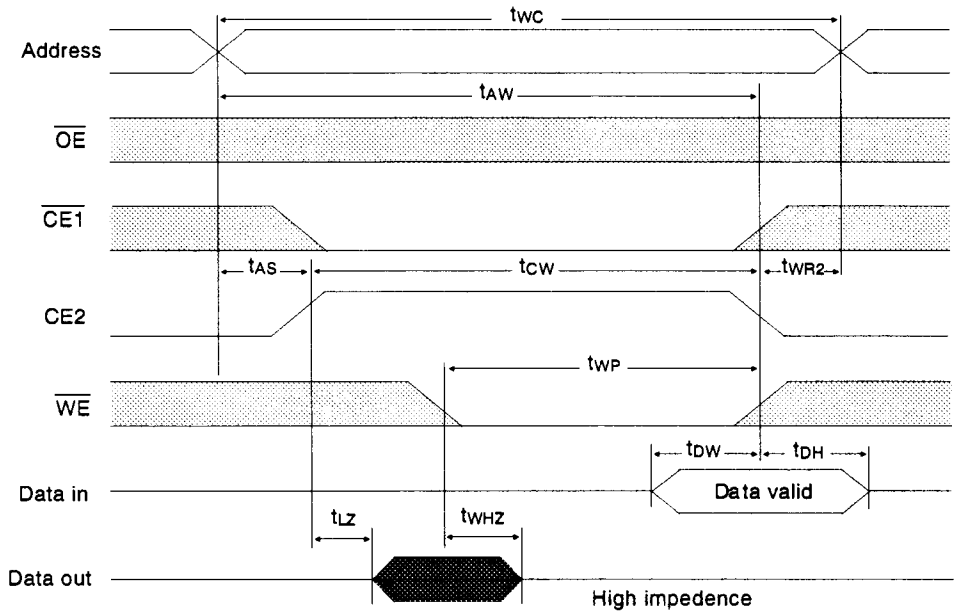






Truth table

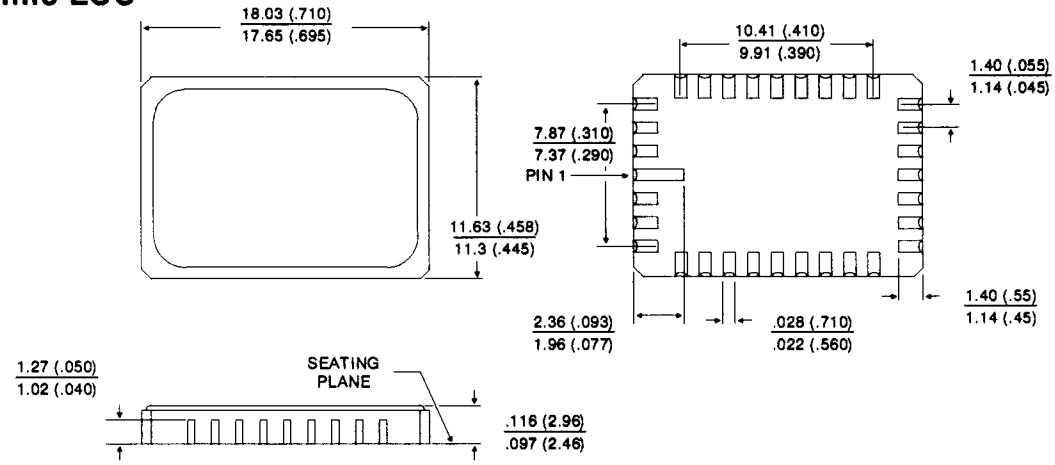
Mode	$\overline{OE}$	$\overline{CS1}$	CS2	$\overline{WE}$	Outputs	V_{CC} Current
Not Selected	X	H	X	X	High Z	I_{SB1}, I_{SB2}
Not Selected	X	X	L	X	High Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High Z	I_{CC1}, I_{CC2}
Read	L	L	H	H	D_{OUT}	I_{CC1}, I_{CC2}
Write	X	L	H	L	D_{IN}	I_{CC1}, I_{CC2}

Note:
H = High, L = Low, X = H or L

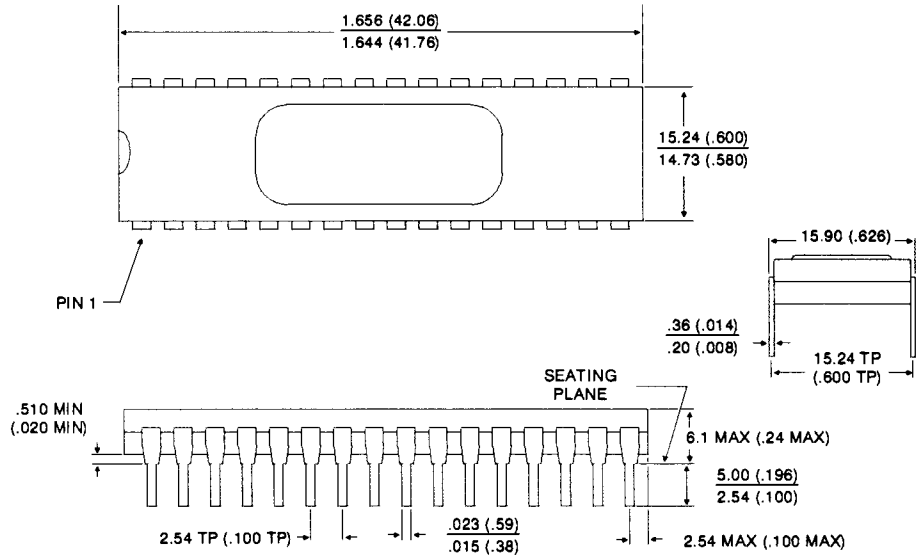
I/O Capacitance

		Min.	Max.	Units
C_{IN}	Input capacitance @ T_{amb} = 25°C, f = 1MHz		7	pF
$C_{I/O}$	I/O capacitance		7	pF

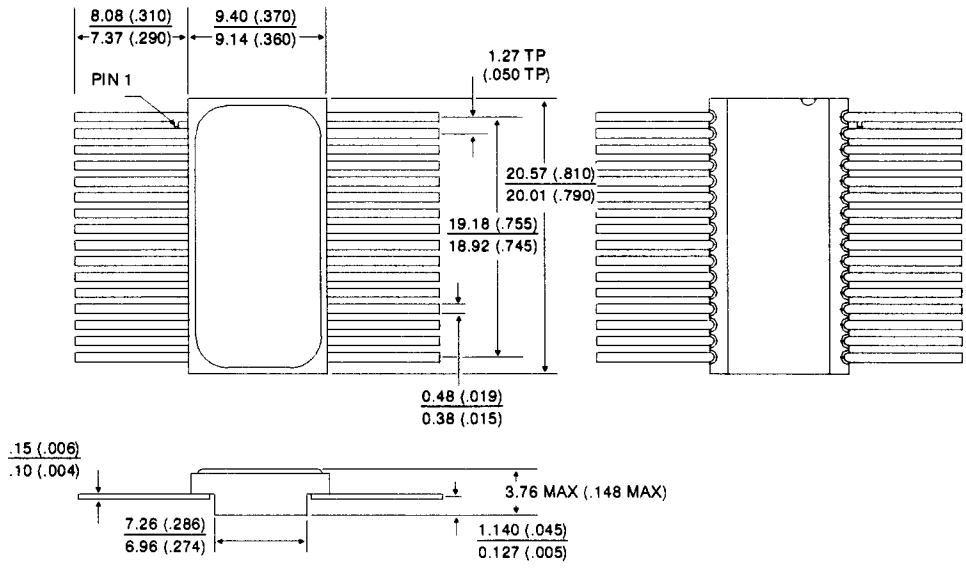
32-Lead Ceramic LCC

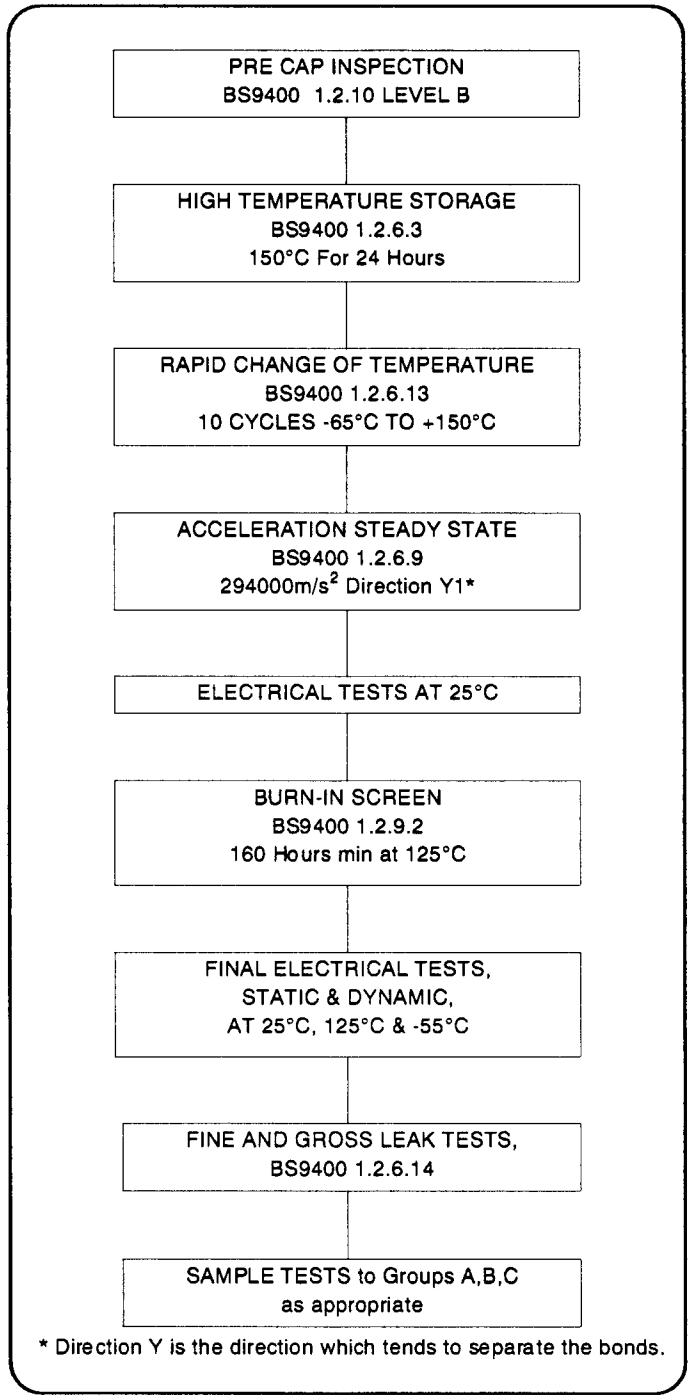


32-Lead 600mil Sidebraze DIL



32-Lead Flat Pack

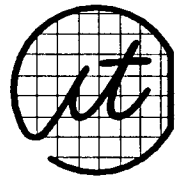




Ordering Information

MS5 8128 J - 55

- MS5: CMOS Ultra Fast Static RAM
- 8128: 128K X 8
- J: Package Style : J = 32 pin ceramic DIL; W = 32 pin ceramic LCC; F = 32 pin ceramic Flat-Pack
- 55: Speed : - 35ns, - 45ns, - 55ns



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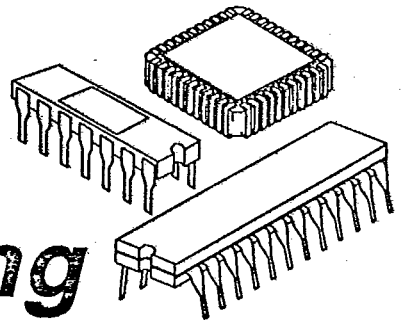

Custom Packaging

Microtech Semiconductors are leaders in Custom assembly, with our considerable expertise in production and test, we can satisfy the most complex requirement.

We are equipped to assemble virtually any hermetic package style - LCC, JLCC, Quad Pack, PGA & SOT 23 to name but a few. Using proven techniques, such as multichip or multicavity design, our expert engineering, with class 1000 cleanroom assembly and final test, assures quality results.

From commercial to space applications Microtech Semiconductors will support your assembly needs.

MICROTECH

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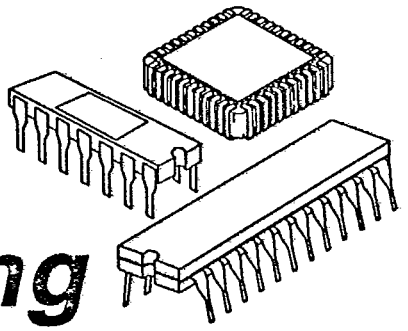

Custom Packaging

Approved to CECC and BS9000, hallmarks of European quality, MICROTECH Semiconductors is totally committed to total quality. Dedicated to supporting the high-reliability equipment manufacturer, our integrated circuits are produced in Class 1000 cleanroom conditions. Final optical inspection takes place under better than Class 100 laminar flow and our impressive range of environmental and electrical test equipment ensures that we release high performance components with no compromise on reliability.