NEC

User's Manual

IE-784225-NS-EM1

Emulation Board

Target devices

μPD784216A Subseries
μPD784218A Subseries
μPD784225 Subseries
μPD784216AY Subseries
μPD784218AY Subseries
μPD784225Y Subseries

Document No. U13742EJ2V0UM00 (2nd edition)
Date Published March 2002 N CP(K)

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J01.12

Major Revisions in This Edition

Page	Description
p.12	Modification of figure and description in **Figure 1-1 System Configuration**
p.15	Modification of description in **Table 1-1 Basic Specifications**
p.20	Addition of **3.3 Selection of Emulator Main Unit**
p.22	Modification of description in **3.4.2 Main system clock settings**
p.27	Modification of description in **3.4.3 Subsystem clock settings**
p.46	Modification of title and description in **APPENDIX B**
p.48	Addition of **APPENDIX C REVISION HISTORY**

The mark ★ shows major revised points.

INTRODUCTION

Product Overview

The IE-784225-NS-EM1 is designed to be used with the IE-78K4-NS to debug the following target devices that belong to the 78K/IV Series of 16-bit single-chip microcontrollers.

- μPD784216A Subseries: μPD784214A, 784215A, 784216A, 78F4216A
- μPD784216AY Subseries: μPD784214AY, 784215AY, 784216AY, 78F4216AY
- μPD784218A Subseries: μPD784217A, 784218A, 78F4218A
- μPD784218AY Subseries: μPD784217AY, 784218AY, 78F4218AY
- μPD784225 Subseries: μPD784224, 784225, 78F4225
- μPD784225Y Subseries: μPD784224Y, 784225Y, 78F4225Y

Target Readers

This manual is intended for engineers who will use the IE-784225-NS-EM1 with the IE-78K4-NS to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-784225-NS-EM1, refer to not only this manual (supplied with the IE-784225-NS-EM1) but also the manual that is supplied with the IE-78K4-NS.

IE-78K4-NS User's Manual	IE-784225-NS-EM1 User's Manual
• Basic specifications • System configuration • External interface functions	• General • Part names • Installation • Differences between target devices and target interface circuits

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-784225-NS-EM1.

Terminology The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K4-NS and the IE-784225-NS-EM1.

Conventions

Data significance: Higher digits on the left and lower digits on the right
Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information

Related Documents The related documents (user's manuals) indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
IE-78K4-NS		U13356E
IE-784225-NS-EM1		This manual
ID78K Series Integrated Debugger Ver. 2.30 or Later Windows™ Based	Operation	U15185E
μPD784216A, 784218A, 784216AY, 784218AY Subseries	Hardware	U13570E
μPD784225, 784225Y Subseries	Hardware	U12697E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL

The IE-784225-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K/IV Series of 16-bit single-chip microcontrollers.

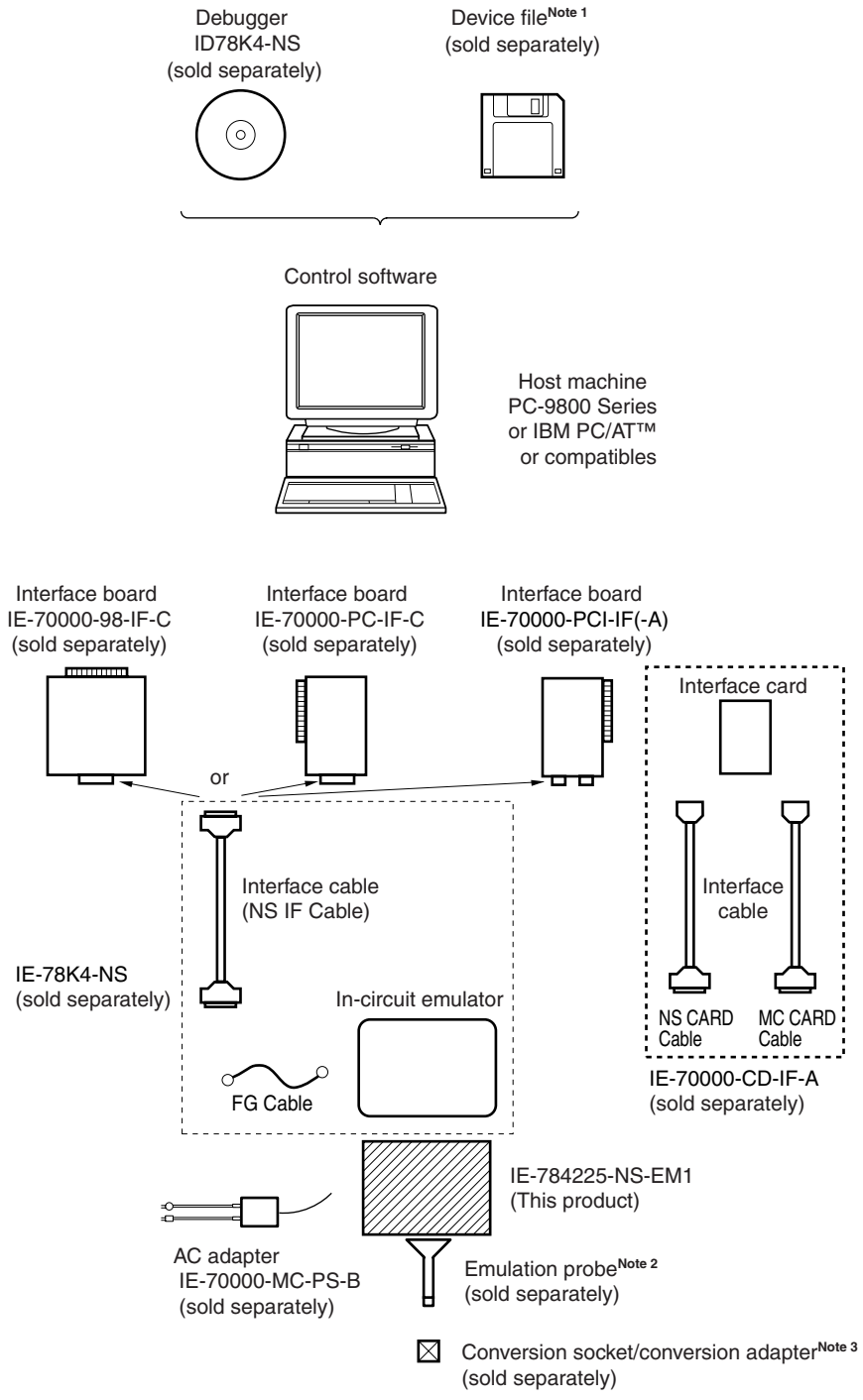
This chapter describes the IE-784225-NS-EM1's system configuration and basic specifications.

- Target devices
  - μPD784216A Subseries
  - μPD784216AY Subseries
  - μPD784218A Subseries
  - μPD784218AY Subseries
  - μPD784225 Subseries
  - μPD784225Y Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-784225-NS-EM1's system configuration.

★ **Figure 1-1. System Configuration**



Notes 1. The device file is as follows, in accordance with the subseries.

μSxxxxDF784218: μPD784216A, 784216AY, 784218A, 784218AY Subseries

μSxxxxDF784225: μPD784225, 784225Y Subseries

★ The device file can be downloaded from the website of NEC Electron Devices (http://www.ic.nec.co.jp/micro/).

2. The emulation probe is as follows, in accordance with the package.

NP-80GC: 80-pin plastic QFP (GC-8BT type)

NP-80GK: 80-pin plastic TQFP (GK-BE9 type)

NP-100GC: 100-pin plastic LQFP (GC-7EA type)

NP-100GF: 100-pin plastic QFP (GF-3BA type)

The NP-80GC, NP-80GK, NP-100GC, and NP-100GF are products of Naito Densei Machida Mfg. Co., Ltd.

★ For further information, contact Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-45-475-4191)

3. The conversion socket/conversion adapter are as follows, in accordance with the package.

EV-9200GK-80: 80-pin plastic TQFP (GK-BE9 type)

EV-9200GF-100: 100-pin plastic QFP (GF-3BA type)

TGC-080SDW: 80-pin plastic LQFP (GC-8BT type)

TGC-100SDW: 100-pin plastic LQFP (GC-7EA type)

The TGC-080SDW and TGC-100SDW are products of TOKYO ELETECH CORPORATION.

For further information, contact Daimaru Kogyo Co., Ltd.

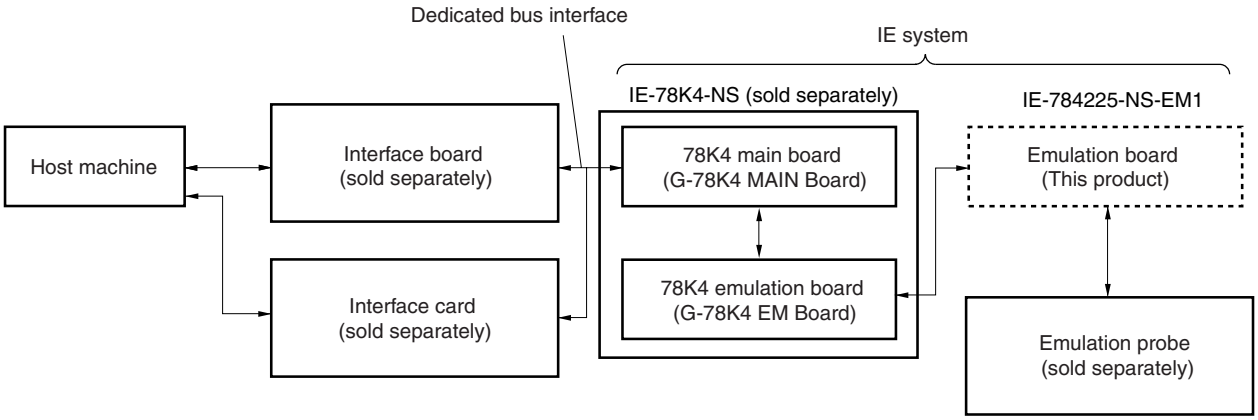
Tokyo Electronics Department (TEL: +81-3-3820-7112)

Osaka Electronics Department (TEL: +81-6-6244-6672)

1.2 Hardware Configuration

Figure 1-2 shows the IE-784225-NS-EM1's position in the basic hardware configuration.

Figure 1-2. Basic Hardware Configuration



1.3 Basic Specifications

The IE-784225-NS-EM1's basic specifications are listed in Table 1-1.

★ **Table 1-1. Basic Specifications**

Parameter	Description
Target device	μPD784216A, 784218A, 784216AY, 784218AY, 784225, 784225Y Subseries
System clock	12.5 MHz
Main clock supply	External: Input via an emulation probe from the target system Internal: Mounted on emulation board (25 MHz), or mounted on the board by the user
Subclock supply	External: Input via an emulation probe from the target system Internal: Mounted on emulation board (32.768 kHz), or mounted on the board by the user
Low-voltage support	3 V or higher (same as target device)

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-784225-NS-EM1 main unit.

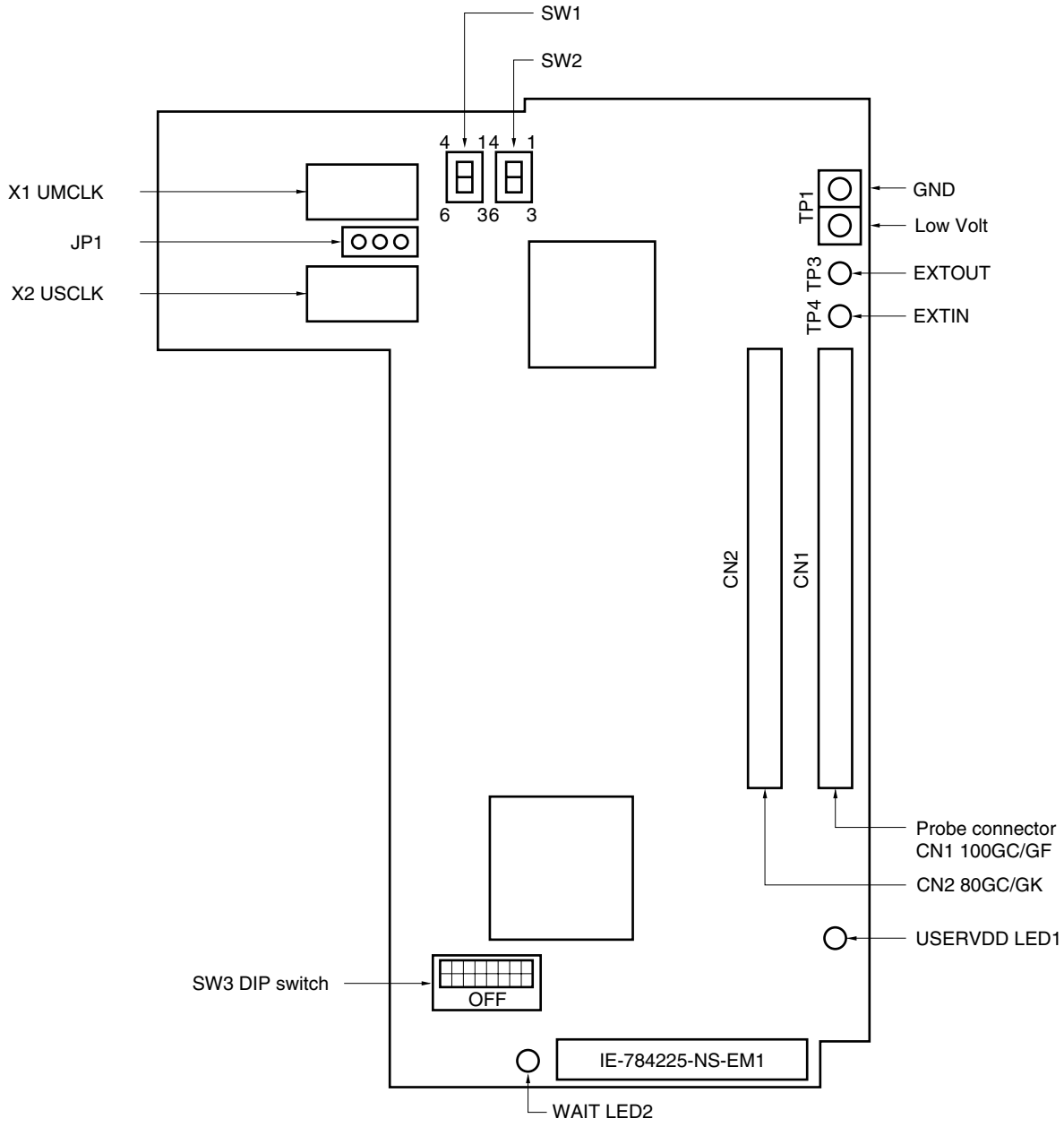
The packing box contains the emulation board (IE-784225-NS-EM1).

If there are any missing or damaged items, please contact an NEC sales representative.

Fill out and return the guarantee document that comes with the main unit.

2.1 Parts of Main Unit

Figure 2-1. IE-784225-NS-EM1 Part Names



CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-784225-NS-EM1 to the IE-78K4-NS, emulation probe, etc. Mode setting methods are also described.

Caution Connecting or removing components to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched OFF.

3.1 Connection

(1) Connection with IE-78K4-NS main unit

See the IE-78K4-NS User's Manual (U13356E) for a description of how to connect the IE-784225-NS-EM1 to the IE-78K4-NS.

(2) Connection with emulation probe

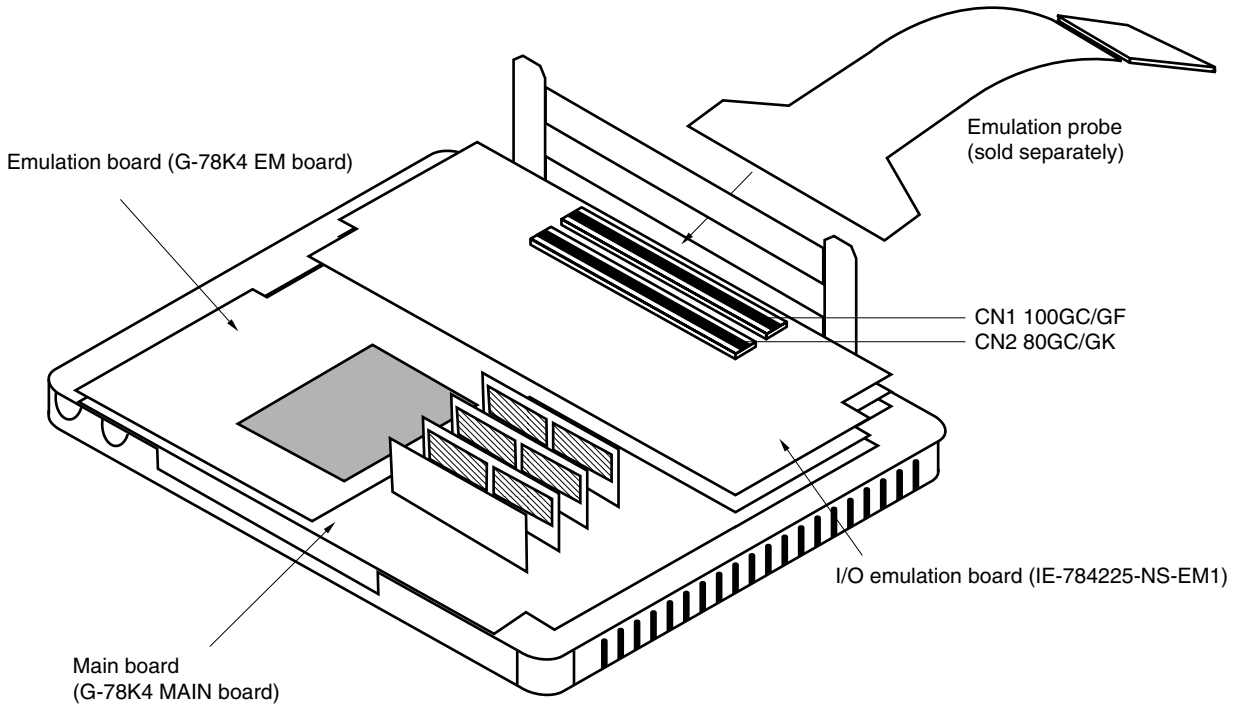
See the IE-78K4-NS User's Manual (U13356E) for a description of how to connect an emulation probe to the IE-784225-NS-EM1.

On this board, the probe connector differs depending on the emulation probe used.

- When using NP-100GC or NP-100GF, connect it to CN1.
- When using NP-80GC or NP-80GK, connect it to CN2.

Caution Incorrect connection may damage the IE system.
Be sure to read the emulation probe's user's manual for a detailed description of the connection method.

Figure 3-1. Connection of Emulation Probe



3.2 Target Device Setting

SW1 in the IE-784225-NS-EM1 must be set in accordance with the target device (the μPD784216A, 784216AY, 784218A, 784218AY, or 784225 Subseries) as follows.

μPD784216A, 784218A Subseries: Set SW1 to the 3, 6 pin side
μPD784225 Subseries: Set SW1 to the 1, 4 pin side

★ 3.3 Selection of Emulator Main Unit

SW2 in the IE-784225-NS-EM1 must be set in accordance with the emulator main unit to be used as follows.

Using IE-784225-NS-EM1 in combination with IE-78K4-NS: Set SW2 to the 3, 6 pin side (shipment setting)
Using IE-784000-R in combination with IE-784225-NS-EM1 and IE-78K4-R-EX2: Set SW2 to the 1, 4 pin side

3.4 Clock Settings

3.4.1 Overview of clock settings

The main system and subsystem clocks to be used during debugging can be selected from (1) to (3) below.

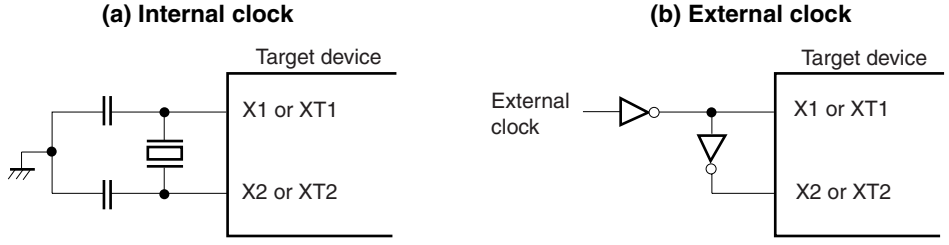
(1) Clock that is already mounted on emulation board
(2) Clock that is mounted by user
(3) External clock

If the target system includes an internal clock, select either “(1) Clock that is already mounted on emulation board” or “(2) Clock that is mounted by user”. For an internal clock, the target device is connected to a resonator and the target device’s internal oscillator is used. An example of the external circuit is shown in part (a) of Figure 3-2. During emulation, the resonator that is mounted on the target system is not used. Instead, it uses the clock that is mounted on the emulation board, which is installed for the IE-78K4-NS.

If the target system includes an external clock, select “(3) External clock”.

For an external clock, a clock signal is supplied from outside of the target device and the target device’s internal oscillator is not used. An example of the external circuit is shown in part (b) of Figure 3-2.

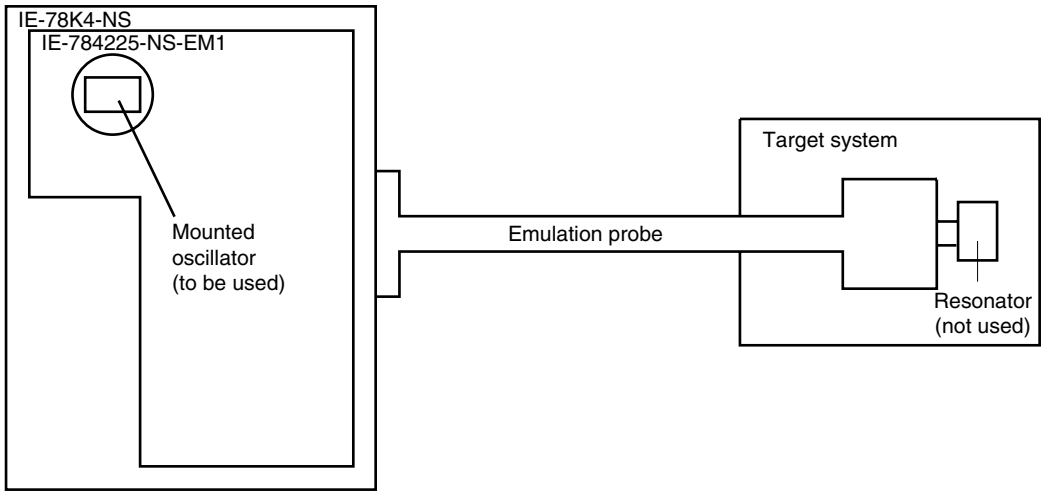
Figure 3-2. External Circuits Used as System Clock Oscillator



(1) Clock that is already mounted on emulation board

A crystal oscillator is already mounted on the emulation board. Its frequency is 25 MHz.

Figure 3-3. When Using Clock That Is Already Mounted on Emulation Board

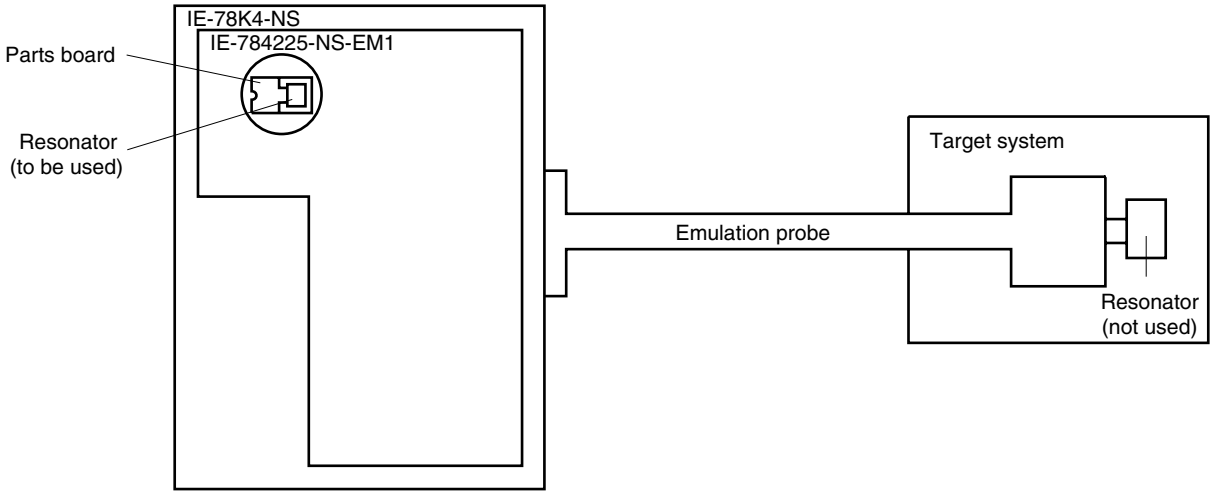


Remark The clock that is supplied by the IE-784225-NS-EM1's oscillator (encircled in the figure) is used.

(2) Clock that is mounted by user

The user is able to mount any clock supported by the set specifications on the IE-784225-NS-EM1. First mount the resonator on the parts board, then attach the parts board to the IE-784225-NS-EM1. This method is useful when using a different frequency from that of the pre-mounted clock.

Figure 3-4. When Using User-Mounted Clock

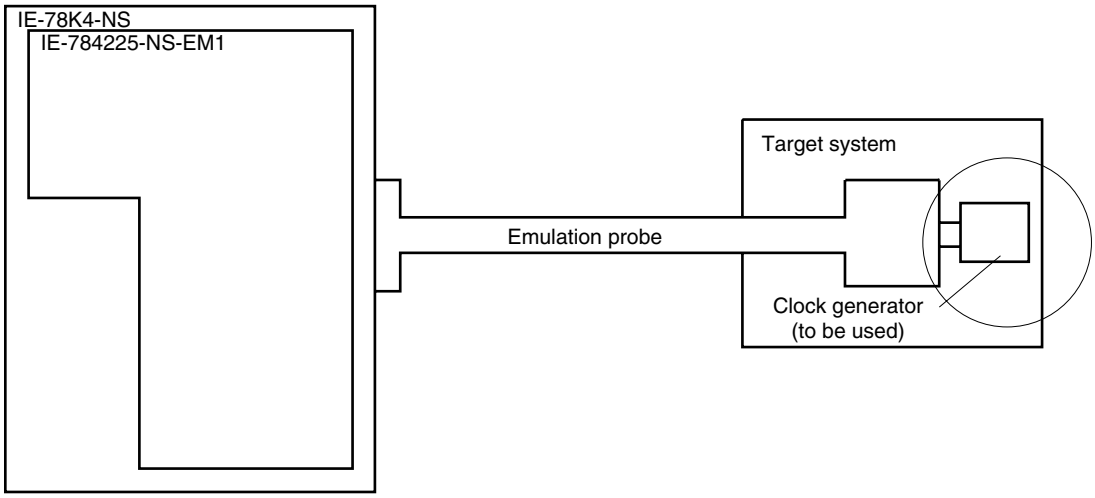


Remark The clock that is supplied by the IE-784225-NS-EM1's resonator (encircled in the figure) is used.

(3) External clock

An external clock connected to the target system can be used via an emulation probe.

Figure 3-5. When Using an External Clock



Remark The clock supplied by the target system's clock generator (encircled in the figure) is used.

3.4.2 Main system clock settings

Table 3-1. Main System Clock Settings

Frequency of Main System Clock		IE-784225-NS-EM1 Parts Board (UMCLK)	CPU Clock Source Selection (ID)
When using clock that is already mounted on emulation board	25 MHz	Oscillator used	Internal
When using clock mounted by user	Other than 25 MHz	Oscillator assembled by user	
When using external clock		Oscillator not used	External

Caution When using an external clock, open the configuration dialog box when starting the integrated debugger (ID78K4-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

Remark The IE-784225-NS-EM1's factory settings are those listed above under "when using clock that is already mounted on emulation board".

(1) When using clock that is already mounted on emulation board

When the IE-784225-NS-EM1 is shipped, a 25 MHz crystal oscillator is already mounted in the IE-784225-NS-EM1's UMCLK socket. When using the factory-set mode settings, there is no need to make any other hardware settings.

When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

(2) When using clock mounted by user

The settings described under either (a) or (b) are required, depending on the type of clock to be used.

When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

(a) When using a ceramic resonator or crystal resonator

- Items to be prepared

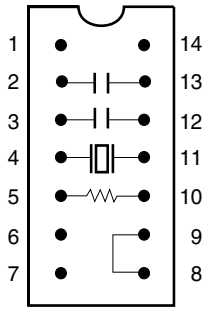
★
- Parts board
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Solder kit

<Steps>

<1> Solder the target ceramic resonator or crystal resonator, resistor Rx, capacitor CA, and capacitor ★ CB (all with a suitable oscillation frequency) onto the parts board (as shown below).

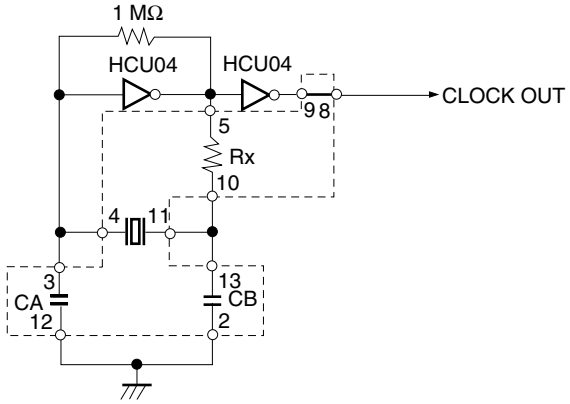
Figure 3-6. Connections on Parts Board (When Using Main System Clock or User-Mounted Clock)

Parts board (UMCLK)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator or crystal resonator
5-10	Resistor Rx
8-9	Short

Circuit diagram



Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

<2> Prepare the IE-784225-NS-EM1.

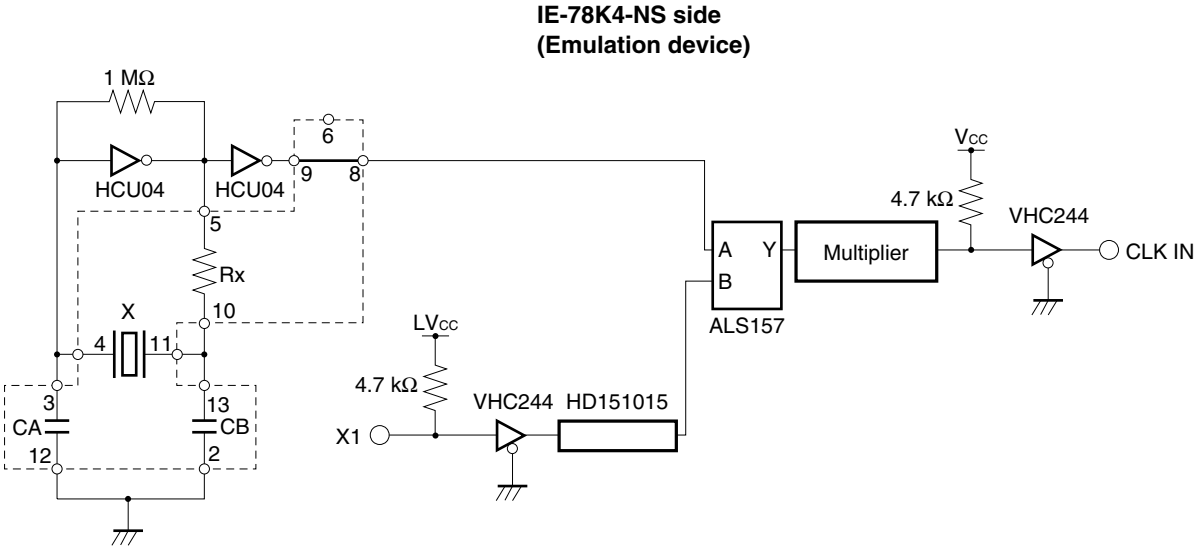
<3> Remove the crystal oscillator that is mounted in the IE-784225-NS-EM1's socket (the socket marked as UMCLK).

<4> Connect the parts board (from <1> above) to the socket (UMCLK) from which the crystal oscillator was removed (see <3> above). Check the pin 1 mark to make sure the board is mounted in the correct direction.

<5> Make sure that the parts board mounted in the UMCLK socket on the emulation board is wired as shown in Figure 3-6 above.

<6> Install the IE-784225-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted resonator to the emulation device.

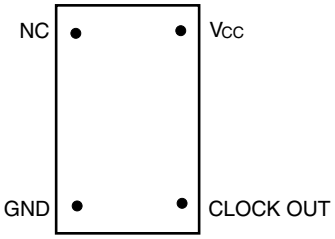


Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

(b) When using a crystal oscillator

- Items to be prepared
  - Crystal oscillator (see pinouts shown in Figure 3-7)

Figure 3-7. Crystal Oscillator (When Using Main System Clock or User-Mounted Clock)



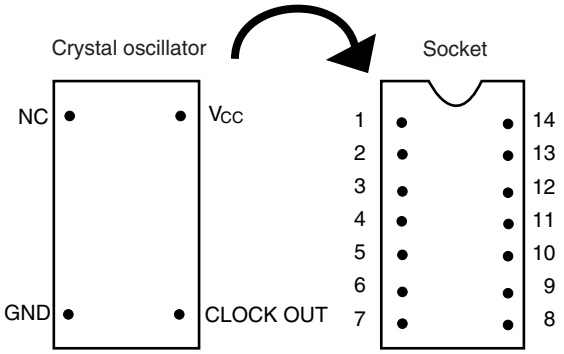
<Steps>

<1> Prepare the IE-784225-NS-EM1.

<2> Remove the crystal oscillator that is mounted in the IE-784225-NS-EM1's socket (the socket marked as UMCLK).

<3> Connect the crystal oscillator (from <2> above) to the socket (UMCLK) from which the crystal oscillator was removed. Insert the crystal oscillator pin into the socket aligning the pins as shown in the figure below.

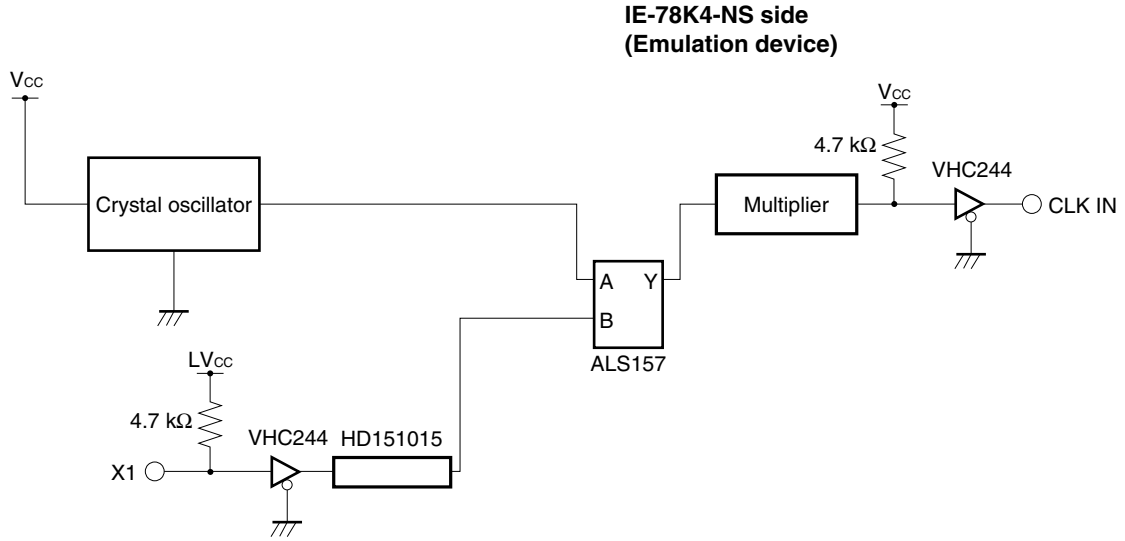
Figure 3-8. Pin Alignment of Crystal Oscillator and Socket



Crystal Oscillator Pin Name	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

<4> Install the IE-784225-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted resonator to the emulation device.



(3) When using external clock

No hardware settings are required for this situation.

When starting the integrated debugger (ID78K4-NS), open the configuration dialog box and select “External” in the area (Clock) for selecting the CPU’s clock source (this selects the user’s clock).

3.4.3 Subsystem clock settings

Table 3-2. Subsystem Clock Settings

Frequency of Subsystem Clock		IE-784225-NS-EM1	
		Parts Board (USCLK)	JP1
When using clock that is already mounted on emulation board	32.768 kHz	6 and 8 shorted	Short 1 and 2
When using clock mounted by user	Other than 32.768 kHz	Oscillator assembled by user	
When using external clock		Not used	Short 2 and 3

Caution Jumper JP1, which is used to select the board's clock or an external clock, should be set only after turning off the IE-78K4-NS's power.

Remark The IE-784225-NS-EM1's factory settings are those listed above under "when using clock that is already mounted on emulation board".

(1) When using clock that is already mounted on emulation board

When the IE-784225-NS-EM1 is shipped, a 32.768 kHz crystal resonator is already mounted on the IE-784225-NS-EM1. Pins 6 and 8 on the parts board (USCLK) are shorted. Short pins 1 and 2 on the IE-784225-NS-EM1's jumper (JP1). There is no need to make any other settings via the integrated debugger (ID78K4-NS).

(2) When using clock mounted by user

The settings described under either (a) or (b) are required, depending on the type of clock to be used. Short pins 1 and 2 on the IE-784225-NS-EM1's jumper (JP1).

There is no need to make any other settings via the integrated debugger (ID78K4-NS).

(a) When using a ceramic resonator or crystal resonator

- Items to be prepared

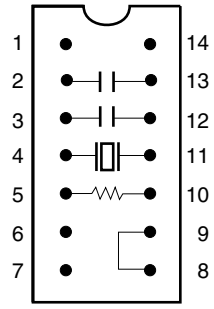
★
- Parts board
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Solder kit

<Steps>

<1> Solder the target ceramic resonator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with a suitable oscillation frequency) onto the supplied parts board (as shown below).

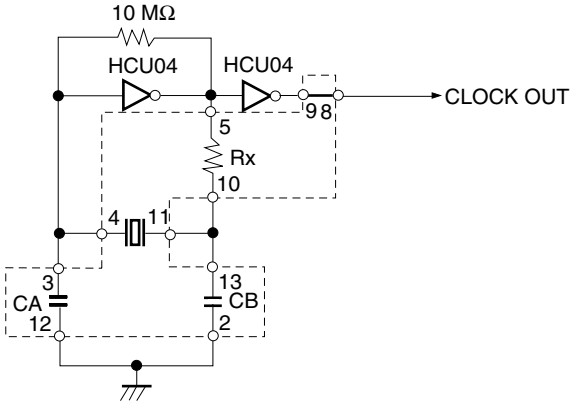
Figure 3-9. Connections on Parts Board (When Using Subsystem Clock or User-Mounted Clock)

Parts board (USCLK)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator or crystal resonator
5-10	Resistor Rx
8-9	Short

Circuit diagram



Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

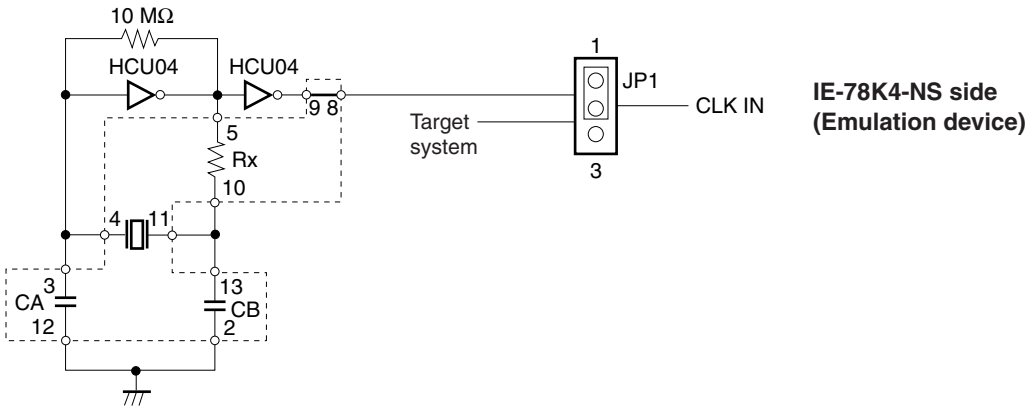
<2> Prepare the IE-784225-NS-EM1.

<3> Remove the parts board that is mounted in the IE-784225-NS-EM1's socket (the socket marked as USCLK).

<4> Connect the parts board (from <1> above) to the socket (USCLK) from which the parts board was removed (see <3> above). Check the pin 1 mark to make sure the board is mounted in the correct direction.

<5> Install the IE-784225-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted resonator to the emulation device.

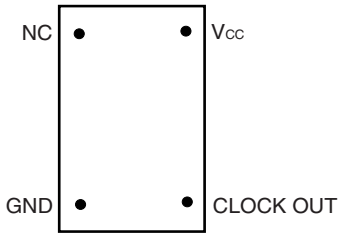


Remark The sections enclosed in broken lines indicate parts that are attached to the parts board.

(b) When using a crystal oscillator

- Items to be prepared
  - Crystal oscillator (see pinouts shown in Figure 3-10)

Figure 3-10. Crystal Oscillator (When Using Subsystem Clock or User-Mounted Clock)

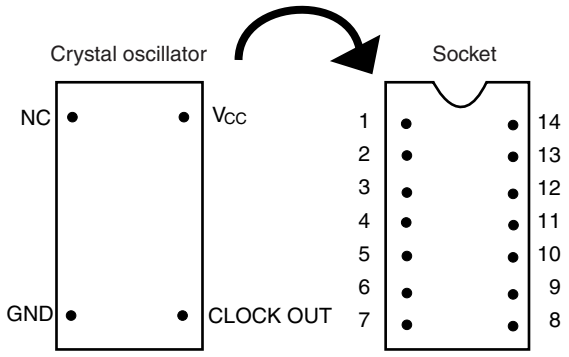


<Steps>

<1> Prepare the IE-784225-NS-EM1.

<2> Remove the parts board that is mounted in the IE-784225-NS-EM1's socket (the socket marked as USCLK).

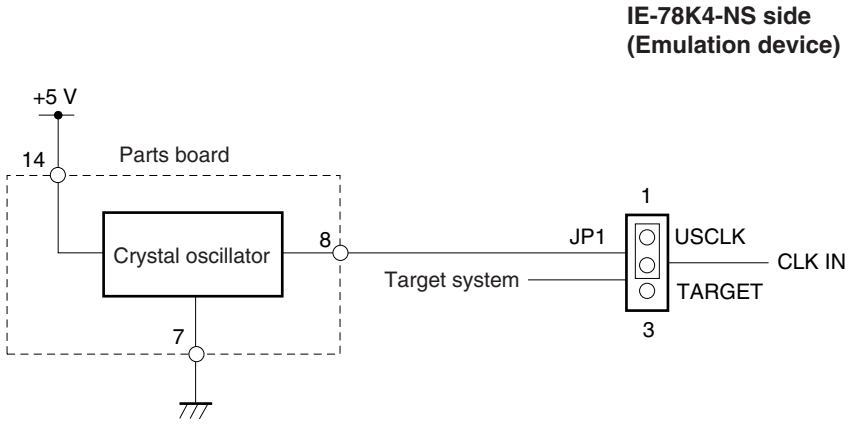
<3> Connect the crystal oscillator (from <2> above) to the socket (USCLK) from which the parts board was removed. Insert the crystal oscillator pin into the socket aligning the pins as shown below.



Crystal Oscillator Pin Name	Socket Pin No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

<4> Install the IE-784225-NS-EM1 in the IE-78K4-NS.

The above steps configure the following circuit and enable supply of the clock from the mounted oscillator to the emulation device.



(3) When using external clock

Short pins 2 and 3 on the IE-784225-NS-EM1's jumper (JP1).

There is no need to make any other settings via the integrated debugger (ID78K4-NS).

3.4.4 Slew-rate clock emulation

It is not possible to set the slew-rate clock using the ENMP bit of the CC register after the IE-784225-NS-EM1 has been activated. To use the slew-rate clock mode, switch 4 of the DIP switch (SW3) must be set as shown in Table 3-3 before power application.

Table 3-3. DIP Switch Setting When Using Slew-Rate Clock Mode

Value of ENMP Bit	DIP Switch Setting
	4
0 (initial setting)	ON
1 (slew-rate clock)	OFF

Caution The IE system may become hung up if a clock that exceeds 12.5 MHz is used when the slew-rate clock mode has been selected.
Be sure not to supply a clock exceeding 12.5 MHz to the UMCLK socket when DIP switch (SW3) 4 is OFF, as this will cause the internal clock to be selected when the IE system is activated.

3.5 Pin Mask Function Settings

3.5.1 Wait (WAIT) mask function

By setting switches 1 and 2 of DIP switch (SW3) in the IE-784225-NS-EM1, it is possible to mask the alternate function (WAIT) of pin P66 in the μPD784216A, 784218A, and 784225 Subseries.

Table 3-4. DIP Switch Setting for Wait (WAIT) Mask Function

Status	DIP Switch Setting	
	1 (WAITMSK)	2 (P66ON)
No mask (initial setting)	OFF	ON
Wait masked	ON	OFF

Caution Do not set the DIP switch to settings other than those above.

3.5.2 Wait display function setting

By setting switch 3 of the DIP switch (SW3) in the IE-784225-NS-EM1, it is possible to display the status of "waiting" with an LED light.

Table 3-5. DIP Switch Setting for Wait Display Function

Status	DIP Switch Setting
	3 (WAITLED)
Wait (WAIT) status not displayed (initial setting)	OFF
Wait (WAIT) status displayed	ON

Caution When pin P66 is used as a port pin, unless the DIP switch is turned OFF the LED may light up.

3.5.3 NMI interrupt mask setting

By setting switch 5 of the DIP switch (SW3) in the IE-784225-NS-EM1, it is possible to mask the NMI interrupt, which is the alternate function of the P02/INTP2 pin.

Table 3-6. DIP Switch Setting for NMI Interrupt Mask

Status	DIP Switch Setting
	5
No NMI mask (initial setting)	ON
NMI masked	OFF

Caution Because the NMI interrupt is the alternate function of the P02/INTP2 pin, this pin cannot operate as the P02/INTP2 pin when the NMI mask status has been set.

3.6 Low-Voltage Emulation Setting

Low-voltage emulation is possible in the IE system.

When the target system is operating on low voltage, supply the same voltage as the target system to the TP1 terminal pin of the IE-784225-NS-EM1. Set the target voltage between 3 and 5 V.

- Maximum current consumption of TP1

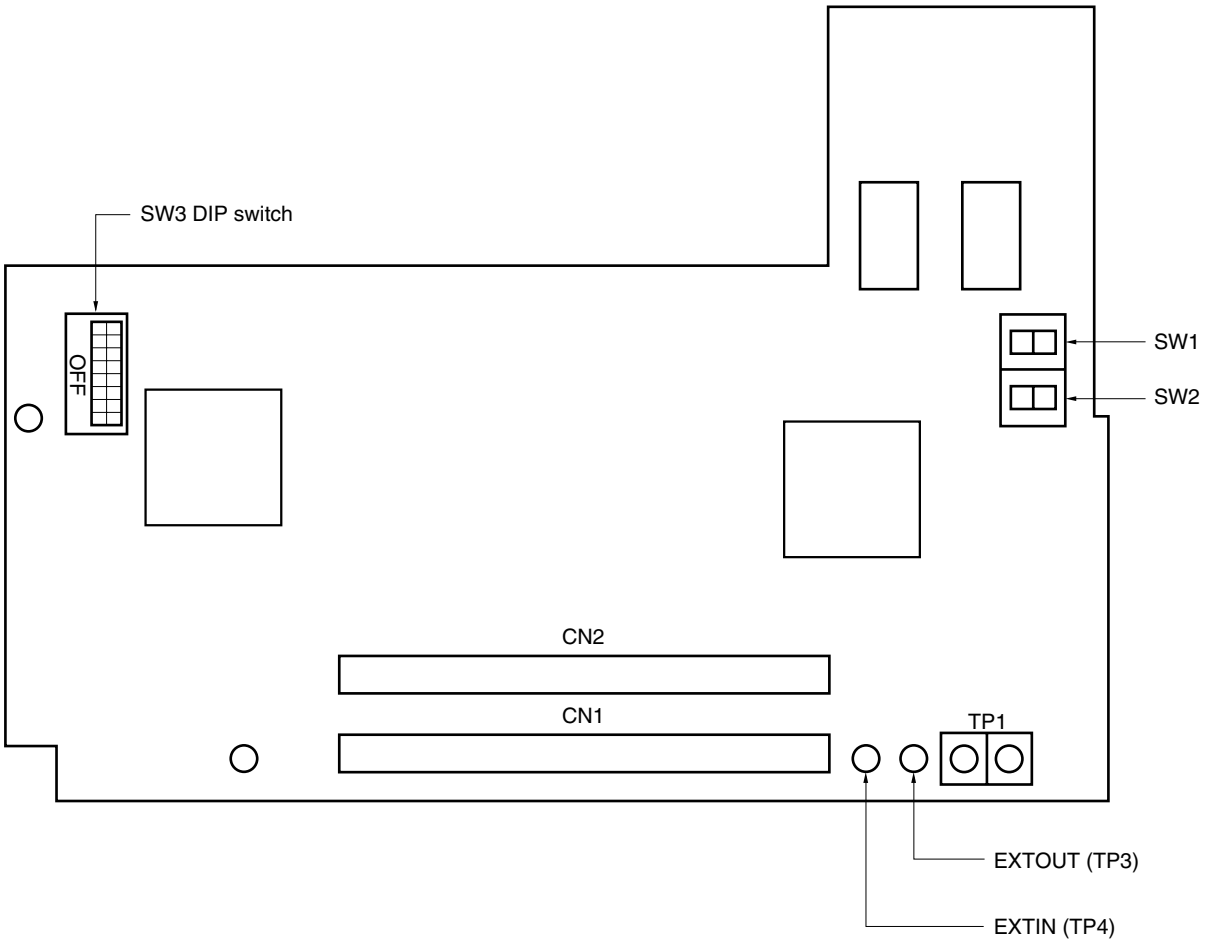
5 V	300 mA
.	.
.	.
.	.
3 V	150 mA

3.7 External Trigger

To set up an external trigger, connect it to the IE-784225-NS-EM1's check pin, EXTOUT pin, and EXTIN pin as shown below.

See the integrated debugger (ID78K4-NS) User's Manual (U12796E) for descriptions of related use methods and pin characteristics.

Figure 3-11. External Trigger Input Position



CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences between the target device's signal lines and the signal lines of the IE-784225-NS-EM1's target interface circuit.

Although the target device is a CMOS circuit, the IE-784225-NS-EM1's target interface circuit consists of an emulation CPU, TTL, CMOS-IC, and other emulation circuits.

When the IE system is connected with the target system for debugging, the IE system performs emulation so as to operate as the actual target device would operate in the target system.

However, some minor differences exist since the operations are performed via the IE system's emulation.

(1) Signals directly input/output to/from the emulation CPU
(2) Signals input from the target system via a gate
(3) Other signals

The IE system's circuit is used as follows for signals listed in (1) to (3) above.

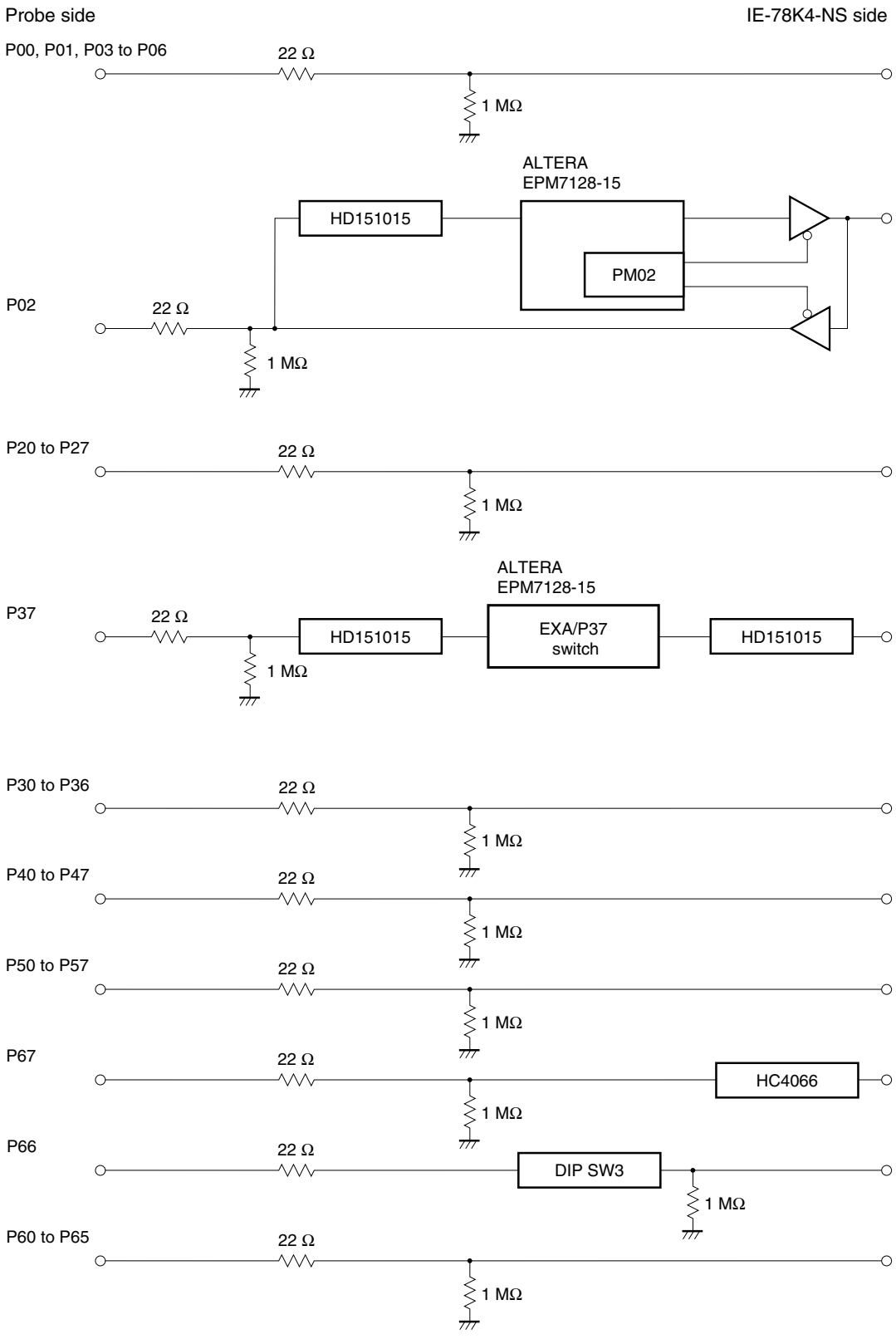
(1) Signals directly input/output to/from the emulation CPU

The following signals perform the same operations as in the μPD784216A, 784216AY, 784218A, 784218AY, and 784225 Subseries. For the signals related to ports excluding ports 1 and 13 (having alternate functions as pins for A/D and D/A converters), however, a 1 MΩ pull-down resistor and 22 Ω resistor are inserted in series.

- Signals related to port 0
- Signals related to port 1 (A/D converter input)
- Signals related to port 2
- Signals related to port 3
- Signals related to port 7
- Signals related to port 10
- Signals related to port 12
- Signals related to port 13 (D/A converter input)
- Signals related to A/D converter
  - AV_{REF0}
  - AV_{REF1}
  - AV_{SS}
  - AV_{DD}[Note]

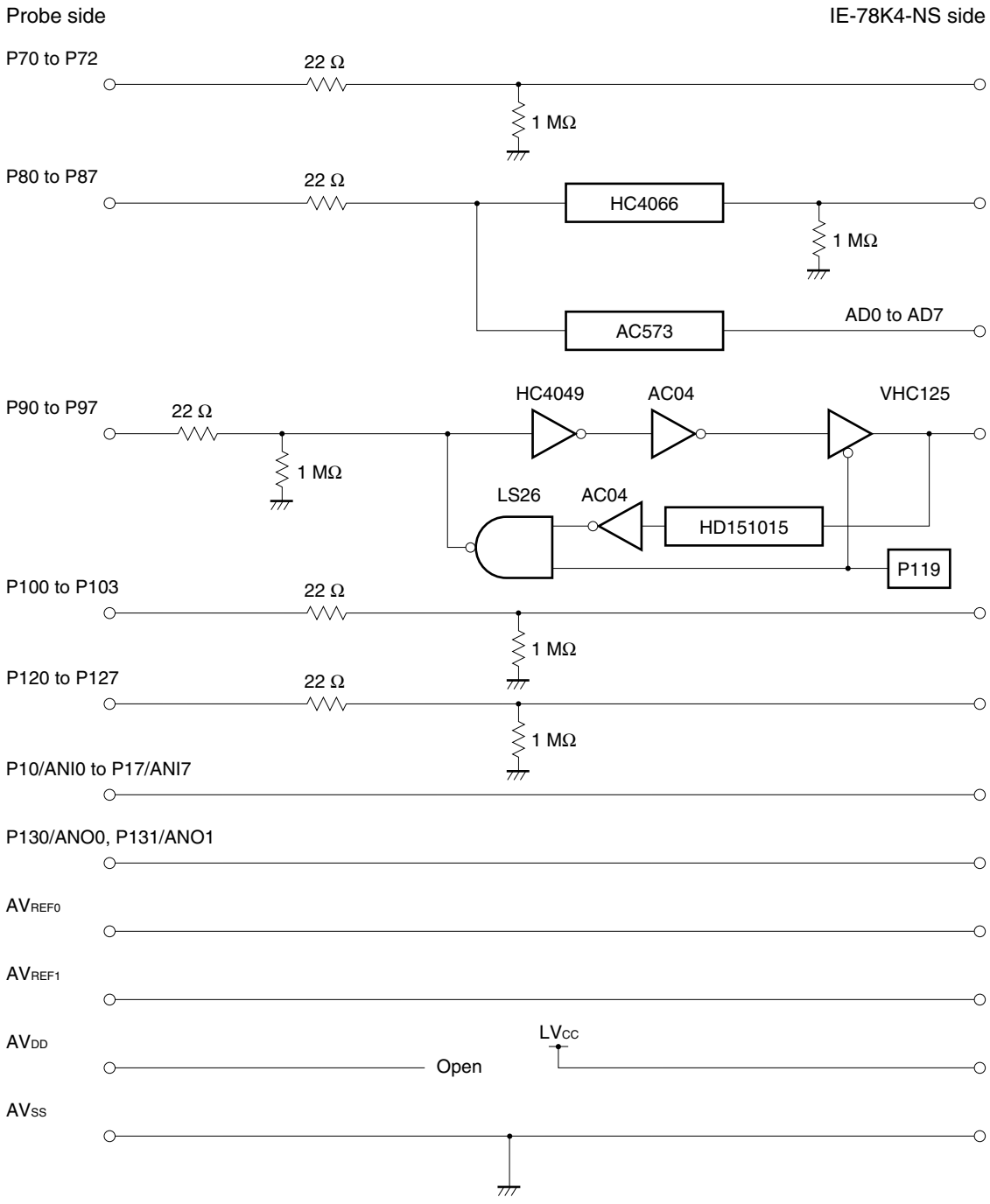
Note The AV_{DD} pin on the target system is not connected to the IE system. Either the power supply of the IE system or the power supply supplied to TP1 is supplied to the AV_{DD} pin of the emulation CPU. Port 10 and AV_{REF0} are not used when the target system is the μPD784225 Subseries.

Figure 4-1. Equivalent Circuit 1 of Emulation Circuit



Remark When the target device is the μPD784225 Subseries, the signal of the P06 pin is not used in the IE system.

Figure 4-2. Equivalent Circuit 2 of Emulation Circuit



Remark When the target device is the μPD784225 Subseries, the following signals are not used in the IE system, and LV_{CC} is supplied to AV_{REF0}.

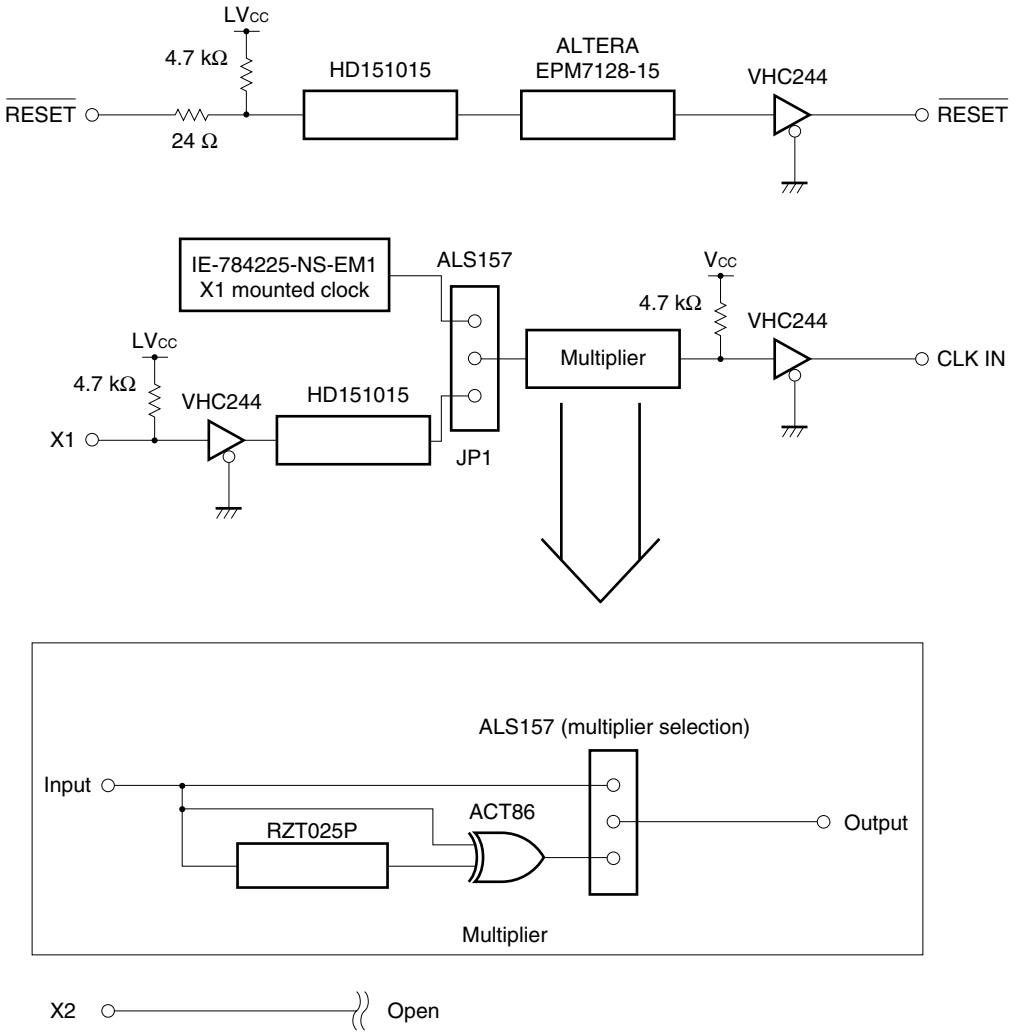
P80 to P87, P90 to P97, and P100 to P103

(2) Signals input from the target system via a gate

Since the following signals are input via a gate, their timing shows a delay compared to that of the μPD784225 Subseries. Their AC characteristics and DC characteristics are therefore different from μPD784225 Subseries, making it necessary to observe a stricter timing design than in the case of μPD784216A, 784216AY, 784218A, 784218AY, and 784225 Subseries.

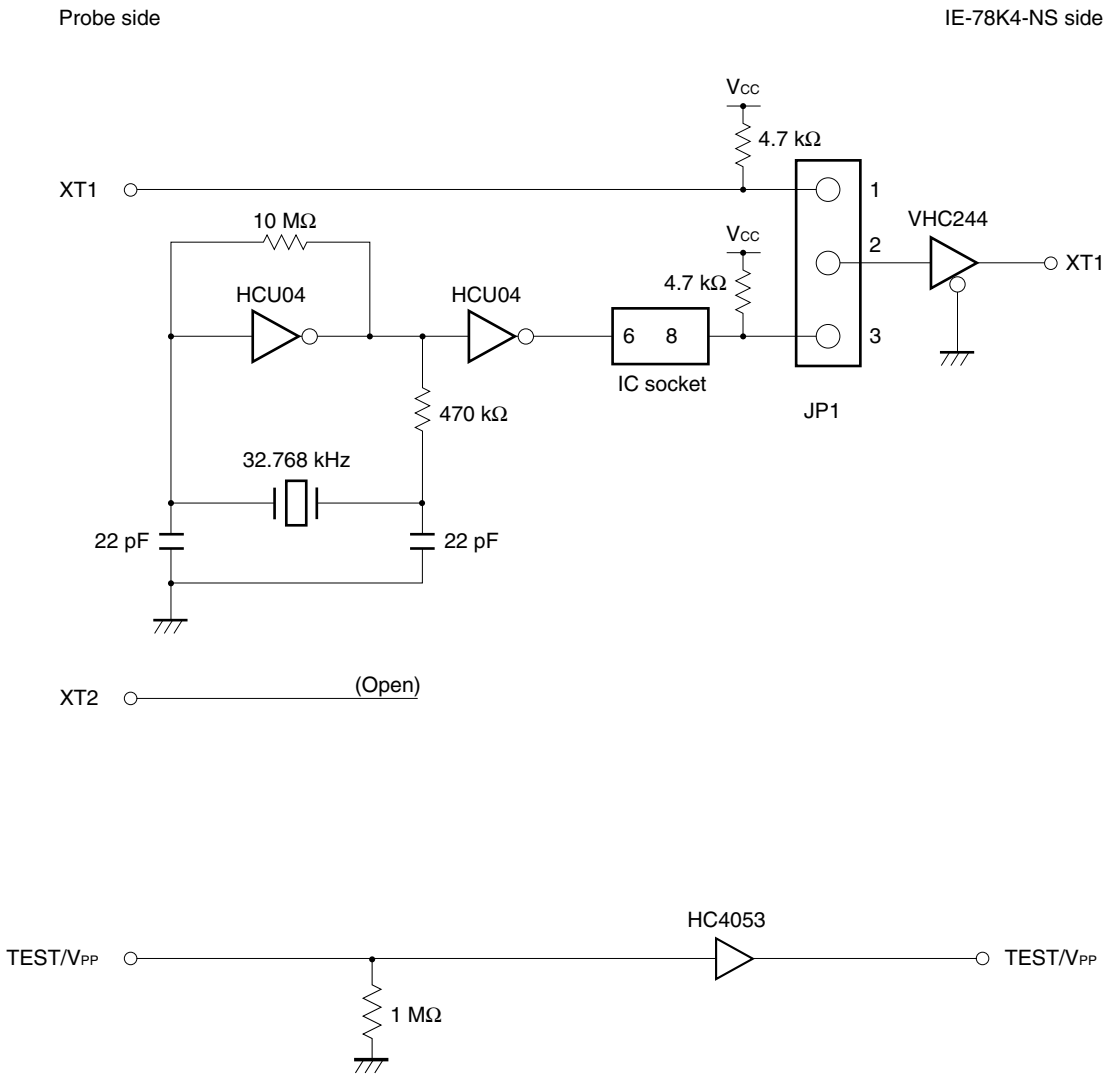
- $\overline{\text{RESET}}$ signal
- Signals related to clock input

Figure 4-3. Equivalent Circuit 3 of Emulation Circuit



Remark The multiplier can be selected by switch 4 of the DIP switch (SW3).
When the multiplier is not selected, the IE system is supplied with the input frequency unchanged.
When the multiplier is selected, the IE system is supplied with a frequency 2 times that input.
Be sure to observe the caution concerning emulation of the slew-rate clock in **3.4.4**.

Figure 4-4. Equivalent Circuit 4 of Emulation Circuit



The internal IE system voltage is selected for the TEST/V_{PP} input to the IE system during reset. The voltage from the target is selected after reset is released.

(3) Other signals

- V_{DD} pin

  When the emulation CPU is operating at 5 V, its power is supplied from the internal IE system, but when operating at low voltage, its power is supplied from the low-voltage pin (TP1). The V_{DD} pin of the target system is only used to control the LED (USERV_{DD}) in the IE system that monitors the input of the target system's power supply.
- V_{SS} pin

  The V_{SS} pin is connected to GND inside the IE system.

APPENDIX A EMULATION PROBE PIN ASSIGNMENT TABLE

Table A-1. NP-80GC/GK Pin Assignments (1/2)

Emulation Probe	CN2 Pin No.	Emulation Probe	CN2 Pin No.
1	114	34	49
2	113	35	50
3	108	36	45
4	107	37	46
5	104	38	41
6	103	39	42
7	100	40	35
8	99	41	8
9	94	42	7
10	93	43	14
11	30	44	13
12	29	45	18
13	24	46	17
14	23	47	22
15	20	48	21
16	19	49	28
17	16	50	27
18	15	51	92
19	10	52	91
20	9	53	98
21	37	54	97
22	43	55	102
23	44	56	101
24	47	57	106
25	48	58	105
26	51	59	112
27	52	60	111
28	57	61	83
29	58	62	77
30	59	63	78
31	60	64	73
32	55	65	74
33	56	66	69

Remarks 1. The NP-80GC/GK are products of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

Table A-1. NP-80GC/GK Pin Assignments (2/2)

Emulation Probe	CN2 Pin No.	Emulation Probe	CN2 Pin No.
67	70	74	71
68	63	75	72
69	64	76	75
70	61	77	76
71	62	78	79
72	65	79	80
73	66	80	85

Remarks 1. The NP-80GC/GK are products of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

Table A-2. NP-100GC Pin Assignments (1/2)

Emulation Probe	CN1 Pin No.	Emulation Probe	CN1 Pin No.
1	118	34	52
2	117	35	57
3	114	36	58
4	113	37	59
5	108	38	60
6	107	39	55
7	104	40	56
8	103	41	49
9	100	42	50
10	99	43	45
11	94	44	46
12	93	45	41
13	30	46	42
14	29	47	35
15	24	48	36
16	23	49	31
17	20	50	32
18	19	51	4
19	16	52	3
20	15	53	8
21	10	54	7
22	9	55	14
23	6	56	3
24	5	57	18
25	33	58	17
26	34	59	22
27	37	60	21
28	38	61	28
29	43	62	27
30	44	63	92
31	47	64	91
32	48	65	98
33	51	66	97

Remarks 1. The NP-100GC is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

Table A-2. NP-100GC Pin Assignments (2/2)

Emulation Probe	CN1 Pin No.	Emulation Probe	CN1 Pin No.
67	102	84	70
68	101	85	63
69	106	86	64
70	105	87	61
71	112	88	62
72	111	89	65
73	116	90	66
74	115	91	71
75	87	92	72
76	88	93	75
77	83	94	76
78	84	95	79
79	77	96	80
80	78	97	85
81	73	98	86
82	74	99	89
83	69	100	90

Remarks 1. The NP-100GC is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

Table A-3. NP-100GF Pin Assignments (1/2)

Emulation Probe	CN1 Pin No.	Emulation Probe	CN1 Pin No.
1	116	34	107
2	115	35	104
3	87	36	103
4	88	37	100
5	83	38	99
6	84	39	94
7	77	40	93
8	78	41	30
9	73	42	29
10	74	43	24
11	69	44	23
12	70	45	20
13	63	46	19
14	64	47	16
15	61	48	15
16	62	49	10
17	65	50	9
18	66	51	6
19	71	52	5
20	72	53	33
21	75	54	34
22	76	55	37
23	79	56	38
24	80	57	43
25	85	58	44
26	86	59	47
27	89	60	48
28	90	61	51
29	118	62	52
30	117	63	57
31	114	64	58
32	113	65	59
33	108	66	60

Remarks 1. The NP-100GF is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

Table A-3. NP-100GF Pin Assignments (2/2)

Emulation Probe	CN1 Pin No.	Emulation Probe	CN1 Pin No.
67	55	84	13
68	56	85	18
69	49	86	17
70	50	87	22
71	45	88	21
72	46	89	28
73	41	90	27
74	42	91	92
75	35	92	91
76	36	93	98
77	31	94	97
78	32	95	102
79	4	96	101
80	3	97	106
81	8	98	105
82	7	99	112
83	14	100	111

Remarks 1. The NP-100GF is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The numbers in the “Emulation probe” column indicate the corresponding pin number on the emulation probe tip.

★ APPENDIX B PROGRAM WAIT CONTROL REGISTER SETTINGS IN IN-CIRCUIT EMULATOR

When performing programmable debugging using the in-circuit emulator, wait control must be performed by setting PWC1 and programmable wait control register 2 (PWC2).

If an external wait is set for the internal ROM area, the CPU becomes deadlocked.

The deadlock status is cleared only by reset input.

The settings of PWC2 and PWC1, other than bits 1 and 0, are invalid in the actual device, but have no adverse effect.

(1) Program wait control register 1 (PWC1) of in-circuit emulator

Address: 0FFC7H After reset: AAH R/W

Symbol	7	6	5	4	3	2	1	0
PWC1	PW31	PW30	PW21	PW20	PW11	PW10	PW01	PW00

(n = 0 to 3)

Wait Target Address		00C000H to 00FFFFH	008000H to 00BFFFH	004000H to 007FFFH	000000H to 003FFFH
PWn1	PWn0				
0	0	No address wait insertion			
0	1	1-wait access wait insertion			
1	0	2-wait access wait insertion			
1	1	Access wait insertion for low-level time input to $\overline{\text{WAIT}}$ pin			

(2) Program wait control register 2 (PWC2) of in-circuit emulator

Address: 0FFC8H After reset: AAAAH W

Symbol	15	14	13	12	11	10	9	8
PWC2	1	0	1	0	1	0	1	0

7	6	5	4	3	2	1	0
PW71	PW70	PW61	PW60	PW51	PW50	PW41	PW40

(n = 4 to 7)

Wait Target Address		080000H to 0FFFFFH	040000H to 07FFFFH	020000H to 03FFFFH	010000H to 01FFFFH
PWn1	PWn0				
0	0	No address wait insertion			
0	1	1-wait access wait insertion			
1	0	2-wait access wait insertion			
1	1	Access wait insertion for low-level time input to $\overline{\text{WAIT}}$ pin			

Remark Wait cycle insertion is controlled by the entire address space (except peripheral RAM area).

★

APPENDIX C REVISION HISTORY

The history of revisions up to this edition is shown below. The “Applied to:” column indicates the chapters in each edition to which the revision was applied.

Edition	Major Revisions from Previous Edition	Applied to:
2nd edition	Change of debugger supply medium to CD-ROM, addition of (-A) to IE-70000-PCI-IF, addition of website address for downloading device files, and modification of telephone number of Naito Densei Machida Mfg. Co., Ltd.	**CHAPTER 1 GENERAL**
	Modification of target devices in basic specifications	
	Addition of description for selection of emulator main unit	**CHAPTER 3 INSTALLATION**
	Deletion of description that parts board is supplied	
	Modification of chapter title and description	**APPENDIX B PROGRAM WAIT CONTROL REGISTER SETTINGS IN IN-CIRCUIT EMULATOR**

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