AK4317

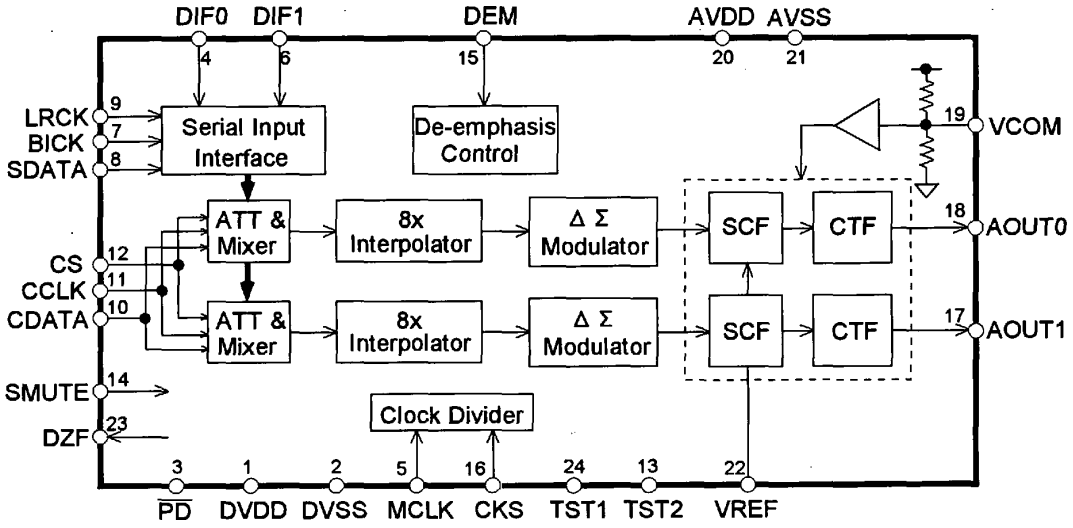
18Bit SCF DAC with ATT & MIXER

General Description

The AK4317 is a 1bit stereo DAC with channel separated volume and channel mixer. This DAC also includes 18bit digital filter and analog LPF. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4317, the loss of accuracy from clock jitter is also improved by using SCF techniques for on-chip post filter. Therefore, the AK4317 is suitable for the system like STB including PLL circuit.

Features

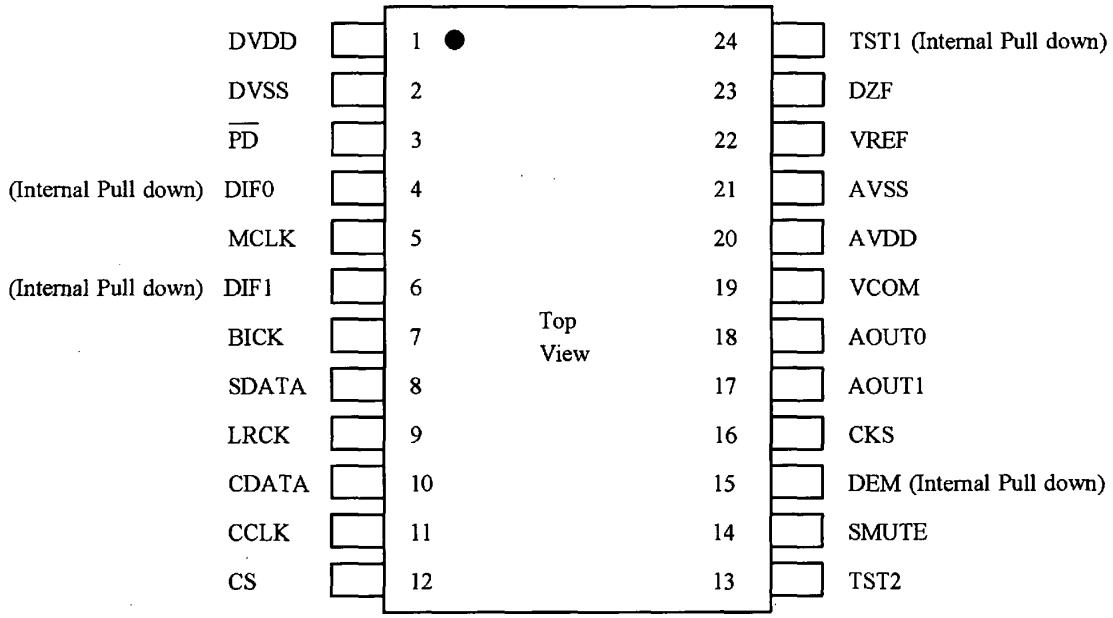
- ☐ Sampling Rate Ranging from 8kHz to 50kHz
- ☐ On chip Perfect filtering
  - • 8 times FIR Interpolator
  - • 2nd order SCF
  - • 2nd order CTF
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ L/R Separated Volume
- ☐ L/R Mixing
- ☐ Soft Mute
- ☐ Audio I/F format : MSB justified, LSB justified, I2S
- ☐ Master Clock: 256fs or 384fs
- ☐ High Tolerance to Clock Jitter
- ☐ THD+N: -86dB
- ☐ DR: 92dB
- ☐ Power Supply:4.5 to 5.5V
- ☐ Small Package: 24pin VSOP
- ☐ AK4311 Compatible



■ Ordering Guide

AK4317-VF	-40~+85°C	24pin VSOP(0.65mm pitch)
AKD4317	Evaluation Board	

■ Pin Layout



■ Compatibility with AK4311/A

1. Changed Specs

Parameter	AK4311	AK4311A	AK4317
Resolution	16bit	16bit	16/18bit
Operating Temperature	-40~85°C	-10~70°C	-40~85°C
Power Supply	3~5.5V	3~5.5V	4.5~5.5V
Digital I/F level	CMOS	CMOS	TTL
X'tal Oscillator	Yes	Yes	No
DR	92dB	91dB	92dB
Package	SSOP	SSOP	VSOP

2. Pin Compatibility

The following pin functions are changed from AK4311/A. But when X'tal oscillating circuit is not used, it is possible to change AK4311/A to AK4317 without changing the board layout.

Pin No.	AK4311/A	AK4317
4	XTO	DIF0
6	CLKO	DIF1

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply
2	DVSS	-	Digital Ground Pin
3	$\overline{PD}$	I	Power-Down Mode Pin When at "L", the AK4317 is in power-down mode and is held in reset. The AK4317 should always be reset upon power-up.
4	DIF0	I	Digital Input Format Pin (Internal Pull-down pin)
5	MCLK	I	Master Clock Input Pin
6	DIF1	I	Digital Input Format Pin (Internal Pull-down pin)
7	BICK	I	Audio Serial Data Clock Pin
8	SDATA	I	Audio Serial Data Input Pin 2's complement MSB-first data is input on this pin.
9	LRCK	I	L/R Clock Pin
10	CDATA	I	Control Data Input Pin Must be tied to "H" or "L" if this pin is not used.
11	CCLK	I	Control Clock Pin Must be tied to "H" or "L" if this pin is not used.
12	CS	I	Chip Select Pin Must be tied to "H" if this pin is not used.
13	TST2	O	Test Pin Must be left floating.
14	SMUTE	I	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
15	DEM	I	De-emphasis Enable Pin (Internal Pull-down pin)
16	CKS	I	Master Clock Select Pin MCLK=256fs,"H": MCLK=384fs
17	AOUT1	O	Channel 1 analog output pin
18	AOUT0	O	Channel 0 analog output pin
19	VCOM	I	Common Voltage Pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
20	AVDD	-	Analog Power Supply Pin
21	AVSS	-	Analog Ground pin
22	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and AVSS set the analog output range. Normally connected to AVSS with a 0.1uF ceramic capacitor.
23	DZF	O	Zero Input Detect Pin
24	TST1	I	Test Pin Must be left floating or tied to AVSS.

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog Digital DADD-AVDD	AVDD DVDD VDA	-0.3 -0.3 -	6.0 6.0 0.3	V V V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1 . All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog (Note 2) Digital	AVDD DVDD	4.5 4.5	5.0 5.0	5.5 AVDD	V V
Voltage Reference (Note 3)		VREF	2.5	-	AVDD	V

Notes: 2. AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
3. Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=2.8Vpp*VREF/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=5.0V; VREF=AVDD; fs=44.1kHz; Signal Frequency=1kHz; 18bit Input Data; Measurement Bandwidth=10Hz~20kHz; $R_L \geq 10k\Omega$; unless otherwise specified)

Parameter	min	typ	max	Units
Resolution		18		Bits
Dynamic Characteristics (Note 4)				
THD+N (0dB Output)	-80	-86		dB
Dynamic Range (-60dB Output, A weight)	88	92		dB
S/N (A weight)	88	92		dB
Interchannel Isolation(1kHz)	80	90		dB
DC Accuracy				
Interchannel Gain Mismatch		0.15	0.3	dB
Gain Drift (Note 5)		20	-	ppm/°C
DC Accuracy				
Output Voltage (Note 6)	2.66	2.8	2.94	Vpp
Load Resistance	10			kΩ
Power Supplies				
Power Supply Current				
Normal Operation ($\overline{PD}$="H")				
AVDD		12	18	mA
DVDD		4	6	mA
Power-Down-Mode ($\overline{PD}$="L")				
AVDD+DVDD (Note 7)		10	50	uA
Power Dissipation (AVDD+DVDD)				
Normal Operation		80	120	mW
Power-Down-Mode (Note 7)		50		uW
Power Supply Rejection (Note 8)		50		dB

Notes: 4. Measured by AD725C(SHIBASOKU). Averaging mode. Refer to the eva board manual.
5. The voltage on VREF pin is held +5V externally.
6. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF pin.
AOUT(typ.@0dB)=2.8Vpp*VREF/5.
7. Power Dissipation in the power-down mode is applied with no external clocks (MCLK,BICK,LRCK held "H" or "L").
8. PSR is applied to AVDD,DVDD with 1kHz, 100mVpp. VREF pin is held +5V.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5V~5.5V; fs=44.1kHz; DEM="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.1dB (Note 9) -6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 9)	SB	24.1			kHz
Passband Ripple	PR			±0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 10)	GD	-	14.7	-	1/fs
Digital Filter + SCF + CTF					
Frequency Response 0~20.0kHz		-	±0.5	-	dB

Note: 9. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.1dB), SB=0.546*fs.

10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/18bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage Low-Level Input Voltage	VIH VIL	2.2 -	- -	- 0.8	V V
High-Level Output Voltage (Iout=-100A) Low-Level Output Voltage (Iout=100A)	VOH VOL	DVDD-0.5 -	-	- 0.5	V V
Input Leakage Current (Note 11)	Iin	-	-	±10	uA

Notes: 11. DIF0,DIF1,DEM,TST1 pins have internal pull-down devices, nominally 160kΩ.

SWITCHING CHARACTERISTICS

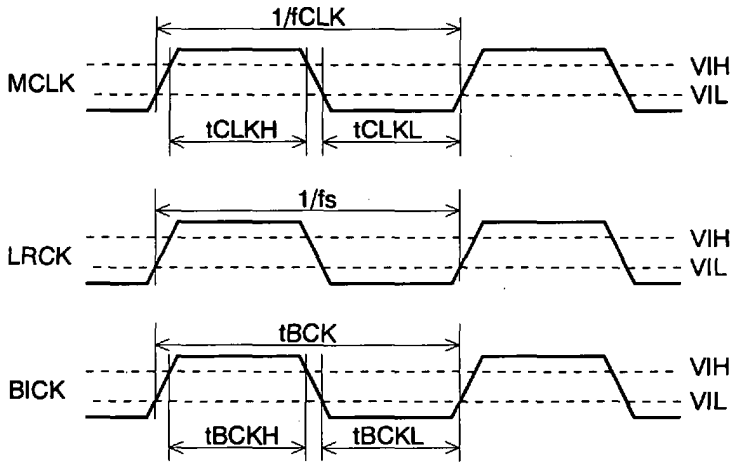
(Ta=25°C; AVDD,DVDD=4.5~5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
Master Clock Timing	256fs:	fCLK	2.048		12.8	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	3.072		19.2	MHz
	Pulse Width Low	tCLKL	23			ns
	Pulse Width High	tCLKH	23			ns
LRCK						kHz
Frequency		fs	8	44.1	50	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing						
BICK Period		tBCK	312.5			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
BICK rising to LRCK edge	(Note 12)	tBLR	50			ns
LRCK Edge to BICK rising	(Note 12)	tLRB	50			ns
SDATA Hold Time		tSDH	50			ns
SDATA Setup Time		tSDS	50			ns
Control Interface Timing						
CCLK Pulse Width Low		tCCKL	100			ns
Pulse Width High		tCCKH	100			ns
CDATA Latch Hold Time		tCDS	50			ns
CDATA Latch Setup Time		tCDH	50			ns
CS Pulse Width Low		tCSW	100			ns
CCLK to CS falling		tCSS	50			ns
CS rising to CCLK		tCSH	50			ns
Reset Timing						
$\overline{PD}$ Pulse Width	(Note 13)	tPD	150			ns

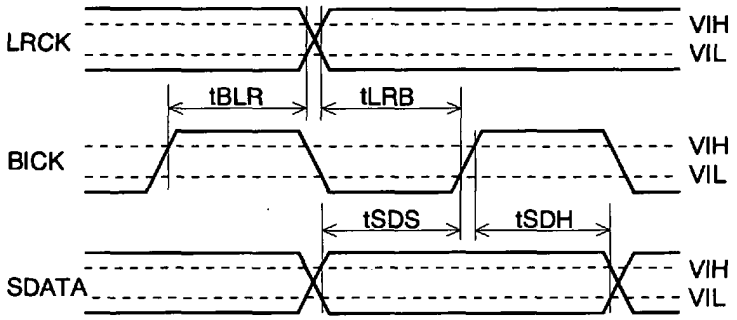
Notes: 12. BICK rising edge must not occur at the same time as LRCK edge.

13. The AK4317 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

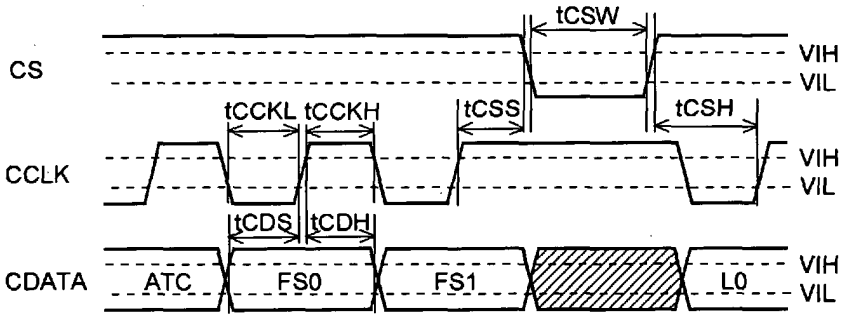
■ **Timing Diagram**



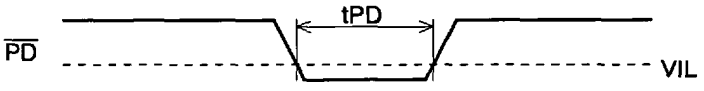
Clock Timing



Audio Interface Timing



Control Interface Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4317 are MCLK, LRCK, BICK. The master clock(MCLK)should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of MCLK is determined by the sampling rate (LRCK) and CKS pin. Table 1 illustrates corresponding clock frequencies. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Refer to Figure 1 .

All external clocks(MCLK,BICK,LRCK) should always be present whenever the AK4317 is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4317 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4317 should be in the power-down mode($\overline{PD}$="L"). After exiting reset at power-up etc., the AK4317 is in power-down mode until MCLK and LRCK are input.

Clock		frequency
LRCK (fs)		8k~50kHz
BICK		~64fs
MCLK	CKS="L"	256fs
	CKS="H"	384fs

Table 1 . System Clocks

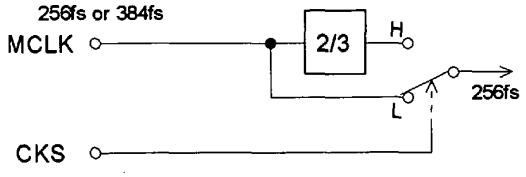


Figure 1 . MCLK divider

■Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Four serial data modes which are compatible with AK4319 are supported and selected by the DIF0 and DIF1 pins as shown in Table 2 . In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16 MSB justified formats by zeroing the unused LSBs.

DIF1	DIF0	Mode	BICK	Figure
0	0	0: 16bit LSB Justified	≥32fs	Figure 2
0	1	1: 18bit LSB Justified	≥36fs	Figure 2
1	0	2: 18bit MSB Justified	≥36fs	Figure 3
1	1	3: I^2S Compatible	≥36fs or 32fs	Figure 4

Table 2 . Serial Data Modes

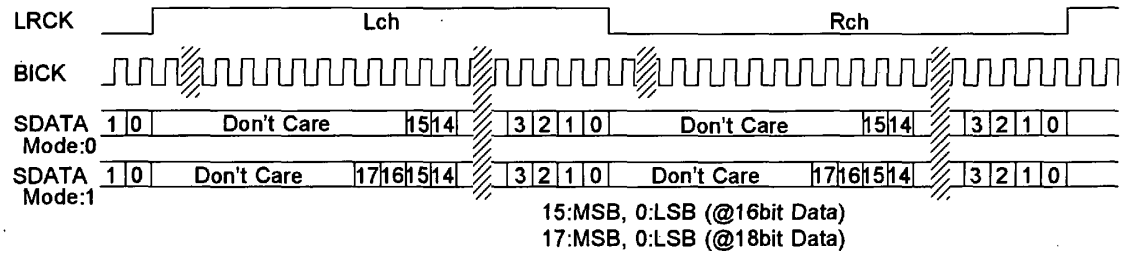


Figure 2 . Mode 0,1 Timing

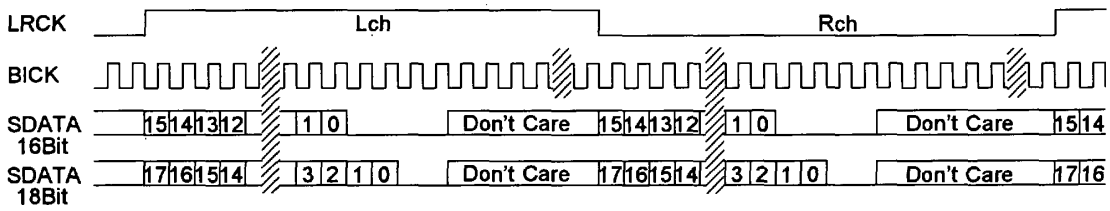


Figure 3 . Mode 2 Timing

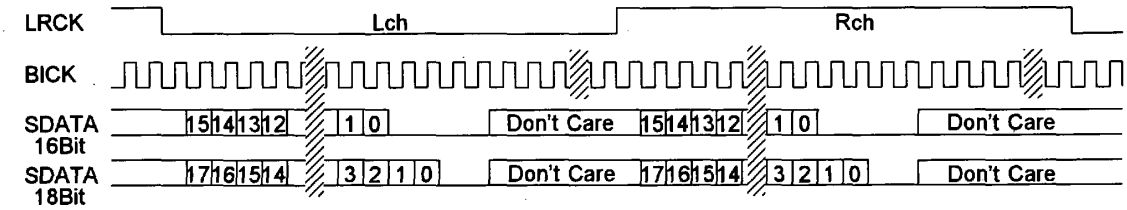


Figure 4 . Mode 3 Timing

■ De-emphasis filter

The AK4317 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz,44.1kHz,48kHz). De-emphasis is enabled by the following two ways.

1. DEM pin

Only one de-emphasis(fs=44.1kHz) set initially can be controlled by DEM pin at resetting. The de-emphasis is enabled by setting DEM pin "H". When the frequency of de-emphasis is set by FS0,FS1 of serial mode control bits, the corresponding de-emphasis can be enabled. In this case, DEM bit in the serial mode control should be "0".

2. DEM bit in the serial mode control

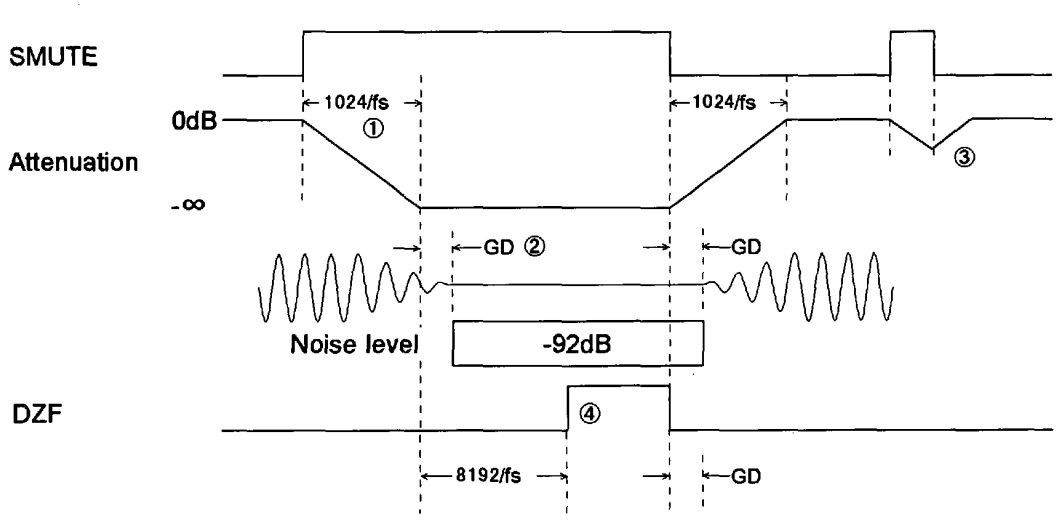
DEM pin should be open or "L". In this case, The de-emphasis corresponding to fs=32kHz, 44.1kHz,48kHz can be controlled by DEM, FS0 and FS1 in the serial mode control bits.

■ **Zero detection**

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

■ **Soft mute operation**

Soft mute operation is performed at digital domain. When SMUTE pin goes "H" or the output mode is set to "MUTE", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE pin is returned to "L" or exiting "MUTE", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission



Notes:

① The output signal is attenuated by -∞ during 1024 LRCK cycles(1024/fs).

② Analog output corresponding to digital input have the group delay(GD).

③ If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④ As the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H".
DZF immediately go to "L" if input data are not zero after DZF "H".

Figure 5 . Soft mute and zero detection

■ Serial Mode Control

The AK4317 can control output attenuation level, output mode, de-emphasis type and attenuation mode via the serial interface. The serial data consists of two 8 bits for setting the attenuation level of each channel and 8 bits for the mode control.

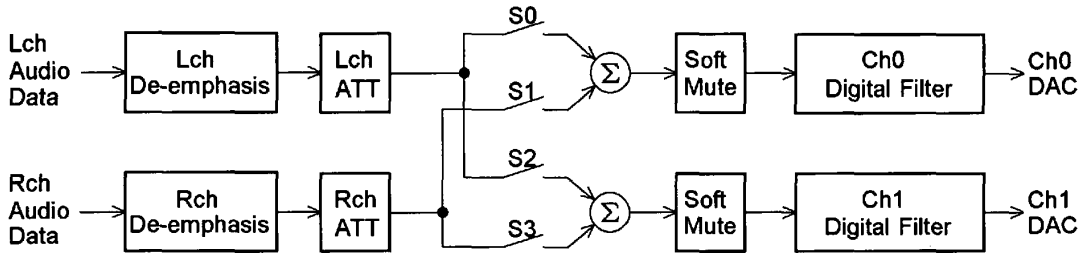
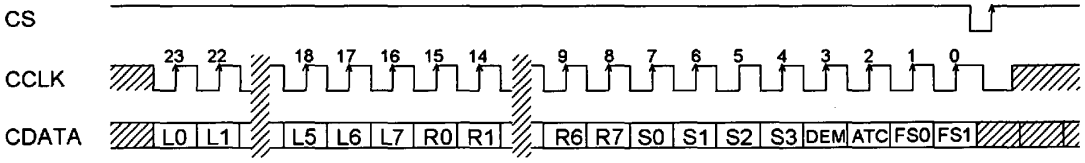


Figure 6 . Configuration of attenuator and mixer



L0-L7:	Lch ATT data, L0=LSB, L7=MSB	:FFH at RESET
R0-R7:	Rch ATT data, R0=LSB, R7=MSB	:FFH at RESET
S0-S3:	Output mode Control	:1001 at RESET
DEM:	De-Emphasis Control	:0 at RESET
ATC:	ATT mode Control	:0 at RESET
FS0,FS1:	fs Control for de-emphasis Filter	:00 at RESET

Note 1: CCLK should be held "H" or "L" except writing to ATT & mode registers in order to avoid the performance degradation.

Note 2: If the above serial mode control is not used, CS should be held "H".

Figure 7 . Serial mode control timing

1. Attenuator Operation

The AK4317 has individually controllable attenuator with linear scale and 256 levels for each channel.

Equation of attenuation level: $ATT=20\times Log_{10}(\text{Binary level}/255)$

FFH: 0dB
:
01H: -48.1dB
00H: Mute(Infinity zero:-∞)

The transition between ATT values is same as soft mute operation. When current value is ATT1 and new value is set as ATT2, ATT1 gradually becomes ATT2 with same operation as soft mute. If new value is set as ATT3 before reaching ATT2, ATT value gradually becomes ATT3 from the way of transition.

Cycle time of soft mute: Ts=1024/fs

When resetting, ATT value is set 00H(Infinity zero). ATT value gradually changes from 00H to FFH(0dB) during Ts after exiting reset.

2. Output mode

The AK4317 supports the following output modes.
- Normal stereo output
- L/R Reverse output
- Monaural output: L/L, R/R, (L+R)/2
- Output muting with soft mute operation

When resetting, ATT values of both channels are FFH and the attenuation levels are set 0dB. The output mode is also set normal stereo output.

S0	S1	S2	S3	AOUT0	AOUT1	Mode	
0	0	0	0	MUTE	MUTE	MUTE	
0	0	0	1	MUTE	R		
0	0	1	0	MUTE	L		
0	0	1	1	MUTE	(L+R)/2		
0	1	0	0	R	MUTE		
0	1	0	1	R	R		
0	1	1	0	R	L	Reverse	
0	1	1	1	R	(L+R)/2		
1	0	0	0	L	MUTE		
1	0	0	1	L	R	Stereo	* at RESET
1	0	1	0	L	L		
1	0	1	1	L	(L+R)/2		
1	1	0	0	(L+R)/2	MUTE		
1	1	0	1	(L+R)/2	R		
1	1	1	0	(L+R)/2	L		
1	1	1	1	(L+R)/2	(L+R)/2	MONO	

Table 3 . Output mode

3. De-emphasis control

DEM bit and DEM pin are ORed internally. The de-emphasis(tc=50/15us) corresponding to fs(sampling frequency)selected by FS0 and FS1 is enabled by setting DEM bit "1" or DEM pin "H". When DEM bit is "0" and DEM pin is "L", the de-emphasis is disabled and the setting of FS0 and FS1 is invalid. The de-emphasis is also disabled at FS0="1" and FS1="0". When resetting, DEM bit is set "0". For example, when the de-emphasis is controlled by only DEM pin at fs=44.1kHz, DEM,FS0,FS1 bits should be "0". This condition is also set at resetting.

FS0	FS1	mode
0	0	44.1kHz
1	0	OFF
0	1	48kHz
1	1	32kHz

Table 4 .De-emphasis filter setting
(Valid at DEM bit="1" or DEM pin="H")

4. Attenuation control

ATT values of both channels are set Lch ATT data by setting ATC bit "1". In this case, Rch ATT data is ignored. When resetting, ATC bit is set "0" (individually control).

■ Power-Down

The AK4317 are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 8 shows an example of the system timing at the power-down and power-up.

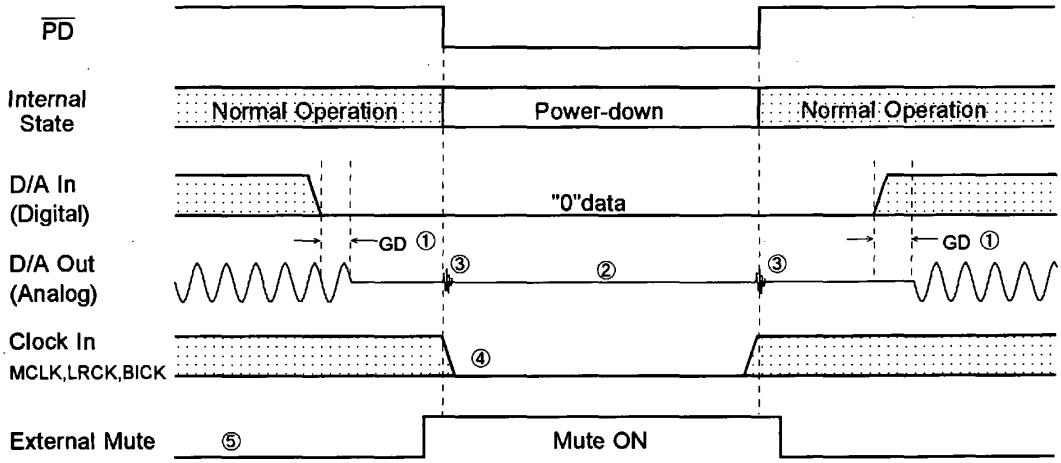


Figure 8 . Power-down/up sequence example

Notes:

① Analog output corresponding to digital input have the group delay(GD).
② Analog outputs are floating(Hi-Z) at the power-down mode.
③ Click noise about -50dB occurs at the edges("↑↓") of $\overline{PD}$ signal.
This noise is output even if "0" data is input.
④ When the external clocks(MCLK,BICK,LRCK) are stopped, the AK4317 should be in the power-down mode.
⑤ Please mute the analog output externally if the click noise(③) influences system application.
The timing example is shown in this figure.

■ System Reset

The AK4317 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The AK4317 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4317 is in power-down mode until LRCK is input.

■ Click Noise from analog output

Click noise occurs from analog output in the following cases.

① When switching de-empahsis mode by DEM bit or DEM pin.
② When switching serial data mode by DIF0,DIF1 pins,
③ When going and exiting power down mode by $\overline{PD}$ pin,

However in case of ① & ②, If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE="H"), no click noise occur.

SYSTEM DESIGN

Figure 9 shows the system connection diagram. An evaluation board[AKD4317] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

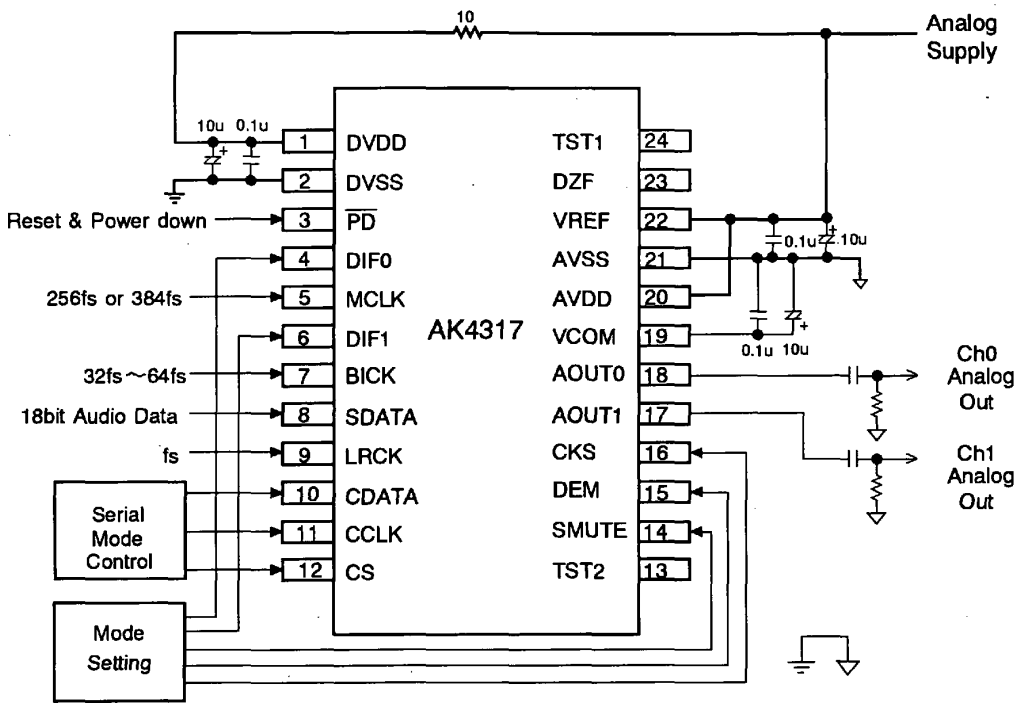


Figure 9 . Typical Connection Diagram

Notes:

- LRCK=fs, MCLK=256fs at CKS="L", MCLK=384fs at CKS="H".
- If the above serial mode control is not used, CS should be held "H".
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- The capacitor value on VCOM depends on low frequency noise level of power supply.
- All input pins except pull-down pins(DIF0,DIF1,DEM,TST1) should not be left floating.

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor as shown inFigure 9 . Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor of around 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4317.

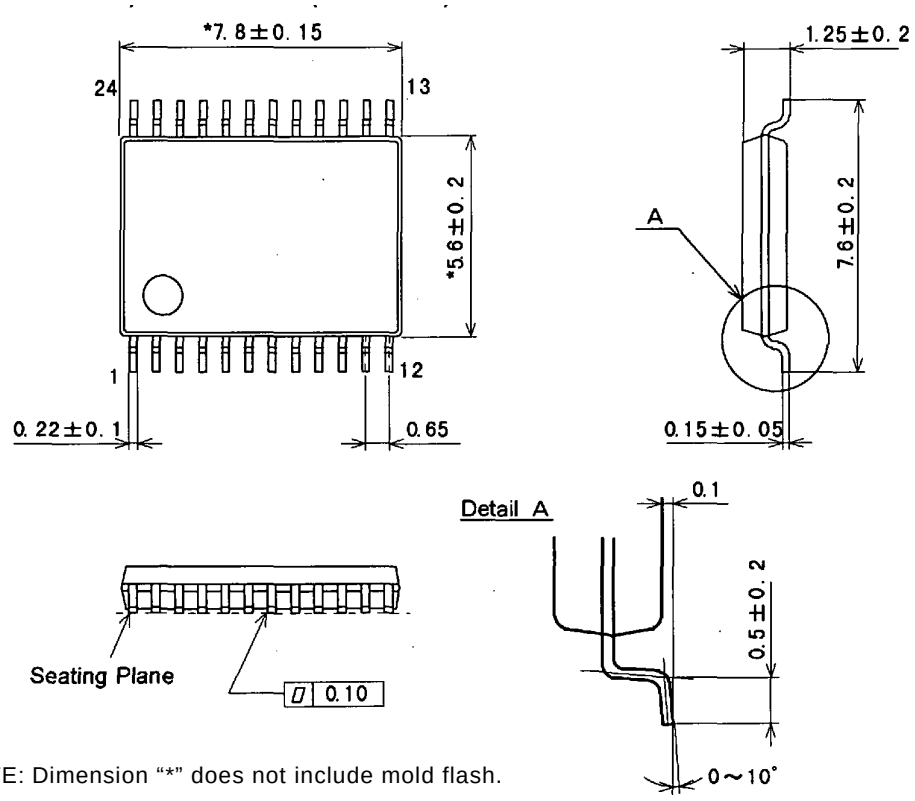
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.8Vpp. AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 1FFFFH(@18bit) and a negative full scale for 20000H(@18bit). The ideal output is VCOM voltage for 00000H(@18bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

● **24pin VSOP (Unit: mm)**

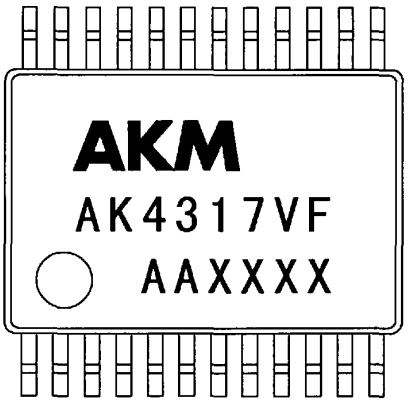


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXX

AA: Lot#

XXXX: Date Code

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