T-75-37-05

GigaBit Logic

16G050
ADVANCE

HIPPI/Fiber Channel Transmitter
1.0625 Gbit/s Data Rate

FEATURES

- 1.0625 GHz operation
- Compliant with the HIPPI/Fiber Channel standard
- 25 or 53.125 MHz Fref input
- On-chip Lock Detect circuitry (TTL levels)
- PLL provides immunity to component aging and temperature effects
- Low power (1.2W typ.)
- Single power supply (+5.0V)
- TTL compatible inputs and CLK/20 & $\overline{\text{CLK/20}}$ outputs
- PECL compatible DX and $\overline{\text{DX}}$ outputs
- Available in small 0.4" x 1.2" substrate or 0.5" x 1.25" flatpack package

APPLICATIONS

- HIPPI /Fiber Channel transmitter
- Fiber optic and microwave transmitters
- Computer-to-peripheral data communication
- Fiber Optic communications test equipment
- High Speed LAN
- High resolution graphic display terminal
- High data rate word or test vector generator
- Digital RF Memory

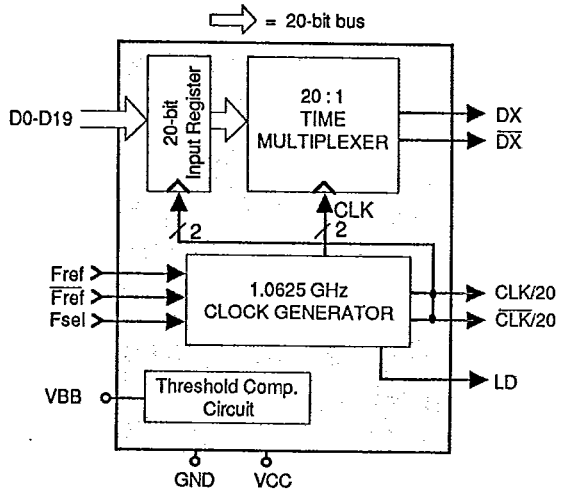
FUNCTIONAL DESCRIPTION

The 16G050 is a monolithic transmitter IC integrating a complete Phase Locked Loop Clock synthesizer and a 20:1 multiplexer. The 16G050 is designed for fiber optic transport of HIPPI encoded with IBM's 8B/10B code and is compliant with the HIPPI/Fiber Channel standard.

The 16G050 accepts 20 TTL encoded data lines (D0-D15) at 53.125 Mb/s, converts them to a single 1.0625 Gbauds high speed serial data stream and generates the 1.0625 GHz high speed clock required to drive the 20:1 MUX. The reference frequency for the clock generator is AC coupled and selectable between the 53.125 MHz coming from the TTL or CMOS protocol encoder IC and the 25 MHz of the 32 HIPPI data lines. In the latter case, the 16G050 generates differential $\overline{\text{CLK/20}}$ and CLK/20 signals (53.125 MHz) for driving the TTL or CMOS protocol encoder IC.

The 16G050 features a Lock Detect (LD) circuitry that outputs a TTL-level signal when the incoming reference frequency (Fref/$\overline{\text{Fref}}$) is not phase locked to the initial VCO frequency or when there is no incoming reference frequency. The 16G050 operates with one power supply (+5.0V). All inputs and outputs are TTL compatible and low frequency (53.125 MHz or less) except for the 1.0625 Gbauds differential data outputs (DX/$\overline{\text{DX}}$) that are shifted positive ECL compatible (PECL: VTH = +3.7V).

16G050 BLOCK DIAGRAM



T-90-20

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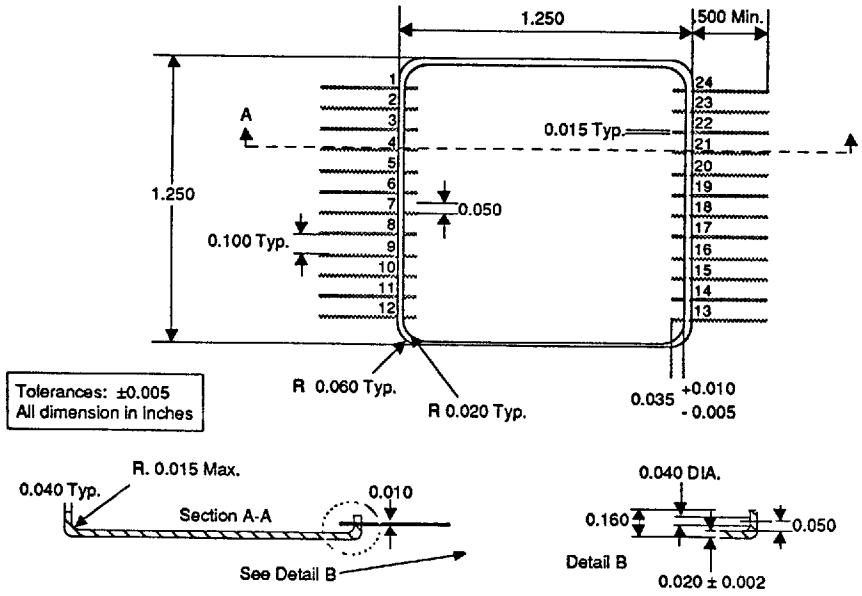
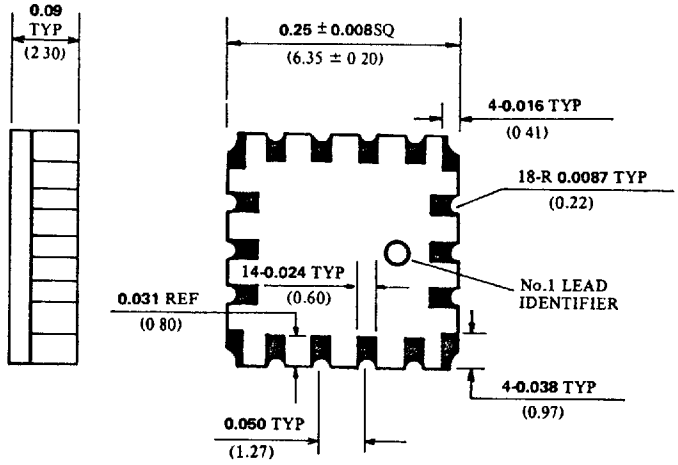
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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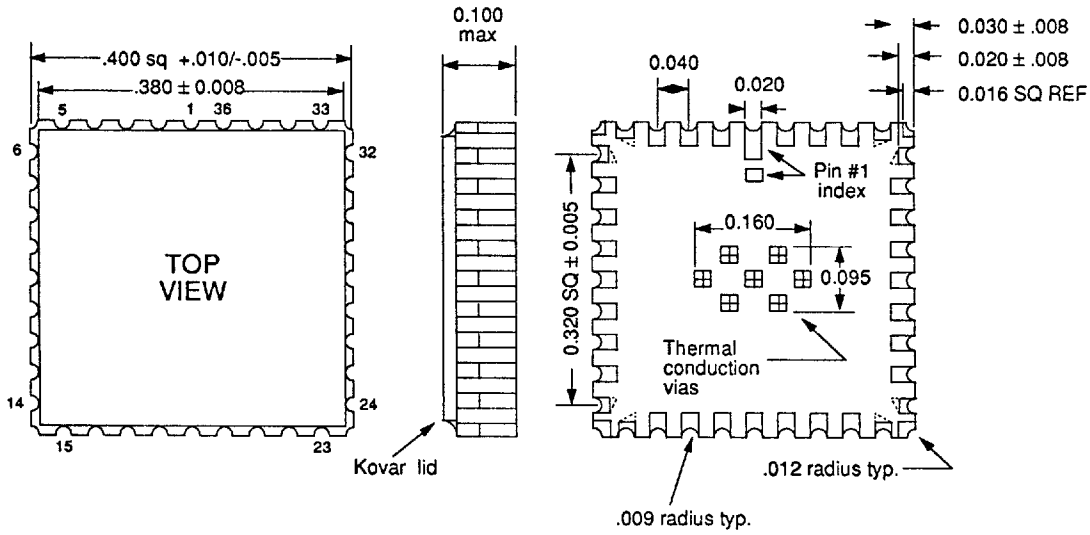
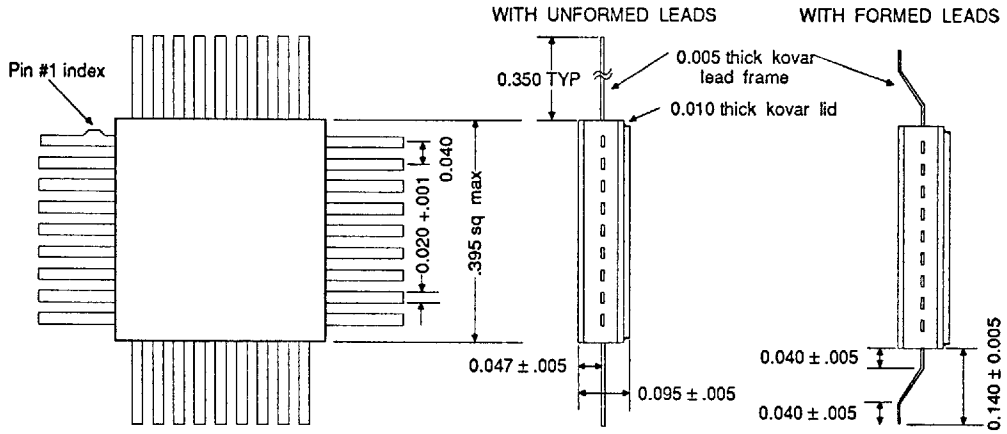
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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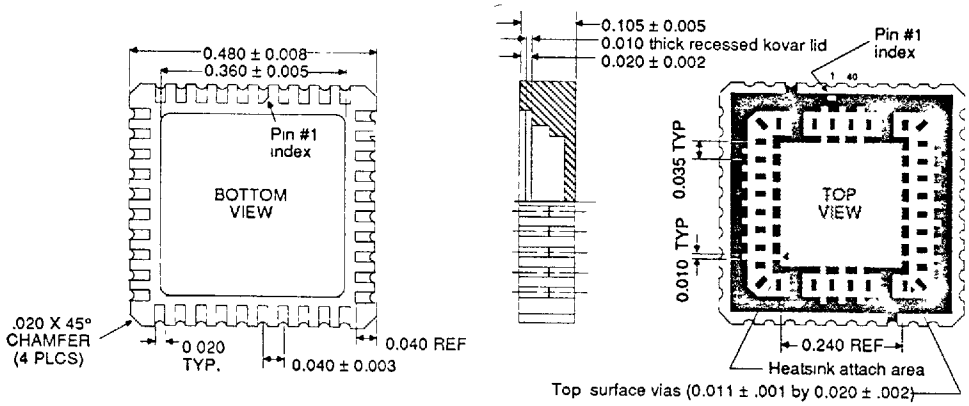
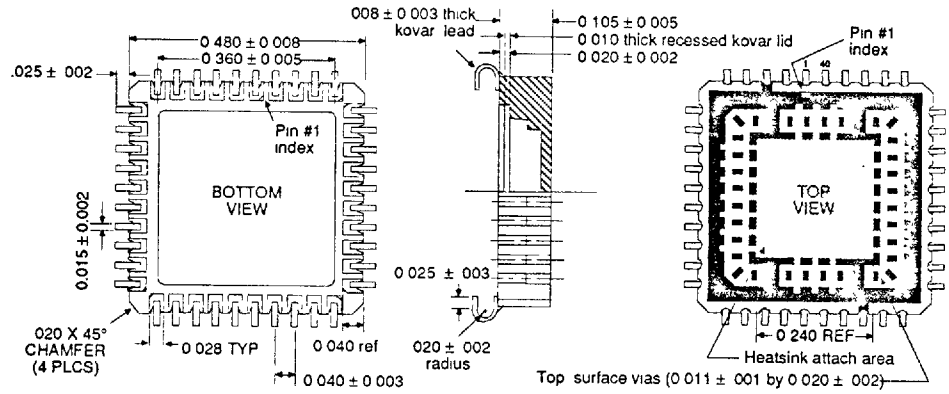
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

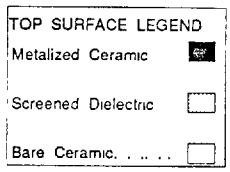


40 PIN LEADED CHIP CARRIER
TYPE C

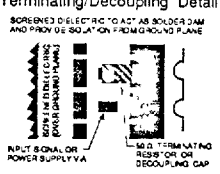


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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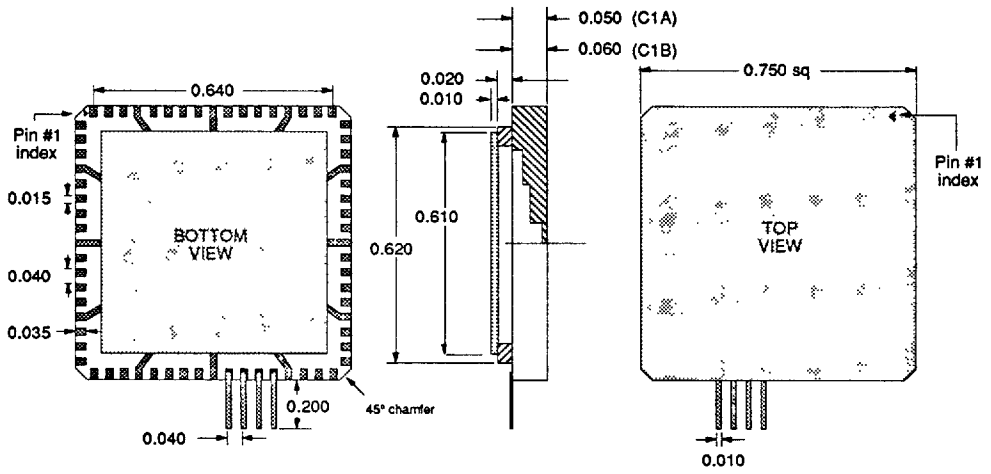
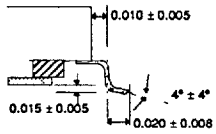
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3