NEC

MOS INTEGRATED CIRCUIT

μPD441000L-X

1M-BIT CMOS STATIC RAM
128K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD441000L-X is a high speed, low power, 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The μPD441000L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

★ The μPD441000L-X is packed in 32-pin plastic SOP and 32-pin plastic TSOP (I) (8×13.4 mm) and (8×20 mm).

Features

- 131,072 words by 8 bits organization
- Fast access time : 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation
  (B version : V_{CC} = 2.7 to 3.6 V, C version : V_{CC} = 2.2 to 3.6 V, D version : V_{CC} = 1.8 to 3.6 V)
- Low V_{CC} data retention
  (B version : 2.0 V (MIN.), C version, D version : 1.5 V (MIN.))
- Operating ambient temperature : T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs : /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD441000L-BxxX	70, 85, 100	2.7 to 3.6	–25 to +85	25	2	2 Note
μPD441000L-CxxX	100, 120	2.2 to 3.6				
μPD441000L-DxxX	120, 150	1.8 to 3.6				

Note 0.5 μA ($T_A \leq 40$ °C)

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The mark ★ shows major revised points.

★ Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD441000LGW-B70X	32-pin Plastic SOP	70	2.7 to 3.6	−25 to +85	B version
μPD441000LGW-B85X	(13.34 mm (525))	85			
μPD441000LGW-B10X		100			
μPD441000LGU-B70X-9JH	32-pin Plastic TSOP (I)	70			
μPD441000LGU-B85X-9JH	(8×13.4) (Normal bent)	85			
μPD441000LGU-B10X-9JH		100			
μPD441000LGU-B70X-9KH	32-pin Plastic TSOP (I)	70			
μPD441000LGU-B85X-9KH	(8×13.4) (Reverse bent)	85			
μPD441000LGU-B10X-9KH		100			
μPD441000LGZ-B70X-KJH	32-pin Plastic TSOP (I)	70			
μPD441000LGZ-B85X-KJH	(8×20) (Normal bent)	85			
μPD441000LGZ-B10X-KJH		100			
μPD441000LGZ-B70X-KKH	32-pin Plastic TSOP (I)	70			
μPD441000LGZ-B85X-KKH	(8×20) (Reverse bent)	85			
μPD441000LGZ-B10X-KKH		100			
μPD441000LGW-C10X	32-pin Plastic SOP	100	2.2 to 3.6		C version
μPD441000LGW-C12X	(13.34 mm (525))	120			
μPD441000LGU-C10X-9JH	32-pin Plastic TSOP (I)	100			
μPD441000LGU-C12X-9JH	(8×13.4) (Normal bent)	120			
μPD441000LGU-C10X-9KH	32-pin Plastic TSOP (I)	100			
μPD441000LGU-C12X-9KH	(8×13.4) (Reverse bent)	120			
μPD441000LGZ-C10X-KJH	32-pin Plastic TSOP (I)	100			
μPD441000LGZ-C12X-KJH	(8×20) (Normal bent)	120			
μPD441000LGZ-C10X-KKH	32-pin Plastic TSOP (I)	100			
μPD441000LGZ-C12X-KKH	(8×20) (Reverse bent)	120			
μPD441000LGW-D12X	32-pin Plastic SOP	120	1.8 to 3.6		D version
μPD441000LGW-D15X	(13.34 mm (525))	150			
μPD441000LGU-D12X-9JH	32-pin Plastic TSOP (I)	120			
μPD441000LGU-D15X-9JH	(8×13.4) (Normal bent)	150			
μPD441000LGU-D12X-9KH	32-pin Plastic TSOP (I)	120			
μPD441000LGU-D15X-9KH	(8×13.4) (Reverse bent)	150			
μPD441000LGZ-D12X-KJH	32-pin Plastic TSOP (I)	120			
μPD441000LGZ-D15X-KJH	(8×20) (Normal bent)	150			
μPD441000LGZ-D12X-KKH	32-pin Plastic TSOP (I)	120			
μPD441000LGZ-D15X-KKH	(8×20) (Reverse bent)	150			

Pin Configurations (Marking Side)

/xxx indicates active low signal.

32-pin Plastic SOP (13.34 mm (525))

[μPD441000LGW-BxxX]

[μPD441000LGW-CxxX]

[μPD441000LGW-DxxX]

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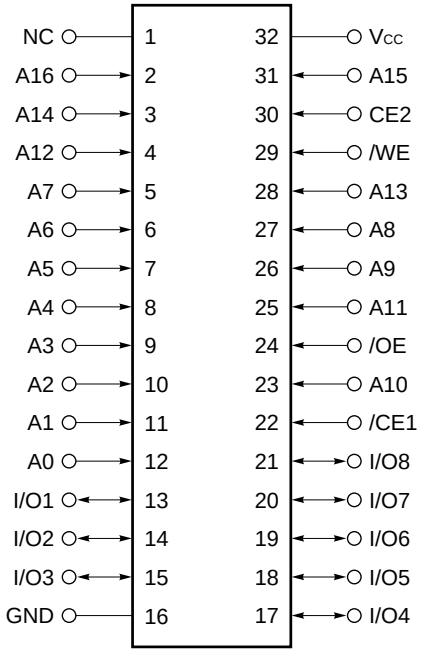

A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8×13.4) (Normal bent)

[μPD441000LGU-BxxX-9JH]

[μPD441000LGU-CxxX-9JH]

[μPD441000LGU-DxxX-9JH]

32-pin Plastic TSOP (I) (8×20) (Normal bent)

[μPD441000LGZ-BxxX-KJH]

[μPD441000LGZ-CxxX-KJH]

[μPD441000LGZ-DxxX-KJH]

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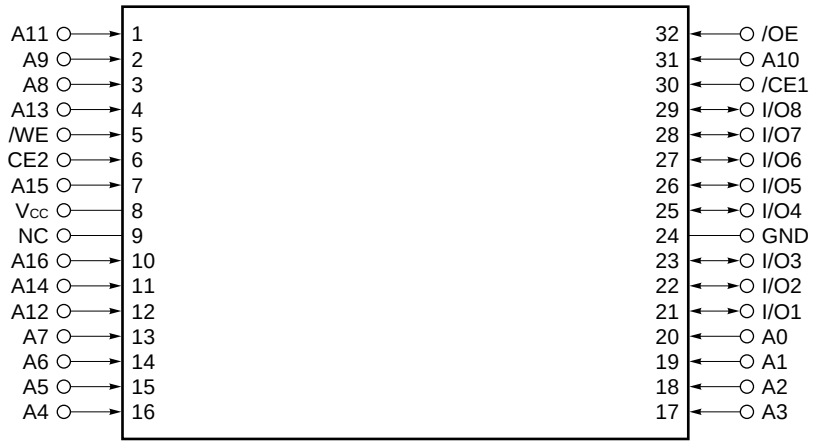

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I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)

[μPD441000LGU-BxxX-9KH]

[μPD441000LGU-CxxX-9KH]

[μPD441000LGU-DxxX-9KH]

32-pin Plastic TSOP (I) (8×20) (Reverse bent)

[μPD441000LGZ-BxxX-KKH]

[μPD441000LGZ-CxxX-KKH]

[μPD441000LGZ-DxxX-KKH]

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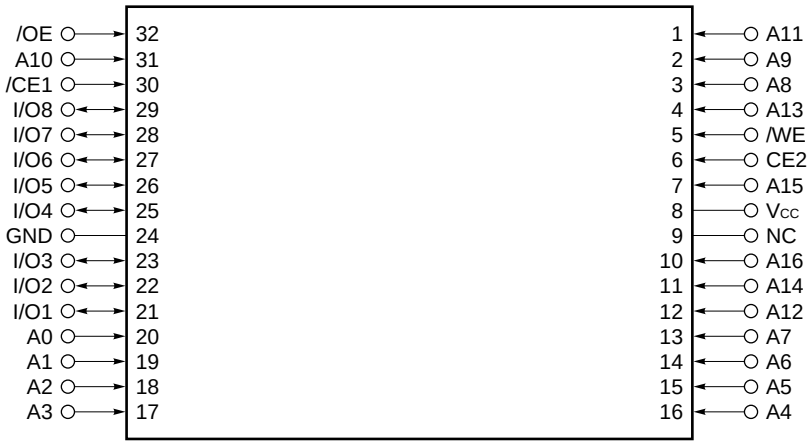

A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
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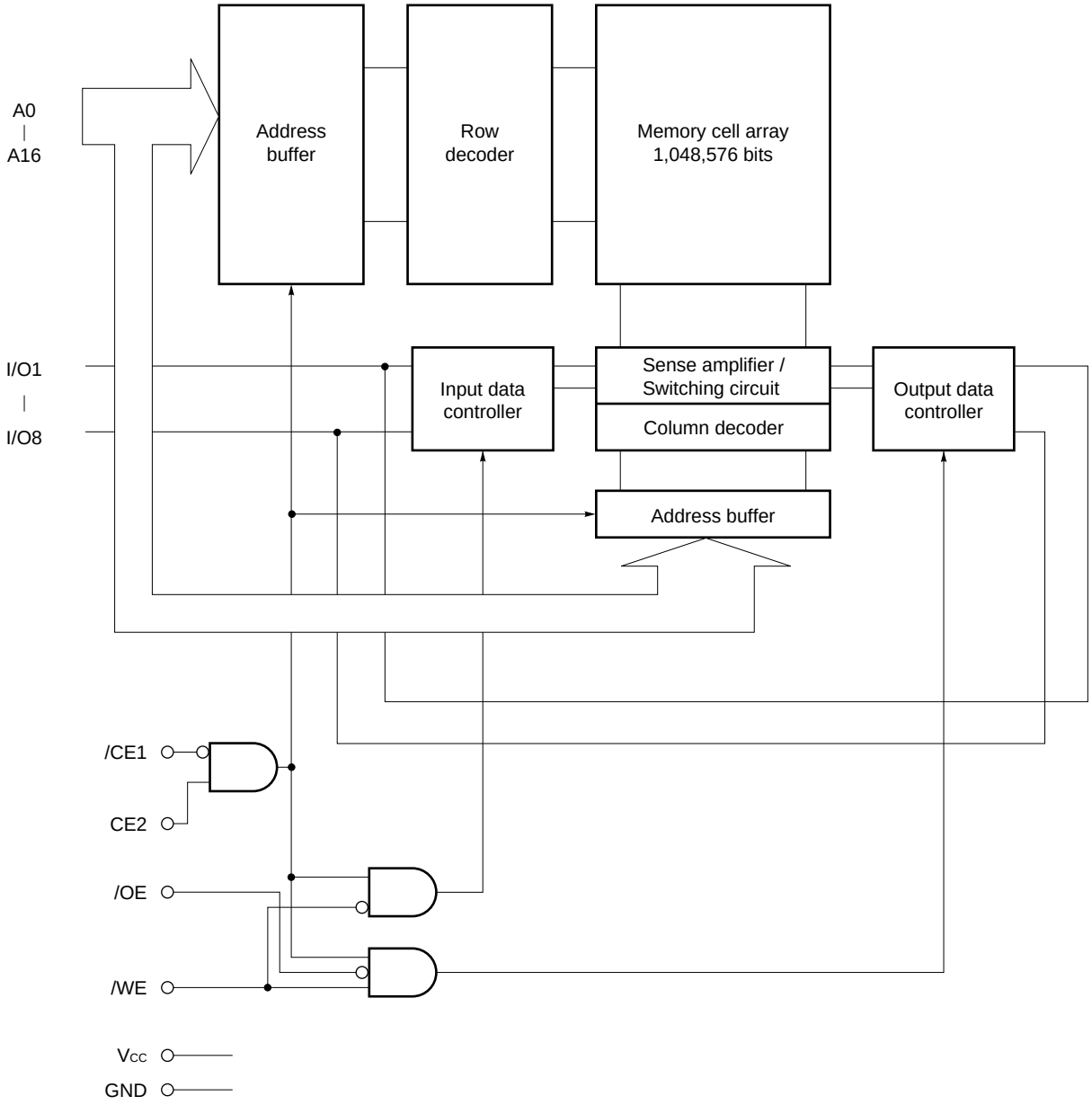
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×	Not selected	High impedance	
L	H	H	H	Output disable	High impedance	I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +4.6	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.5	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD441000L-BxxX		μPD441000L-CxxX		μPD441000L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.5	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.3	–0.3 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		μPD441000L-BxxX			μPD441000L-CxxX			μPD441000L-DxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			23	25		23	25		23	25	mA
		Minimum cycle time,	V_{CC} ≤ 2.7 V		–	–		20	23		20	23	
		$I_{I/O}$ = 0 mA	V_{CC} ≤ 2.2 V		–	–		–	–		17	20	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},				5			5			5	
		$I_{I/O}$ = 0 mA	V_{CC} ≤ 2.7 V			–			4			4	
			V_{CC} ≤ 2.2 V			–			–			3	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,				4			4			4	
		V_{IL} ≤ 0.2 V,	V_{CC} ≤ 2.7 V			–			3			3	
		V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.2 V			–			–			3	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}				0.3			0.3			0.3	mA
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.05	2		0.05	2		0.05	2	μA
		CE2 ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.7 V		–	–		0.04	2		0.04	2	
			V_{CC} ≤ 2.2 V		–	–		–	–		0.03	1.5	
	I_{SB2}	CE2 ≤ 0.2 V			0.05	2		0.05	2		0.05	2	
			V_{CC} ≤ 2.7 V		–	–		0.04	2		0.04	2	
			V_{CC} ≤ 2.2 V		–	–		–	–		0.03	1.5	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			2.4			2.4			V
			V_{CC} ≤ 2.7 V	–			1.8			1.8			
			V_{CC} ≤ 2.2 V	–			–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

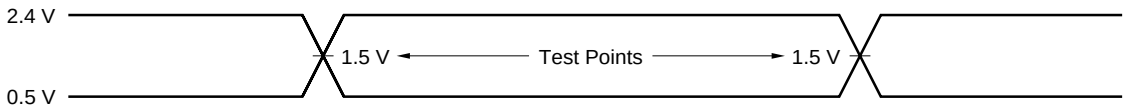
2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

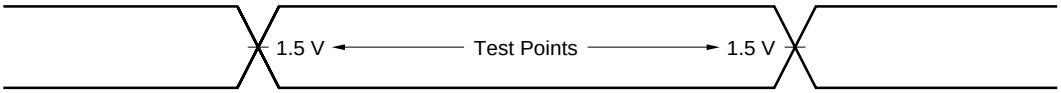
AC Test Conditions

[μPD441000L-B70X, μPD441000L-B85X, μPD441000L-B10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

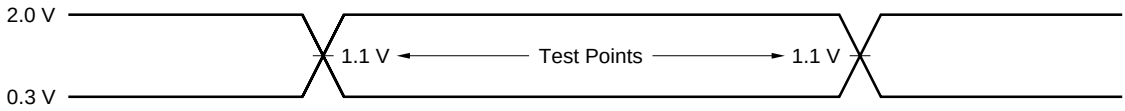


Output Load

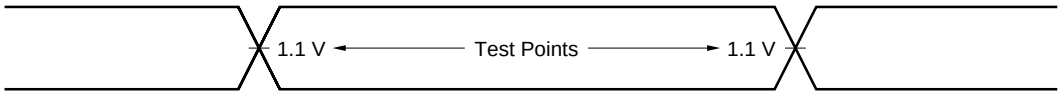
1TTL + 50 pF

[μPD441000L-C10X, μPD441000L-C12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

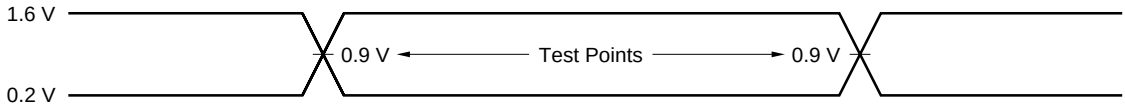


Output Load

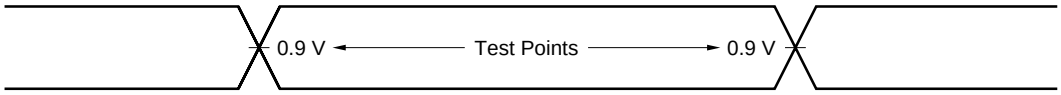
1TTL + 30 pF

[μPD441000L-D12X, μPD441000L-D15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

Read Cycle (1/3) (B version)

Parameter	Symbol	μPD441000L-B70X		μPD441000L-B85X		μPD441000L-B10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/3) (C version)

Parameter	Symbol	μPD441000L-C10X		μPD441000L-C12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	**Note 1**
/CE1 access time	t_{CO1}		100		120	ns	
CE2 access time	t_{CO2}		100		120	ns	
/OE to output valid	t_{OE}		50		60	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		35		40	ns	
CE2 to output in high impedance	t_{HZ2}		35		40	ns	
/OE to output in high impedance	t_{OHZ}		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (3/3) (D version)

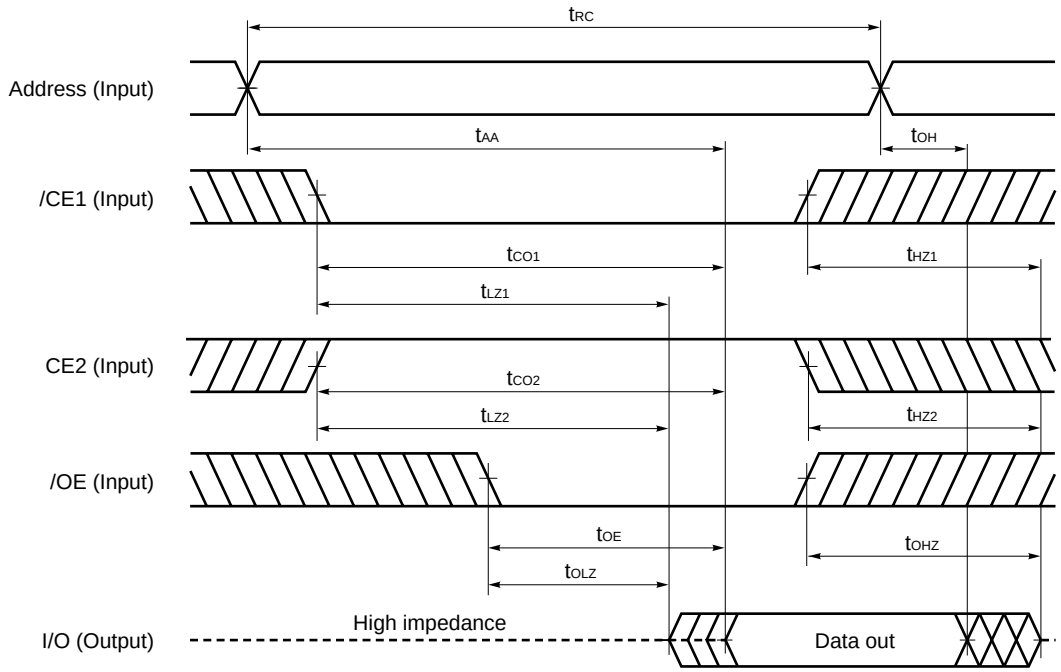
Parameter	Symbol	μPD441000L-D12X		μPD441000L-D15X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	**Note 1**
/CE1 access time	t_{CO1}		120		150	ns	
CE2 access time	t_{CO2}		120		150	ns	
/OE to output valid	t_{OE}		60		70	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		40		50	ns	
/OE to output in high impedance	t_{OHZ}		40		50	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (B version)

Parameter	Symbol	μPD441000L-B70X		μPD441000L-B85X		μPD441000L-B10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		60		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	35		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle (2/3) (C version)

Parameter	Symbol	μPD441000L-C10X		μPD441000L-C12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
/CE1 to end of write	t_{CW1}	80		100		ns	
CE2 to end of write	t_{CW2}	80		100		ns	
Address valid to end of write	t_{AW}	80		100		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	60		85		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	45		60		ns	
Data hold time	t_{DH}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

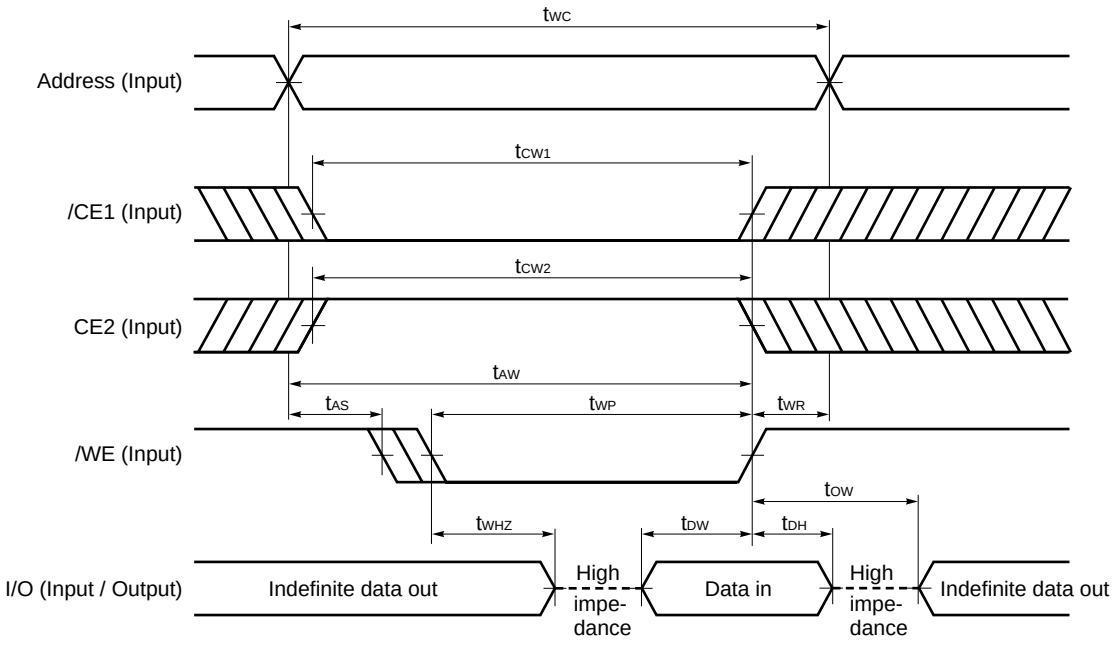
Write Cycle (3/3) (D version)

Parameter	Symbol	μPD441000L-D12X		μPD441000L-D15X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	120		150		ns	
/CE1 to end of write	t_{CW1}	100		120		ns	
CE2 to end of write	t_{CW2}	100		120		ns	
Address valid to end of write	t_{AW}	100		120		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	85		100		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	60		80		ns	
Data hold time	t_{DH}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

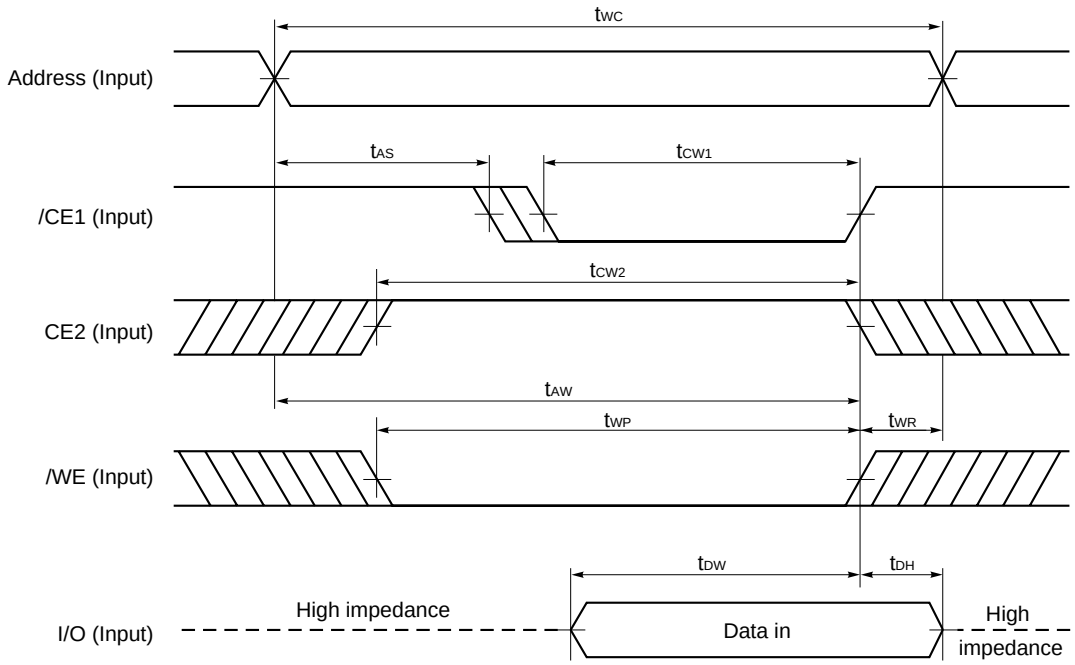
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

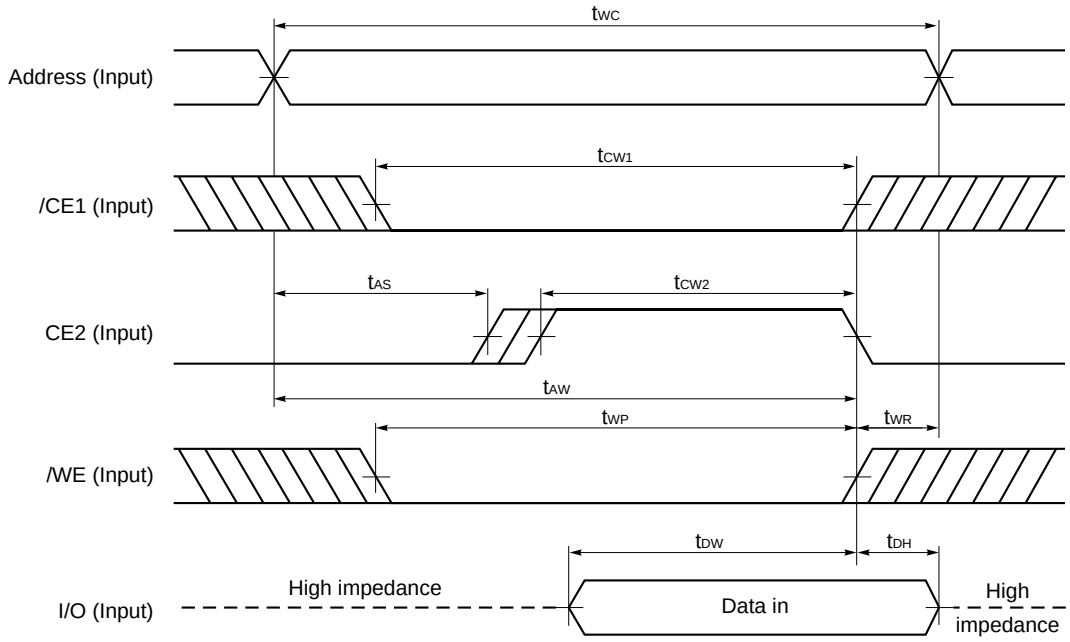


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

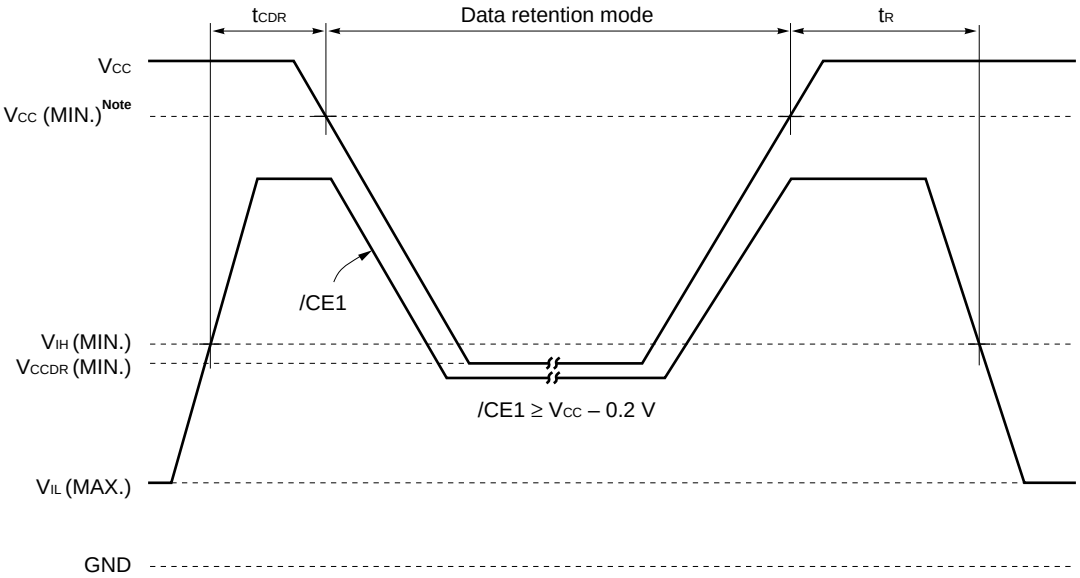
Parameter	Symbol	Test Condition	μPD441000L -BxxX			μPD441000L -CxxX			μPD441000L -DxxX			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	2		3.6	1.5		3.6	1.5		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2		3.6	1.5		3.6	1.5		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.05	2 Note		0.05	2 Note		0.05	2 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.05	2 Note		0.05	2 Note		0.05	2 Note	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		5			5			5			ms

Note 0.5 μA (T_A ≤ 40 °C)

Data Retention Timing Chart

(1) /CE1 Controlled

★

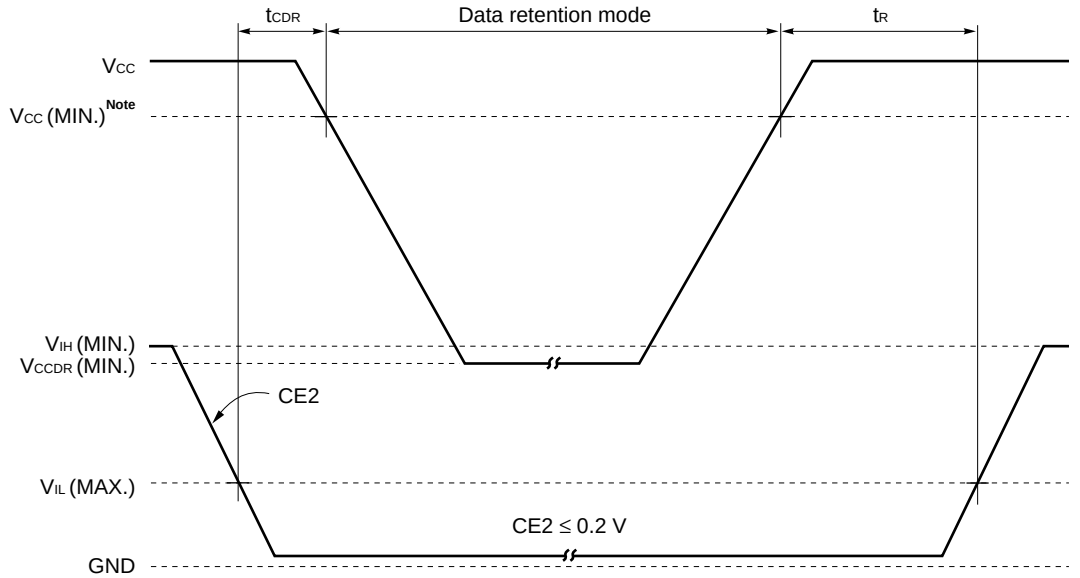


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

★

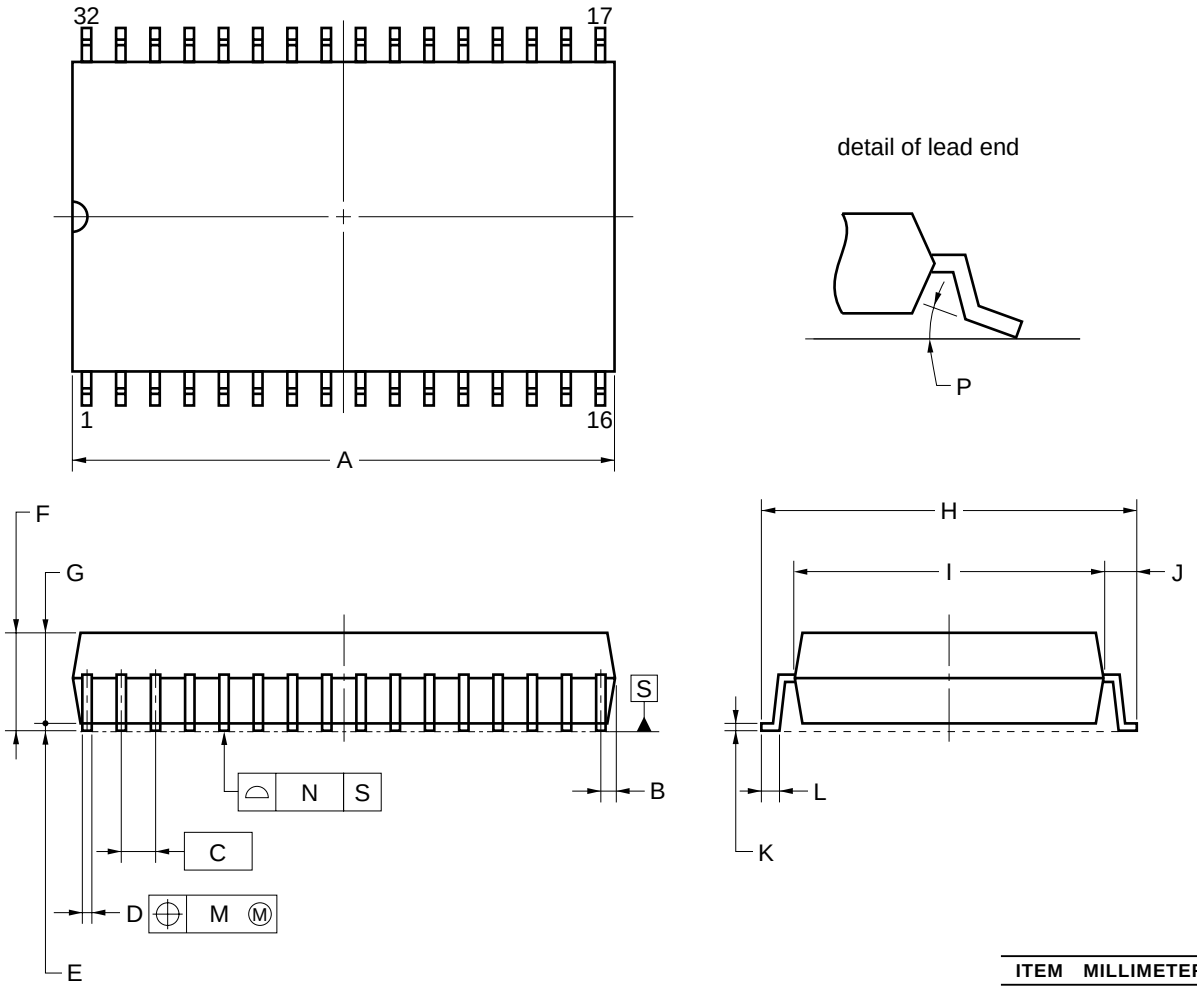


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

★ 32-PIN PLASTIC SOP (13.34 mm (525))



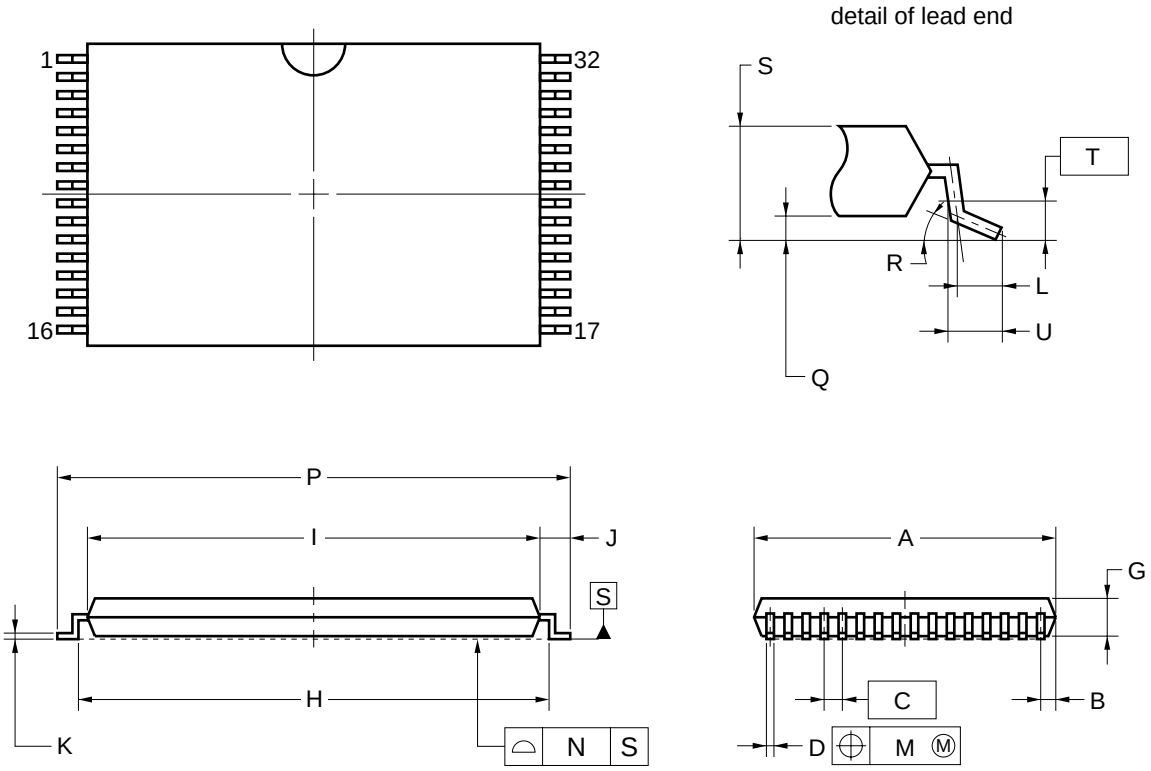
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	20.61 MAX.
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.40^{+0.10}_{-0.05}$
E	0.15±0.05
F	2.95 MAX.
G	2.7
H	14.1±0.3
I	11.3
J	1.4±0.2
K	$0.20^{+0.10}_{-0.05}$
L	0.8±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P32GW-50-525A-1

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

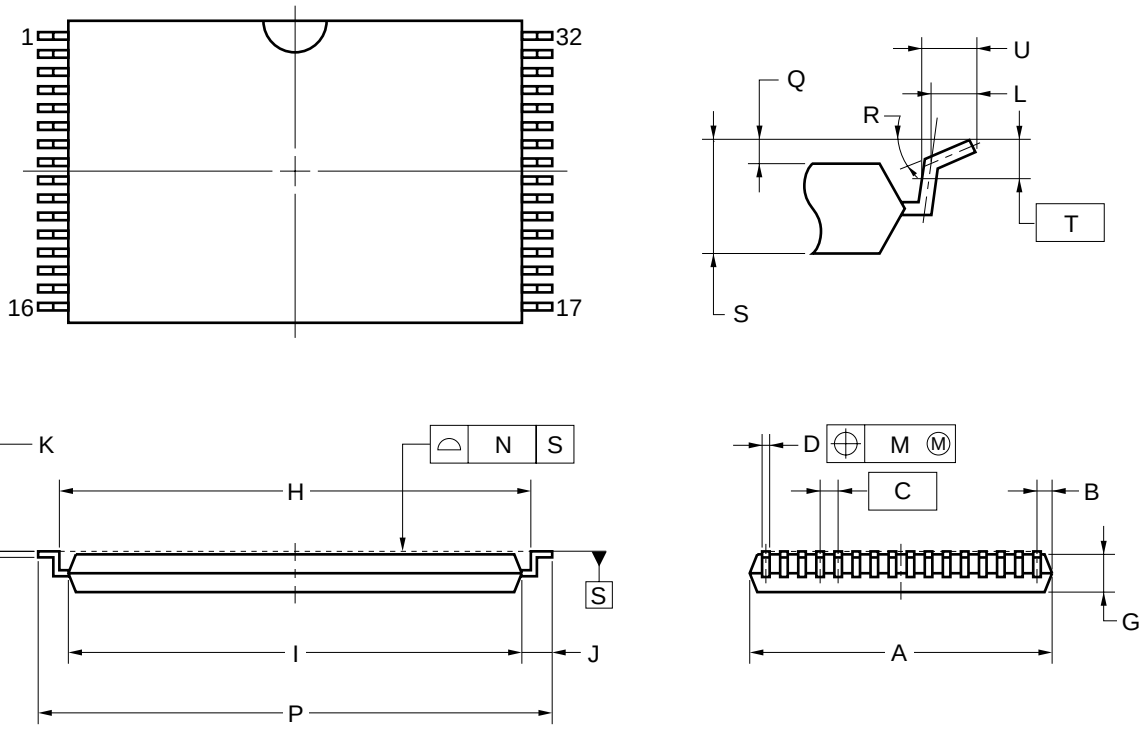
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

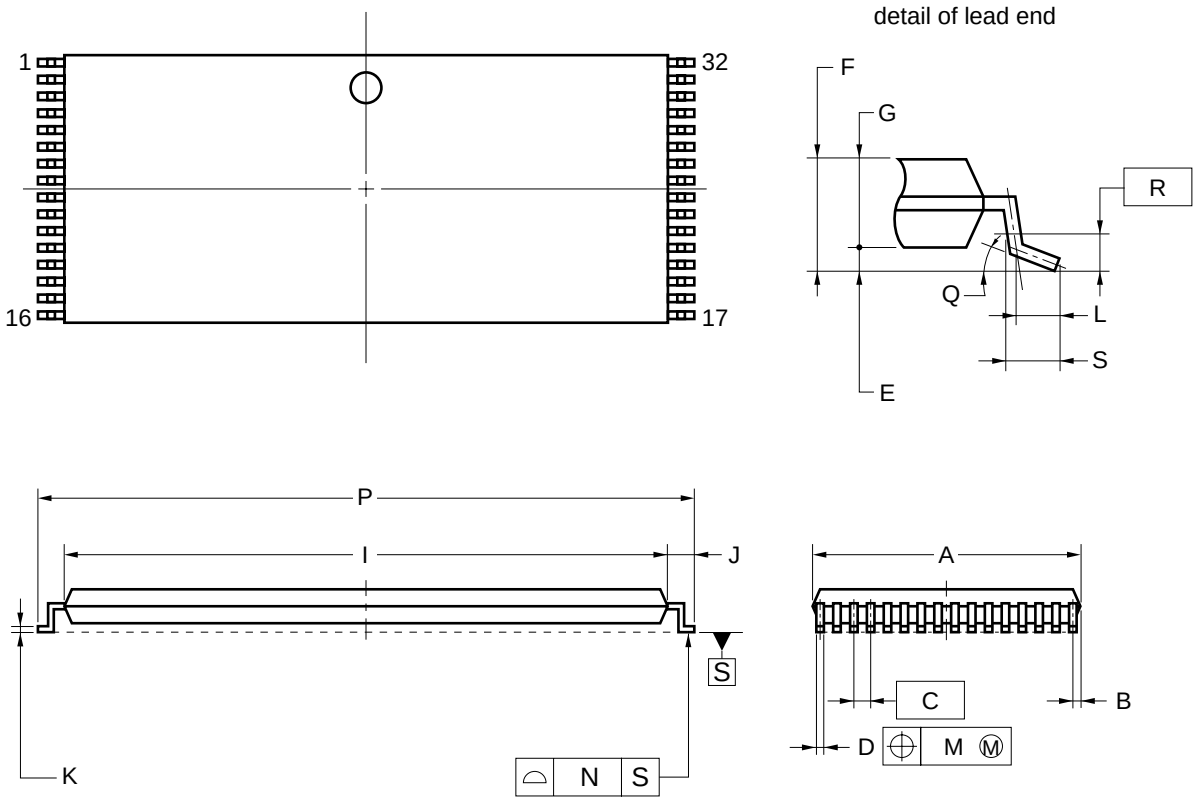
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9KH-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



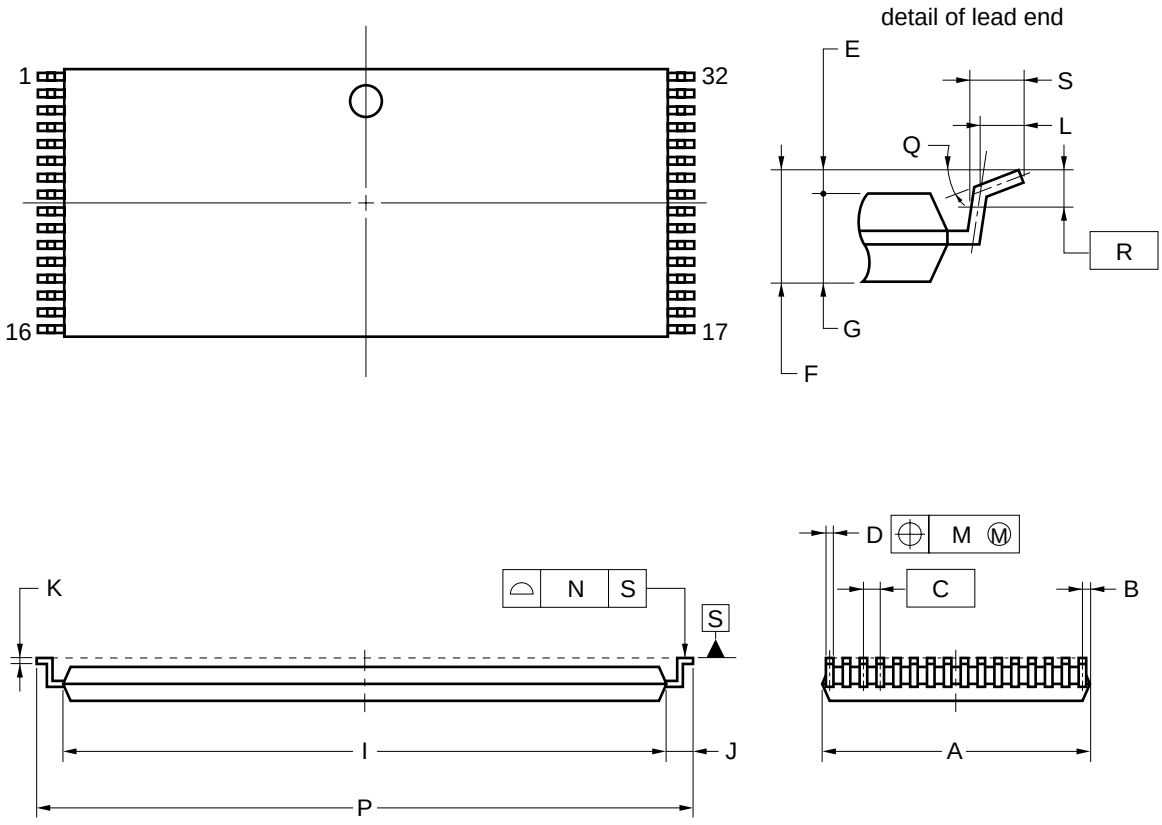
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S32GZ-50-KJH1-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S32GZ-50-KKH1-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD441000L-X.

★ Types of Surface Mount Device

μPD441000LGW-BxxX	:	32-pin Plastic SOP (13.34 mm (525))
μPD441000LGW-CxxX	:	32-pin Plastic SOP (13.34 mm (525))
μPD441000LGW-DxxX	:	32-pin Plastic SOP (13.34 mm (525))
μPD441000LGU-BxxX-9JH	:	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD441000LGU-CxxX-9JH	:	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD441000LGU-DxxX-9JH	:	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD441000LGU-BxxX-9KH	:	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD441000LGU-CxxX-9KH	:	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD441000LGU-DxxX-9KH	:	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD441000LGZ-BxxX-KJH	:	32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD441000LGZ-CxxX-KJH	:	32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD441000LGZ-DxxX-KJH	:	32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD441000LGZ-BxxX-KKH	:	32-pin Plastic TSOP (I) (8×20) (Reverse bent)
μPD441000LGZ-CxxX-KKH	:	32-pin Plastic TSOP (I) (8×20) (Reverse bent)
μPD441000LGZ-DxxX-KKH	:	32-pin Plastic TSOP (I) (8×20) (Reverse bent)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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