

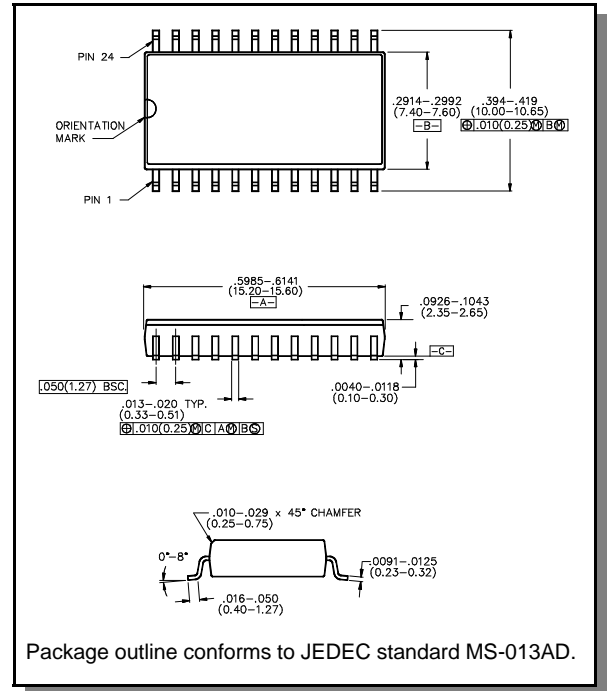
Features

- Typical Isolation: 36 dB (2,000 MHz)
- Typical Insertion Loss: 1.8 dB (2,000 MHz)
- Integral ASIC TTL/CMOS Driver
- Plastic, 50 mil Pitch, SOW-24 Lead, Wide Body
- Low DC Power Consumption
- 50 Ohm Nominal Impedance
- Tape and Reel Packaging Available
- Test Boards Available

Description

M/A-COM's SW65-0114 is a GaAs MMIC absorptive SPDT switch with an integral silicon ASIC driver. This device is in a 24-lead plastic package. This switch offers excellent broadband performance and repeatability from DC to 3 GHz, while maintaining low DC power dissipation. The SW65-0114 is ideally suited for wireless infrastructure applications. Also available in ceramic package with improved performance.

SOW-24



Electrical Specifications: $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Units	Min	Typical	Max
Insertion Loss	DC - 3.0 GHz	dB	—	1.8	2.2
Isolation (All arms off)	DC - 3.0 GHz	dB	33	36	—
VSWR	DC - 3.0 GHz	—	—	On 1.7:1 Off 2.1:1	2.2:1
T_{rise} T_{fall} T_{on} T_{off} Transients	10%/90%, 90%/10% ¹ 50% TTL to 90%/10% RF In-band (peak to peak)	nS nS mV	— — —	15 50 50	50 150 150
1 dB Compression	.05 GHz .5 - 3.0 GHz	dBm dBm	— —	+20 +27	— —
Input IP_3	Two tone inputs 0.05 GHz up to +5 dBm 0.5 - 3.0 GHz	dBm dBm	— —	+35 +46	— —
V_{CC}	—	V	+4.5	+5.0	+5.5
V_{EE}	—	V	-8.0	-5.0	-4.75
I_{CC}	$V_{CC} = +5.0\text{V}$	mA	—	—	4
I_{EE}	$V_{EE} = -5.0\text{V}$	mA	—	—	-1
Logic "0"	$I_{in} = 20\mu\text{A max}$	V	0.0	—	0.8
Logic "1"	$I_{in} = 20\mu\text{A max}$	V	2.0	—	5.0

1. Decoupling capacitors (.01 μF) are required on the power supply lines.

Absolute Maximum Ratings ^{2,3}

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 3.0 GHz	+27 dBm +34 dBm
Bias Voltages V_{EE} V_{CC} Control Voltage ⁴	-8.5V +5.5V -0.5V to V_{CC} +0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

2. Operation of this device above any one of these parameters may cause permanent damage.
3. When the RF input is applied to the terminated port, the absolute maximum power is +30 dBm.
4. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Pin Configuration

Pin #	Function	Pin #	Function
1	RFC	13	C1
2	GND	14	GND
3	GND	15	GND
4	GND	16	GND
5	GND	17	GND
6	RF2	18	GND
7	GND	19	RF1
8	V_{EE}	20	GND
9	GND	21	GND
10	V_{CC}	22	GND
11	GND	23	GND
12	C2	24	GND

Truth Table

TTL Control Input		RF Common To:	
C1	C2	RF1	RF2
1	0	On	Off
0	1	Off	On

Ordering Information

Part Number	Package
SW65-0114	Bulk Packaging
SW65-0114TR	Tape and Reel (1K Reel)
SW65-0114-TB	Units Mounted on Test Board

Specifications subject to change without notice.

- North America: Tel. (800) 366-2266
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