CIRRUS LOGIC®

CL-SH5500

Product Bulletin

FEATURES

SCSI Interface

- **Supports 8- or 16-bit Fast/Wide data bus**
- **Fast/Wide DMA/PIO transfers up to 20 Mbytes/second**
- **Supports SCSI-2 Initiator and Target Modes**
- **Data Streaming Mode with automatic disconnect and reconnect based on buffer threshold or empty/full conditions**
- **Automated SCSI phase processing for Arbitration, Selection, Message, Command, Status, and Bus Free**
- **Integrated 48-mA and active pull-up SCSI Bus drivers**
- **Supports differential SCSI Interface through differential control outputs for external drivers**

Microcontroller Interface

- **Supports high-speed microcontroller interfaces**
- **Supports multiplexed or non-multiplexed address/data microcontrollers**
- **Supports direct microcontroller access to the SCSI Bus**
- **Supports direct microcontroller access to buffer memory and eight external switches**
- **Supports auto-wait or scheduled access to WCS and buffer memory**
- **Separate host- and disk-interrupt structures for flexible interrupt or polled-firmware design**

(cont.)

High-Performance Fast/Wide SCSI Disk Controller

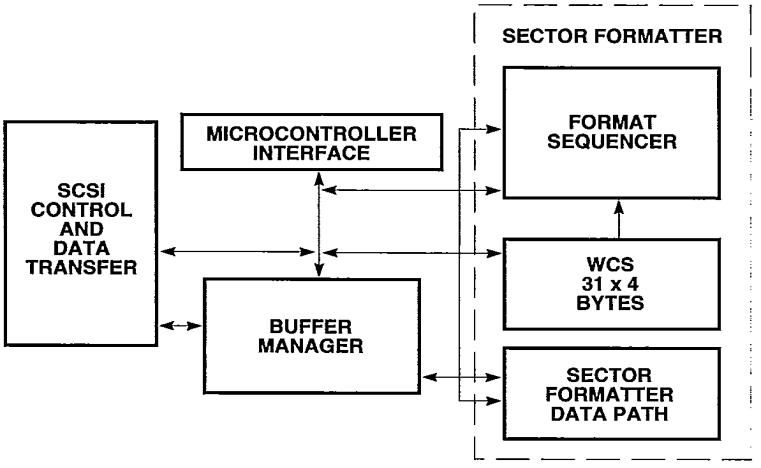
OVERVIEW

The CL-SH5500 is a high-performance, high-speed single-chip controller for disk drive systems. The CL-SH5500 design combines a local microcontroller port, extensive hardware support for the SCSI interface, a five-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SH5500, along with a local microcontroller, system ROM and RAM, and an optional data separator, completes a disk controller subsystem with high performance at a low overall cost.

The SCSI Host interface is designed for compliance with the SCSI-2 specification. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SH5500. The CL-SH5500 has significant SCSI automation features that minimize command overhead and firmware intervention. Routine bus control operations such as arbitration, selection and reselection are automati-

(cont.)

Functional Block Diagram



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High-Performance SCSI Disk Controller

FEATURES (cont.)

Sector Formatter

- Full-track multi-sector transfer capability
- Transfers SCSI information to/from the microcontroller through a 24-byte FIFO under Automatic Programmed I/O (PIO)
- Programmable Format Sequencer Writable Control Store (WCS — 31 x 4 bytes)
- Supports up to 72-Mbit NRZ data rates
- 1-bit serial or 2-bit parallel NRZ interface
- Allows split data field processing for embedded servo and zoned designs
- Provides 16-bit CRC and 88-bit Reed-Solomon ECC with on-the-fly correction
- Programmable on-the-fly error burst length

Buffer Manager

- Supports 8- or 16-bit buffer memory data lines
- Five-channel, circular buffer control with priority resolution
- Direct buffer addressing up to 256K bytes of SRAM and 4 Mbytes of DRAM
- Supports scatter/gather operation for LRU cache support
- Supports Streaming Mode, and automatic host and disk operation in the same circular buffer simultaneously (with a mechanism to prevent overrun and underrun)
- Supports multi-track, minimal-latency operations
- Permits concurrent buffer memory throughput of up to 40 Mbytes/second
- Flexible buffer segmentation logic
- Automatic SCSI disconnect/reconnect with local interrupt for programmable buffer threshold and buffer empty/full conditions

Technology

- 128-pin Quad Flat Pack (SQFP) package
- Advanced, low-power, double-metal CMOS technology

OVERVIEW (cont.)

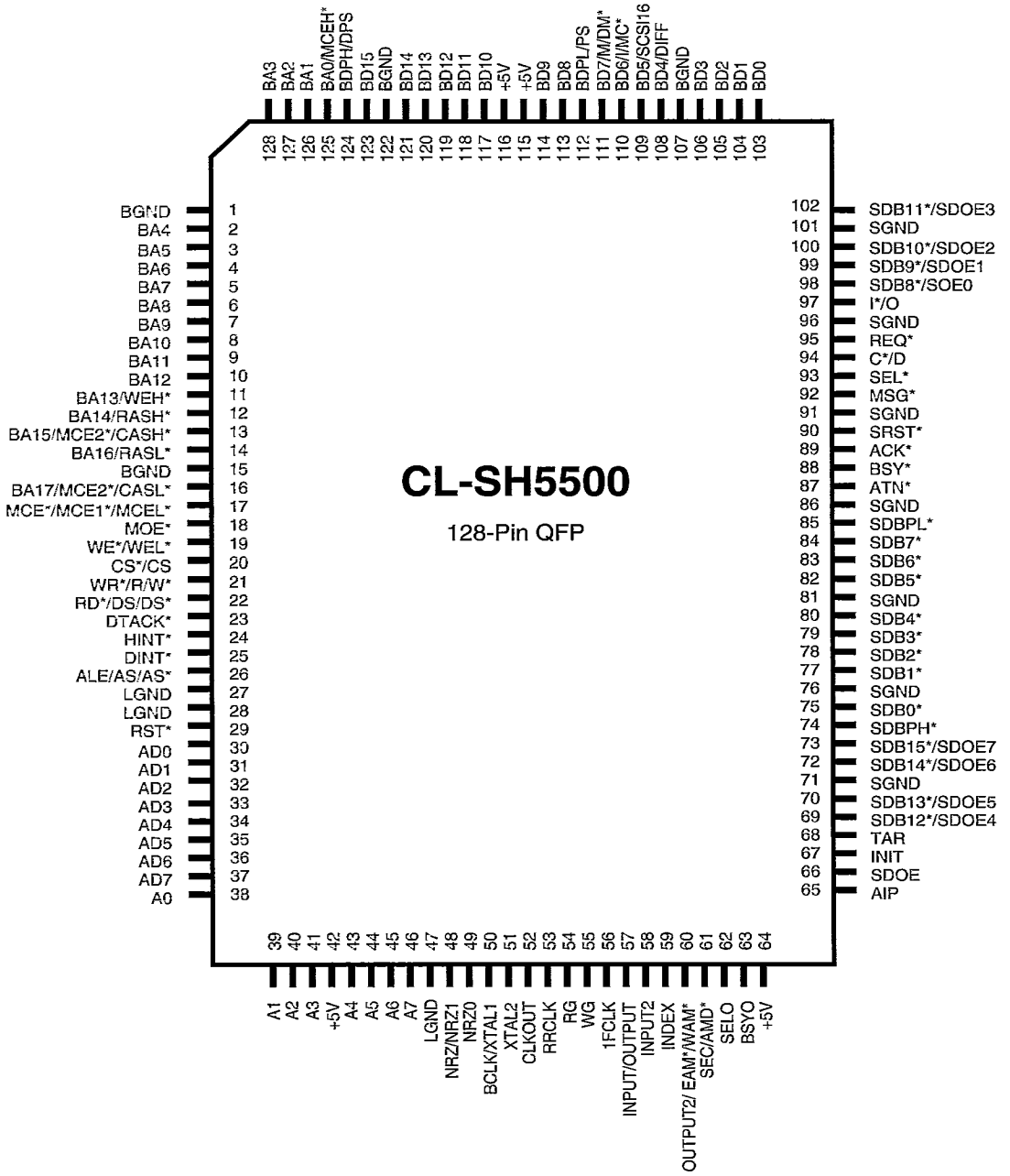
cally sequenced in hardware. Additionally, the CL-SH5500 automatically handles SCSI selection with messages (identify, tag) and/or command. The receive command, disconnect sequence and command-complete sequence are also automated.

A local microcontroller provides the CL-SH5500 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host control. During data transfer operations, the CL-SH5500 requires only minimal intervention from the local microcontroller.

The microcontroller–to–CL-SH5500 communication path is a multiplexed/non-multiplexed address and data bus similar to that provided by the Intel® 80196 and the Motorola® 68HC11 class of controllers. (There is a configuration signal available to allow for either family of data control signal methods). The CL-SH5500 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 72 Mbits and can perform automatic multi-sector transfers up to a complete track, while handling multiple data-segments per sector. The Sector Formatter is subdivided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter data path consists of the NRZ-data-handling circuitry that includes the serializer/deserializer (SERDES), the 88-bit Reed-Solomon ECC and 16-bit CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The component is programmable to provide all of the necessary address and control signals for RAM devices of varying access times. The CL-SH5500 also allows fully automatic host-to-media and media-to-host multisector transfers, while monitoring the state of the buffer to identify buffer full/empty conditions, and programmable data thresholds. These conditions are monitored to automatically disconnect or reconnect from the SCSI Bus.



CL-SH5500 Pin Diagram

CL-SH5500

High-Performance SCSI Disk Controller

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PIN DESCRIPTION

Symbol	Pin Number	Type	Description
Microcontroller Interface Pins			
CS*/CS	20	I	Chip Select
WR*/R/W*	21	I	Write Strobe/ Read/Write
RD*/DS/DS*	22	I	Read Strobe/ Data Strobe
DTACK*	23	OD	Data Transfer Acknowledge
HINT*	24	O, OD, Z	Host Interrupt
DINT*	25	O, OD, Z	Disk Interrupt
ALE/AS/AS*	26	I	Address Latch Enable/ Address Strobe
RST*	29	I	Reset
AD0:7	30-37	I/O	Local Microcontroller Address/Data Bus
A[0:7]	38-41, 43-46	I/O	Local Microcontroller Address Bus
SCSI Bus Interface Pins			
SDB0*:7*	75, 77-80, 82-84	I/O	SCSI Data Bus
SDBLP*	85	I/O	SCSI Data Bus Low Parity
SDB8*:15*/SDOE0:7	98-100, 102, 69-70, 72-73	I/O	SCSI Data Bus/ SCSI Data Bus Enable
SDBHP*	74	I/O	SCSI Data Bus High Parity
ATN*	87	I/O	SCSI Attention
BSY*	88	I/O, OD	SCSI Busy
ACK*	89	I/O	SCSI Acknowledge
SRST*	90	I/O, OD	SCSI Reset
MSG*	92	I/O	SCSI Message
SEL*	93	I/O, OD	SCSI Select
C*/D	94	I/O	SCSI Command/Data
REQ*	95	I/O	SCSI Request
I*/O	97	I/O	SCSI Input/Output
SDOE	66	I/O	SCSI Data Bus Output Enable
INIT	67	I/O	Initiator
TAR	68	I/O	Target
AIP	64	I/O	Arbitration in Progress
BSYO	63	I/O	Busy Out
SELO	62	I/O	Select Out
Buffer Manager Interface Pins			
BD0:3	103-106, 108-109	I/O	Buffer Memory Data Bus 0:3
BD4/DIFF	108	I/O	Buffer Memory Data Bus 4/ Differential Configuration
BD5/SCSI16	109	I/O	Buffer Memory Data Bus 5/ SCSI 16-Bit Select
BD6/I/MC*	110	I/O	Buffer Memory Data Bus 6/ Intel/Motorola Configuration
BD7/M/DM*	111	I/O	Buffer Memory Data Bus 7/ Multiplexed/Demultiplexed Address Configuration
BDPL/PS	112	I/O	Buffer Memory Data Parity Low/ Polarity Select
BD8:15	113-114, 117-121	I/O	Buffer Memory Data Bus
BDPH/DPS	124	I/O	Buffer Memory Data Parity High/ Readgate/Writegate Polarity Select
BA0/MCEH*	125	O	Buffer Memory Address Line 0/ MCEH*
BA1:12	126-128, 2-10	O	Buffer Memory Address Lines 1:12
BA13/WEH*	11	O	Buffer Memory Address Line 13/ WEH*
BA14/RASH*	12	O	Buffer Memory Address 14/ RASH*
BA15/MCE2*/CASH*	13	O	Buffer Memory Address 15/ MCE2*/ CASH*
BA16/RASL*	14	O	Buffer Memory Address 16/ RASL*
BA17/MCE2*/CASL*	16	O	Buffer Memory Address 17/ MCE2*/ CAS*
MCE*/MCE1*/MCEL*	17	O	Memory Chip Enable/ Memory Chip Enable1/ Memory Chip Enable Low
MOE*	18	O	Memory Output Enable
WE*/WEL*	19	O	Write Enable
BCLK/XTAL1	50	I	System Clock/ XTAL1
XTAL2	51	O	XTAL2
CLKOUT	52	O	Clock Output
Sector Formatter Interface Pins			
NRZ0	49	I/O	NRZ0
NRZ/NRZ1	48	I/O	Non Return to Zero
RRCLK	53	I	Read Reference Clock
RG	54	O	Read Gate
WG	55	O	Write Gate
1FCLK	56	I	1FCLK
INPUT/OUTPUT	57	I/O	Format Sequencer Input/Output
INPUT2	58	I/O	Input2
INDEX	59	I	Index
OUTPUT2/EAM*/WAM*	60	O	Output2/ Enable Address Mark/ Write Address Mark
SECTOR/AMD*	61	I/O	Sector/ Address Mark Detect
Power and Ground Pins			
BGND	1, 15, 107, 122	N/A	Buffer Ground Pins
LGND	27, 28, 47	N/A	Logic Ground Pins
+5V	43, 65, 115, 116	N/A	Power Supply (+5 volt) Pins
SGND	71, 76, 81, 86, 91, 96, 101	N/A	High Current SCSI Ground Pins

NOTES: * denotes negative-true signal. I indicates input pin; O indicates output pin; I/O indicates input/output pin; OD indicates open-drain output pin; Z indicates three-state output or input/output pins. All unused input pins must be tied to GND or VDD appropriately. SGND, BGND, and LGND are connected to three separate ground rings internally.

CL-SH5500

High-Performance SCSI Disk Controller

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ADVANTAGES

Unique Features	Benefits
• *16-bit Fast/Wide SCSI Data Bus*	Allows 20-Mbytes/second SCSI transfers.
• *Automatic disconnect/reconnect on programmable buffer empty/full threshold*	Optimizes SCSI Bus utilization.
• *Automatic multisector transfer between host and disk*	Reduces local microcontroller real-time response.
• *Programmable wait states for microcontroller*	Allows the fastest microcontrollers to operate without degrading bus performance.
• *Separate disk and host microcontroller interrupts*	Supports faster, more direct interrupt processing by microcontroller.
• *15-byte or -word offset in Synchronous Mode*	Greater flexibility for synchronous data transfer negotiations.
• *24-byte FIFO for automatic PIO transfers*	Decreases command and information transfer overhead.
• *Five Buffer Manager DMA channels*	Enables read-look-ahead for high performance.
• *Direct 256-Kbyte–SRAM or 4-Mbyte–DRAM addressing*	Increases buffer size alternatives to support caching.
• *Verification of odd parity through the buffer*	Improves data integrity between host and disk data transfers.
• *Variable buffer segmentation logic*	Allows protected data segments in buffer.
• *Advanced-programmable branch conditions in the Writable Control Store (WCS) program*	Supports flexible, automated defect management and retry algorithms.
• *Conditional Format Sequencer execution of up to four paths*	Supports end-of-track, retry and defect management code.
• *Programmable read synchronization timeout*	Simplifies ID and Data Field searches.
• *'On-the-fly' error correction circuitry*	Enables high-speed ECC correction within half of a sector time period.
• *Multiple data field processing within the ECC*	Provides support for embedded servo drives, zoned-recorded drives, and large defect skipping.
• *Minimal latency support*	Reduces the rotational latency by an average of one-half revolution.
• *Programmable power management*	Reduces power consumption for small form-factor drives.
• *2-bit parallel NRZ interface*	Faster data transfers to/from the controller.